Miniature Four-Way and Two-Way 24 GHz Wilkinson Power Dividers in 0.13 μm CMOS

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***Abstract*—This letter presents 24 GHz four-way and two-way miniature Wilkinson power dividers (PDs) in a standard CMOS technology. The chip area is significantly reduced using a lumped-element design, and the effective areas of four-way and two-way Wilkinson dividers are 0.33×0.33 mm^2 and 0.12×0.29 mm^2, respectively. The four-way Wilkinson divider results in an insertion loss $<$2.4 dB, an input/output return loss better 15.5 dB, and a port-to-port isolation $>$24.7 dB from 22 to 26 GHz. The two-way Wilkinson divider results in an insertion loss $<$1.4 dB, an input/output return loss better 8.9 dB, and a port-to-port isolation $>$14.8 dB from 22 to 26 GHz. To the author's knowledge, this is the first demonstration of 24 GHz four-way Wilkinson PD in a standard CMOS technology.**

***Index Terms*—CMOS, four-way power divider (PD), lumped PD, 24 GHz, Wilkinson PD.**

I. Introduction

THE 24 GHz frequency range recently became very important due to short range automotive radar and phased-array antenna applications [1], [2]. For these applications, Wilkinson power dividers (PDs) and combining networks are widely used and have low insertion loss and high isolation characteristics [3]. However, at 24 GHz, the length of $\lambda/4$ transmission line is still too long to be integrated in an RFIC process. A lumped Wilkinson PD using micromachining technology was proposed [4], but this is not available in a standard CMOS process. Recently, a Wilkinson PD with CMOS active inductors was presented [5], but this design suffers from potential linearity and power handling problems. Another issue in Wilkinson PDs is multiway capabilities, and a binary-tree connection of two-way Wilkinson PDs occupies a very large area. Therefore, an N-way Wilkinson PD is an excellent candidate for reduced size [6], [7].

In this letter, 24-GHz four-way and two-way miniature Wilkinson PDs are presented in a standard CMOS technology.

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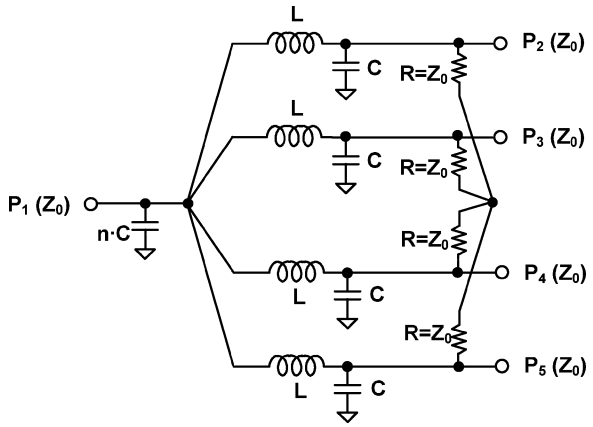

Fig. 1. Four-way lumped-element Wilkinson PD.

II. Design of Miniaturized Wilkinson PDs

Fig. 1 presents a lumped-element implementation of a four-way Wilkinson PD. The values of L and C are determined by

$$L = \frac{Z_T}{2\pi f}, \quad C = \frac{1}{2\pi f Z_T} \tag{1}$$

where Z_T is the characteristic impedance of the equivalent $\lambda/4$ transmission line. In the case of four-way Wilkinson PDs, the characteristic impedance of the $\lambda/4$ transmission line is $2Z_0$ and the isolation resistance is Z_0. Therefore, the calculated series inductance is about 660 pH and the shunt capacitance is about 66 fF at 24 GHz for an input/output port impedance of 50 Ω. The inductor is designed with Sonnet[1]. The top metal (4-μm thick) in the IBM 8RF-DM process is used to reduce the ohmic loss of the inductor, and the simulated quality factor of the inductor is about 14 at 24 GHz. Because the shunt capacitance is too small to implement with MIM capacitors, interdigital capacitors [$C2 \sim C5$ in Fig. 2(b)] are used in the four-way Wilkinson PD at each output ports. However, at the input node, the shunt capacitance is 4C, and an MIM capacitor [C1 in Fig. 2(a)] is used. $N+$ resistors of 50 Ω value, shown in Fig. 2(b), are used as isolation resistors because they can be implemented below the interconnection metals and have a low sheet resistance of 73 $\Omega/\square$. The resistors and the interdigital capacitors are placed under the common input node to reduce the chip size and result in a symmetric layout. In fact, the layout is perfectly symmetric to ensure equal response for all four output ports. For measurement purposes, two ports (P4, P5) among the

[1]* Sonnet–2.5D EM simulator of Sonnet Software Inc.

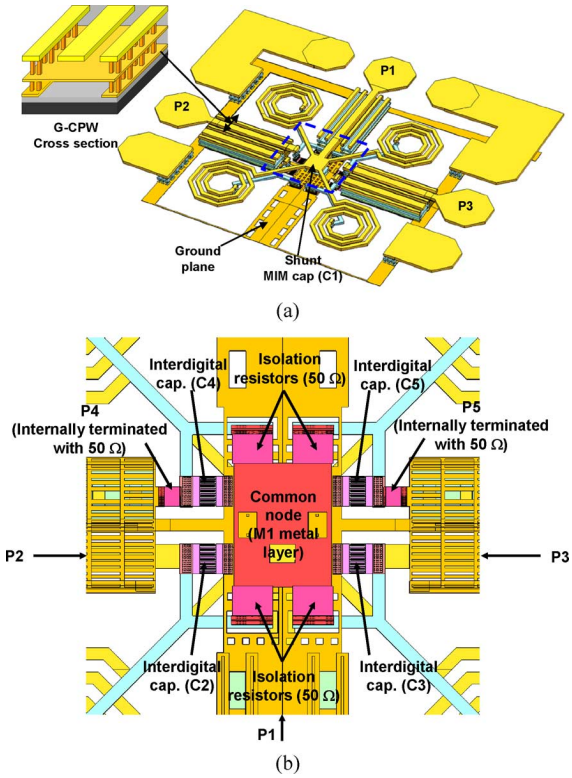

Fig. 2. (a) 3-D view of the four-way Wilkinson power combiner. (b) Bottom view of the four-way Wilkinson power combiner.

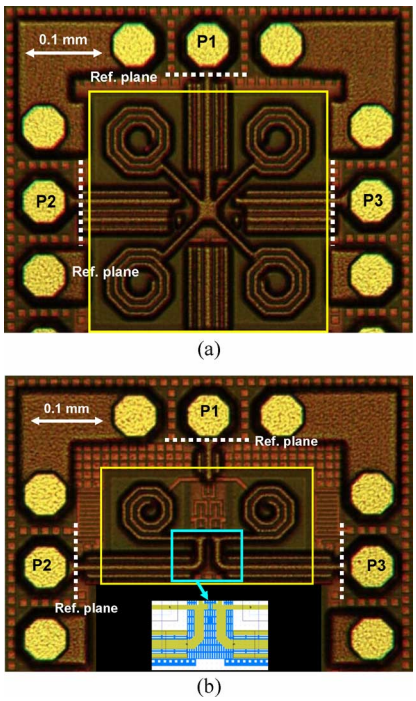

Fig. 3. Microphotograph of the fabricated (a) four-way (0.33×0.33 mm^2), and (b) two-way (0.12×0.29 mm^2) Wilkinson PDs.

four output ports are internally terminated with 50-Ω resistors in the four-way Wilkinson PD as shown in Fig. 2(b). Grounded 50 Ω CPW transmission lines (G-CPW) are used for interconnection to the probing pads [Fig. 2(a)]. The simulated loss of the G-CPW line is about 0.34 dB/mm at 24 GHz.

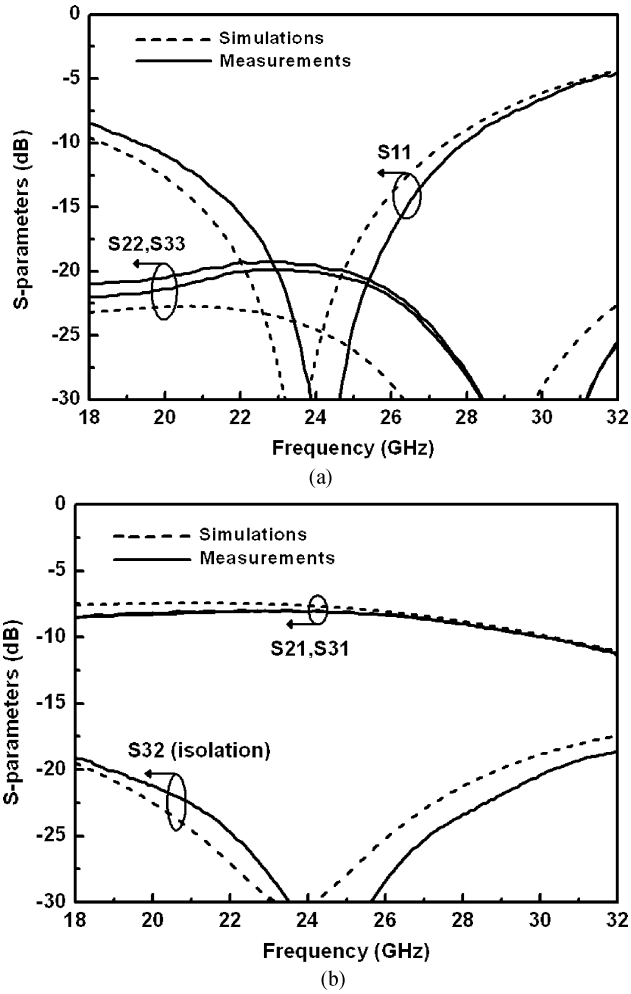

Fig. 4. (a) Measured input/output return losses of the four-way Wilkinson PD (port 4 and 5 are internally terminated with 50 Ω resistors). (b) Measured insertion losses and isolation of the four-way Wilkinson PD. There is no difference between measured S21 and S31 due to symmetry.

In the case of the two-way Wilkinson PD, the calculated inductance of L and the capacitance of C are about 470 pH and about 94 fF, respectively, at 24 GHz for an input/output port impedance of 50 Ω. The simulated quality factor of the inductor is about 17 at 24 GHz. Because the shunt capacitance (C) is small, two MIM capacitors are connected in series at the two output nodes, and a single MIM capacitor (2C) is connected at the combined input node. A TaN 100 Ω resistor which has highest accuracy among the provided resistors is used as an isolation resistor (60 Ω/□). Because TaN is fabricated under the top metal layer, it is easy to interconnect with the inductors and MIM capacitors, and therefore the via inductance is negligible. To reduce the imbalances between two output ports, a fully symmetric layout is performed.

The four-way and two-way Wilkinson PDs were simulated using Sonnet to take into account the interaction between the different inductors. The resistors and capacitors were not included in the Sonnet simulation due to their small features. The S-parameters of the networks which were obtained using Sonnet were used in a Spectre-RF simulation together with lumped element models of the resistors and capacitors. The

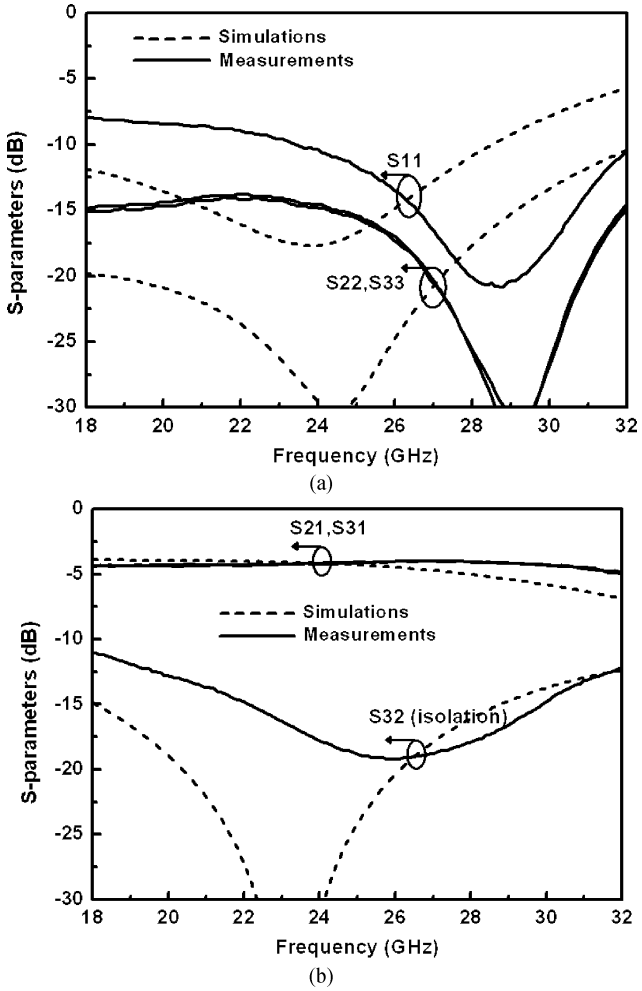

Fig. 5. (a) Measured input/output return losses of the two-way Wilkinson PD. (b) Measured insertion losses and isolation of the two-way Wilkinson PD.

simulated S-parameters of full networks are shown in Figs. 4 and 5.

III. Measured Results

The Wilkinson PDs are fabricated in a standard 0.13 μm CMOS technology (Fig. 3). The effective areas of four-way and two-way Wilkinson dividers are 0.33×0.33 mm^2 and 0.12×0.29 mm^2, respectively. SOLT calibration is performed and the probing pads are deembedded with the pad model of the provided design kit. Fig. 4 presents the simulated and the measured results of four-way Wilkinson PD. An insertion loss $<$2.4 dB, an isolation $>$24.7 dB, a return loss $<$15.5 dB at the input port, and a return loss $<$ 19.2 dB at the output port are achieved from 22 to 26 GHz. The measurements of the four-way Wilkinson power combiner agree well with the simulation results. View of the identical measured results between S_{21} and S_{31} over 18–32 GHz, we are confident that the

TABLE I
Summary of Four-Way and Two-Way Wilkinson PDs

	4-Way Wilkinson		2-Way Wilkinson
Operation freq. (GHz)	22 ~ 26	20 ~ 28	22 ~ 26
Insertion loss (dB)	< 2.4	< 3.0	< 1.4
Input return loss (dB)	< 15.5	< 9.8	< 8.9
Output return loss (dB)	< 19.2	< 19.2	< 13.8
Isolation (dB)	> 24.7	> 21.2	> 14.8
Size* (mm^2)	0.33 × 0.33		0.12 × 0.29

* Excluding pads

symmetrical crossover at the center of the four-way Wilkinson is not introducing any detrimental parasitic effects and that S_{41} and S_{51} will be the same as S_{21} and S_{31}. The same reasoning applies for S_{23} and S_{45}.

For the two-way Wilkinson PD, an insertion loss $<$1.4 dB, an isolation $>$ 14.8 dB, a return loss $<$8.9 dB at the input port, and a return loss $<$13.8 dB at the output port are achieved from 22 to 26 GHz. The frequency shift to higher frequency is due to smaller capacitance than the designed values. Again, S_{21} and S_{31} are identical over the entire frequency range.

The measured results of four-way and two-way Wilkinson PDs are summarized in Table I.

IV. Conclusion

This letter presents 24 GHz miniaturized lumped π-networks four-way and two-way Wilkinson PDs with a commercially available CMOS technology with excellent performance. The PDs can be integrated with CMOS RFICs without any additional process techniques.

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