

170-GHz Transceiver with On-Chip Antennas in SiGe Technology

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Abstract — A single-chip transceiver with on-die transmit and receive antennas, Rx and Tx amplifiers, 165-GHz oscillator and static frequency divider is reported in a SiGe HBT process with f_T/f_{MAX} of 270GHz/340GHz. This marks the highest frequency transceiver in silicon and the highest level of functional integration above 100 GHz in any semiconductor technology. The downconversion gain peaks at -5 dB and the transmit power is -5 dBm when measured at the transceiver pads. Both degrade by approximately 25 dB when measured above the antennas of the transceiver with on-die antennas. The experimental performance of dipole (with and without floating metal strips) and patch antennas is also investigated. The measured 15-dB gain of a standalone amplifier is centered at 170 GHz and remains higher than 10 dB from 160 GHz to 180 GHz while the saturated output power is 0 dBm at 165 GHz.

Index Terms — SiGe HBT technology, mm-wave transceivers, integrated antenna, amplifiers, frequency divider

I. INTRODUCTION

The increase in the cutoff and oscillation frequencies of silicon transistors has continued unabated, allowing for single-chip transceivers to break the 100-GHz barrier [1]. This opens up opportunities for new, very-short range imagers for dental and medical applications where sub-mm resolution is required over distances of several centimeters. Although 100+GHz systems on chip are now feasible at room temperature, one of the significant hurdles that remain is posed by packaging. The flip-chip pad capacitance and design rules continue to remain too large and too coarse to be useful above 100 GHz in silicon technologies with a conventional thin dielectric and thin-metal BEOL. Although antennas with +2dBi gain have been demonstrated in silicon ICs at 77 GHz [2], the multi-chip packaging and the lens required to achieve such performance fall short of the packaging-free promise of on-die antennas. In this paper we explore three different 170-GHz antenna designs for integration in a digital 130-nm CMOS backend and we demonstrate successful operation of a single-chip transceiver which includes two antennas and yet satisfies the strict metal density rules of 130-nm SiGe BiCMOS production technology.

II. TRANSCEIVER ARCHITECTURE

The transceiver block diagram is shown in Fig. 1. It re-uses the 165-GHz push-push differential oscillator and Gilbert-cell mixer of [1], along with a new 160-to-180 GHz amplifier, the static frequency divider from [3], and receive and transmit antennas. Three identical amplifiers are included on the

transmit, receive, and LO paths, respectively, to significantly improve the transmitter output power and the receiver downconversion gain when compared to the circuit presented in [1].

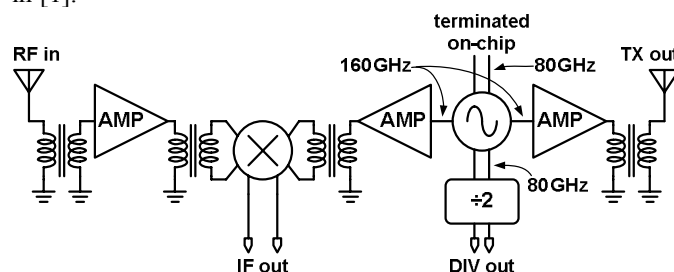


Fig. 1. 160-to-180 GHz transceiver block diagram.

Transformers are employed at the interfaces between circuit blocks to provide good isolation by separating the bias supply planes, and for single-ended to differential conversion. One of the two 80-GHz differential outputs of the oscillator drives an on-die divider [3] to demonstrate the feasibility of integrating an on-chip PLL together with the LO distribution network.

III. AMPLIFIER DESIGN

A frequency-scaled version of the five-stage 140-GHz amplifier in [1] was designed to operate in the 160-GHz to 180-GHz range. Its schematic is illustrated in Fig. 2 and consists of three cascode stages followed by two common-emitter stages. The last stage is composed of two devices, with CBEB layout configuration, connected in parallel to achieve higher output power. The input and output matching networks of the three amplifiers are modified so as to allow for maximum power transfer from the oscillator, to the mixer, or to and from the 50-Ω antenna impedance, depending on where the amplifier is located in the block diagram of Fig. 1.

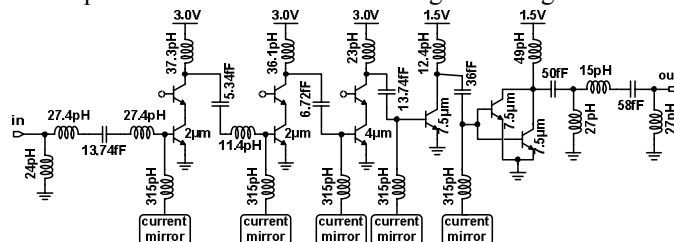


Fig. 2. 160-to-180 GHz amplifier schematic.

Scaling this amplifier in frequency from 140 GHz to 170 GHz was accomplished by adjusting component values and reducing inductive, resistive, and capacitive layout

parasitics. To tune all the resonant load circuits in all amplifier stages to 170 GHz, capacitors with values smaller than 30 fF are required. Since such small MiM capacitor values were not available in the design kit, custom Metal-Oxide-Metal capacitors were designed using ASITIC. Fig. 3 illustrates the 3-D capacitor structure and the 2π model which was used in circuit simulations. The 2π equivalent circuit was derived from the simple- π circuit employing a procedure similar to that described in [4]. To minimize their inductance and the die area of the amplifier, all capacitors have a short aspect ratio, instead of the square layout typical of MiM capacitors.

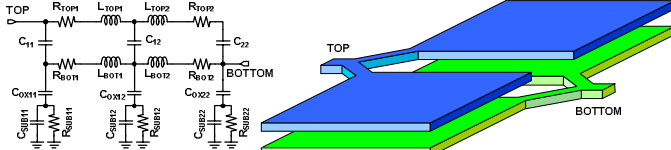


Fig. 3. Custom capacitor layout geometry (right, not to scale) and the corresponding 2π equivalent circuit (left).

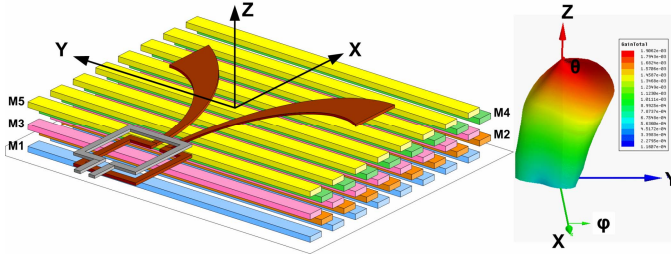


Fig. 4. 3-D view of the dipole antenna with metal fill (left, not to scale). HFFS-simulated radiation pattern of the antenna without metal fill (right).

IV. ANTENNA DESIGN

In an effort to explore the merits of integrating 170-GHz antennas on chip, three different antennas were designed using HFSS with the goal of minimizing area without sacrificing gain. The first is a patch antenna, realized in the 6th copper layer of the technology, and is used as a reference for size ($475\mu\text{m} \times 450\mu\text{m}$) and gain (-8 dBi in simulations). The second design is a tapered dipole antenna with increased gain and smaller size. Neither of these two designs satisfies the metal density rules of the 130-nm SiGe BiCMOS process and therefore cannot be integrated in a real product. A second dipole-antenna design was then derived from the first by inserting a floating metal-strip pattern under the antenna, similar to a slow-wave t-line [5]. A detailed drawing of the third antenna with metal fill is shown in Fig. 4. The staggered floating metal strips in metals 1 through 5 reduce the dielectric height above the silicon substrate and increase the effective permittivity, thus dramatically reducing the antenna size required for operation at 170 GHz. The small size of this antenna and the floating metal under it, ensure its full compliance with the metal-density rules of any modern nanoscale CMOS or SiGe BiCMOS process.

V. FABRICATION AND TEST PROCEDURE

The transceiver with and without antennas, and breakouts of the three different antennas and of the amplifier were fabricated in a SiGe HBT technology [6] with f_T of 270 GHz and f_{MAX} of 340 GHz. The measured f_T and f_{MAX} are plotted in Fig. 5 at 25°C and 125°C. The process features 6 copper layers and an aluminum cap layer used for pad openings, MiM capacitors, and poly resistors. The top Cu layer is 0.9- μm thick and 4.5 μm above the silicon substrate. SiO₂ is employed as the inter-metal dielectric. Die photos of the transceiver, amplifier breakout, and antenna breakouts are shown in Figs. 6-8.

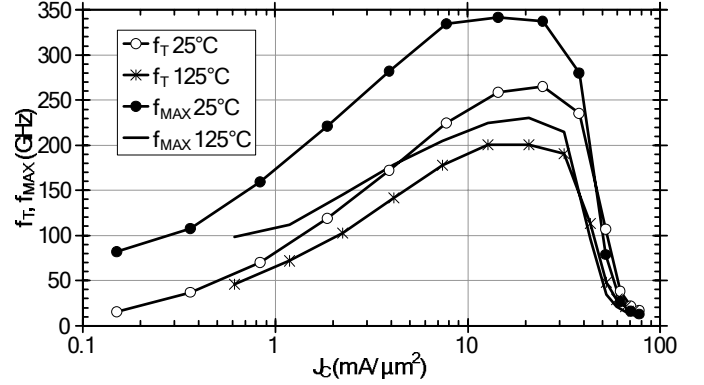


Fig. 5. Measured f_T and f_{MAX} vs. current density and temperature for an HBT with an effective emitter size of $0.11\mu\text{m} \times 5.55\mu\text{m}$.

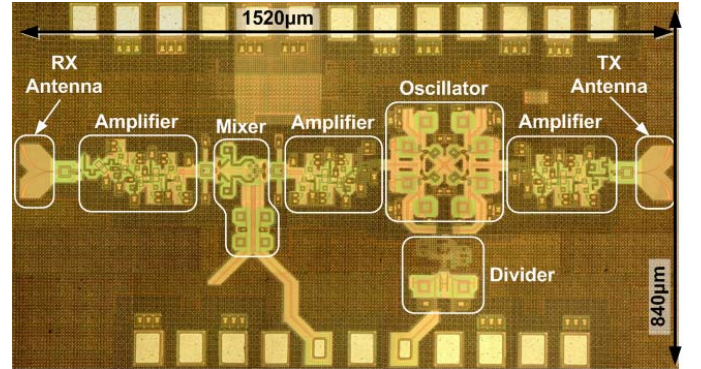


Fig. 6. Die photo of the transceiver with integrated antennas.

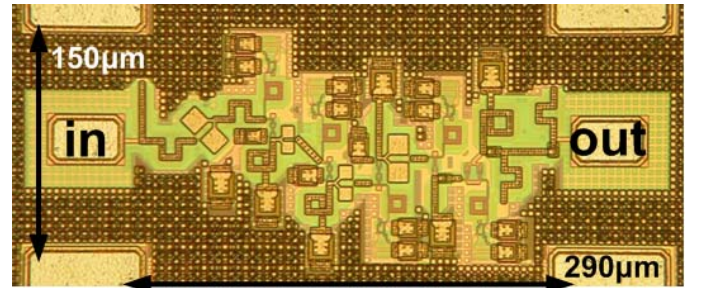


Fig. 7. Die photo of the 160-to-180 GHz amplifier breakout.

All circuits and the antennas were measured on wafer, in a D-band waveguide setup. The RF input signal was generated using an Oleson multiplier. Output signals in the D-band were measured with an external down-convert mixer and an Agilent

PSA, or with an Elva D-band power sensor. The antenna radiation pattern was estimated by applying a signal to the input pad of each antenna test-structure and employing a suspended 110-to-170 GHz Cascade Microtech GSG probe to measure the radiated power. All setup losses were de-embedded from the measurements. Where applicable (amplifier and transceiver without antennas), the pad capacitance was not de-embedded.

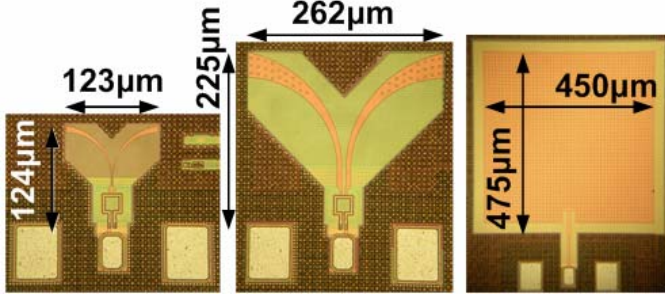


Fig. 8. On-chip antenna test-structures. Left: dipole with fill; center: dipole without metal fill; right: patch antenna (not to scale).

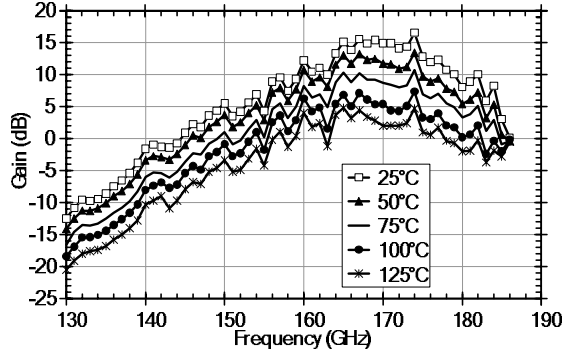


Fig. 9. Measured amplifier gain vs. frequency over temperature.

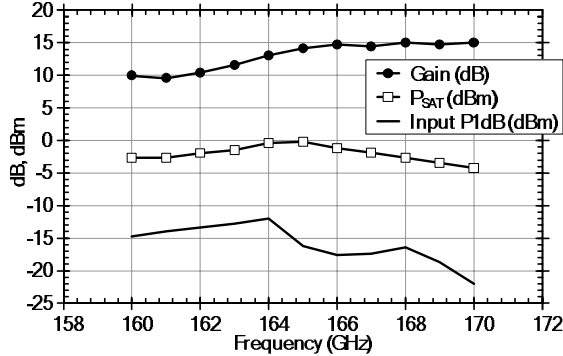


Fig. 10. Measured gain, saturated output power, and input P_{1dB} of the amplifier at 25°C.

V. MEASUREMENT RESULTS

A. 160-GHz to 180-GHz Amplifier

Fig. 9 shows the amplifier gain measured over temperature up to 125°C. It is higher than 15 dB from 166 GHz to 174 GHz and the 3-dB bandwidth exceeds 10 GHz. Fig. 10 summarizes the amplifier linearity measurements in the 160-to-170GHz range at 25°C. The maximum output power of 0 dBm occurs at 164 to 165 GHz and the best input P_{1dB} is

-12 dBm at 164 GHz. The amplifier DC power consumption is 135 mW.

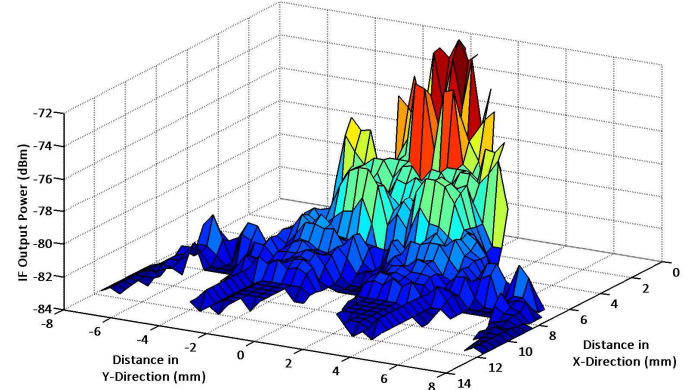


Fig. 11. Antenna pattern measured directly above the receiver.

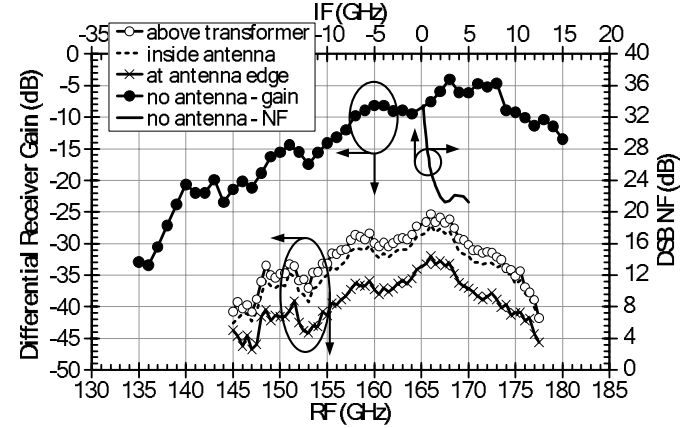


Fig. 12. Measured conversion gain of the receiver with and without antenna, and measured DSB NF of the receiver without antenna.

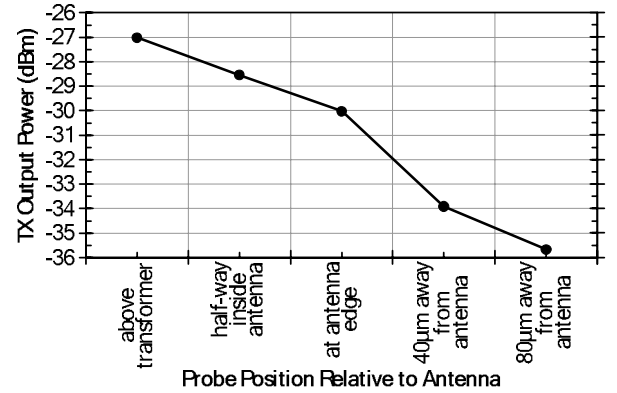


Fig. 13. Output power of the transmitter with antenna, measured at 5 different locations near the antenna.

B. 170-GHz Transceiver

The receiver antenna pattern of Fig. 11 was measured on the transceiver with on-die antennas using a probe suspended near the receiver antenna. The on-chip oscillator signal is at 165.3 GHz and the 162.6-GHz RF signal is applied through a GSG probe placed above the receive antenna. The receiver gain is compared in Fig. 12 with that measured on an identical receiver without on-die antennas. The DSB noise figure of the receiver with pads is 21 dB. Fig. 13 shows the transmitter

output power at 165.3 GHz, measured on the transceiver with antennas for several positions of the sensing probe above the transmitter antenna. For reference, the measured output power of the transmitter with pads is -5 dBm. The total DC power consumption of the transceiver, including three 170-GHz amplifiers, quadrature oscillator, mixer, and static frequency divider, is 800 mW.

C. 170-GHz Antennas

Antenna gain measurements are summarized in Fig. 14 versus frequency, and in Figs. 15-17 at 164 GHz. The plotted antenna radiation pattern is calculated by subtracting the setup losses from the power measured by the sensing probe above the antenna and includes propagation loss. These results demonstrate that, although all antennas have significant loss, the dipoles perform better than the patch. The dipole with metal fill shows comparable or better performance than the conventional dipole while occupying significantly less area and satisfying all metal density rules.

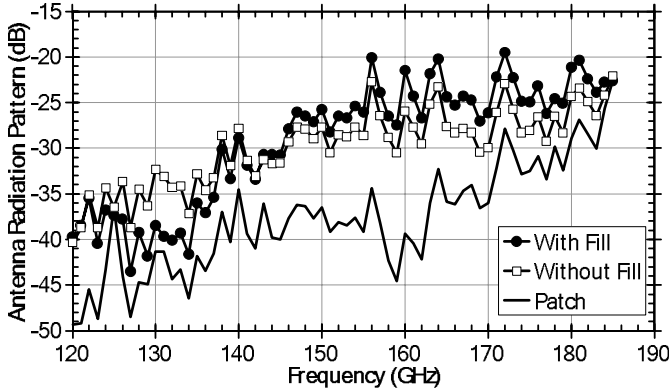


Fig. 14. Measured radiation pattern of the three antennas versus frequency.

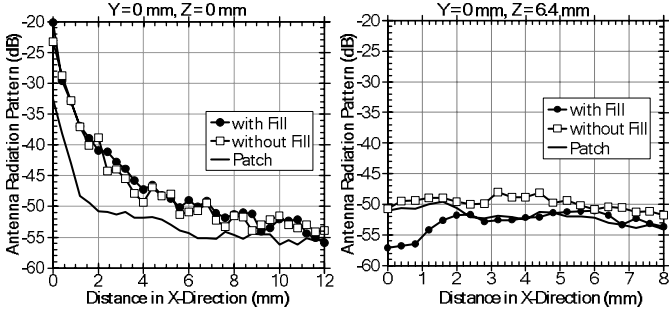


Fig. 15. Antenna radiation pattern at 164 GHz measured by moving the probe away from the antenna in the X-direction for Z=0mm (left) and Z=6.4 mm (right), Y=0mm in both cases.

VI. CONCLUSION

The first single-chip silicon transceiver with on-die transmit and receive antennas operating in the 160-GHz to 180-GHz range was demonstrated. Antenna test structure measurements indicate that a dipole design with floating metal strips has better performance than a patch antenna while satisfying the

stringent metal density rules of 130-nm CMOS and SiGe BiCMOS technologies. Nevertheless, the antenna loss remains unacceptably high, around 25 dB, indicating that a thick-metal, thick low-k dielectric BEOL and a low-k sealant may be needed to alleviate it.

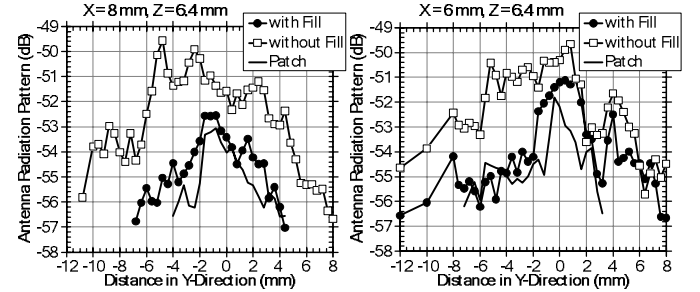


Fig. 16. Antenna radiation pattern at 164 GHz measured by moving the probe around the antenna in the Y-direction for X=8mm (left) and X=6mm (right), Z=6.4mm in both cases.

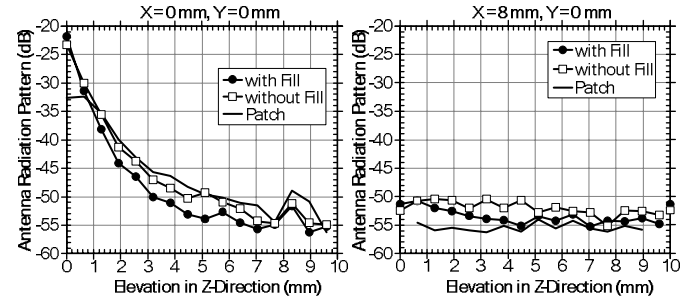


Fig. 17. Antenna radiation pattern at 164 GHz measured by moving the probe around the antenna in the Z-direction for X=0mm (left) and X=8mm (right), Y=0mm in both cases.

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