A Millimeter-Wave (40–45 GHz) 16-Element Phased-Array Transmitter in 0.18-μm SiGe BiCMOS Technology

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***Abstract*—This paper demonstrates a 16-element phased-array transmitter in a standard 0.18-μm SiGe BiCMOS technology for Q-band satellite applications. The transmitter array is based on the *All-RF* architecture with 4-bit RF phase shifters and a corporate-feed network. A 1:2 active divider and two 1:8 passive tee-junction dividers constitute the corporate-feed network, and three-dimensional shielded transmission-lines are used for the passive divider to minimize area. All signals are processed differentially inside the chip except for the input and output interfaces. The phased-array transmitter results in a 12.5 dB of average power gain per channel at 42.5 GHz with a 3-dB gain bandwidth of 39.9–45.6 GHz. The RMS gain variation is $<$ 1.3 dB and the RMS phase variation is $<$ 8.8° for all 4-bit phase states at 35–50 GHz. The measured input and output return losses are $<-$10 dB at 36.6–50 GHz, and $<-$10 dB at 37.6–50 GHz, respectively. The measured peak-to-peak group delay variation is $\pm$20 ps at 40–45 GHz. The output P_{-1dB} is -5 ± 1.5 dBm and the maximum saturated output power is -2.5 ± 1.5 dBm per channel at 42.5 GHz. The transmitter shows $<$ 1.8 dB of RMS gain mismatch and $<$ 7° of RMS phase mismatch between the 16 different channels over all phase states. A $-$30 dB worst-case port-to-port coupling is measured between adjacent channels at 30–50 GHz, and the measured RMS gain and phase disturbances due to the inter-channel coupling are $<$ 0.15 dB and $<$ 1°, respectively, at 35–50 GHz. All measurements are obtained without any on-chip calibration. The chip consumes 720 mA from a 5 V supply voltage and the chip size is 2.6 $\times$ 3.2 mm^2.**

***Index Terms*—BiCMOS analog integrated circuit, millimeter-wave, MIMO, phase shifter, phased-array, quadrature networks, radar, SiGe BiCMOS, smart antenna, wireless communication.**

I. Introduction

MILLIMETER-WAVE wireless communications have recently been gaining a lot of interest for high data-rate communication links [1], [2]. However, the indoor wireless propagation channel is challenging at high frequencies, $f > 30$ GHz, and for outdoor applications the atmospheric attenuation and rain absorption can be severe. These effects increase the channel noise temperature and limit the channel capacity [3], [4]. The phased-array technique is an attractive solution to compensate for these propagation impairments, since a highly directive antenna array improves the signal-to-noise ratio, hence channel capacity, significantly. The high antenna gain also enhances the spatial diversity since the phased-array filters the signal in the space-time domain and rejects an interferer from a different direction substantially [5].

In terms of scalability, phased-arrays based on the *All-RF* architecture and using RF phase shifters [6]–[8] have a simple system architecture and result in a relatively straightforward extension to large array implementations (32–10,000 elements). On the other hand, the mixer-based approach in [9] and [10], and the IF phase shifting scheme in [11] requires the same number of frequency conversion units as the number of array elements, requiring a complicated LO distribution network for large arrays.

This work demonstrates a Q-band (40–45 GHz) 16-element phased-array transmitter for satellite communications. The design is based on 4-bit RF active phase shifters and the chip is realized in 0.18-μm SiGe BiCMOS technology ($f_t = 150$ GHz). The signal frequency band is 43–45 GHz (bandwidth: 2 GHz, 4.5%), and is centered at the satellite communication frequency of 44 GHz. Fig. 1 illustrates the tile-based array construction, where the 16-element sub-array (called a "tile") is assembled into the array (called a "super-tile") in a layered configuration and thus making a 20 $\times$ 20 element array [12]–[14]. Each tile utilizes batch-fabricated three-dimensional silicon micromachining technology [15] to integrate 16 patch antennas, 16 InP power amplifiers and SiGe BiCMOS beamforming transmitter in a multi-layered single package. The layer-level integration allows for choosing optimum process technologies for each functional layer, resulting in a high performance system in terms of yield and cost. InP power amplifiers are required due to the high transmit power requirements per element (>30 dBm) [16]. To minimize transmission-line loss, low dielectric-constant BCB layers ($\epsilon_r = 2.7$, $\tan\delta = 0.002$) are chosen for interconnects and result in $\sim$ 0.4 dB/λ of attenuation at 44 GHz [17]. The maximum saturated output power required per element from the silicon beamformer is $-3 \sim 0$ dBm which is enough to drive the InP PA module.

There is a tradeoff between the scan range and bandwidth in large phased-arrays, which is detailed in Section II. The specific function blocks of the 16-element array transmitter are provided in Section III. Section IV addresses the design details of the transmitter, and finally the experimental results are presented in Section V.

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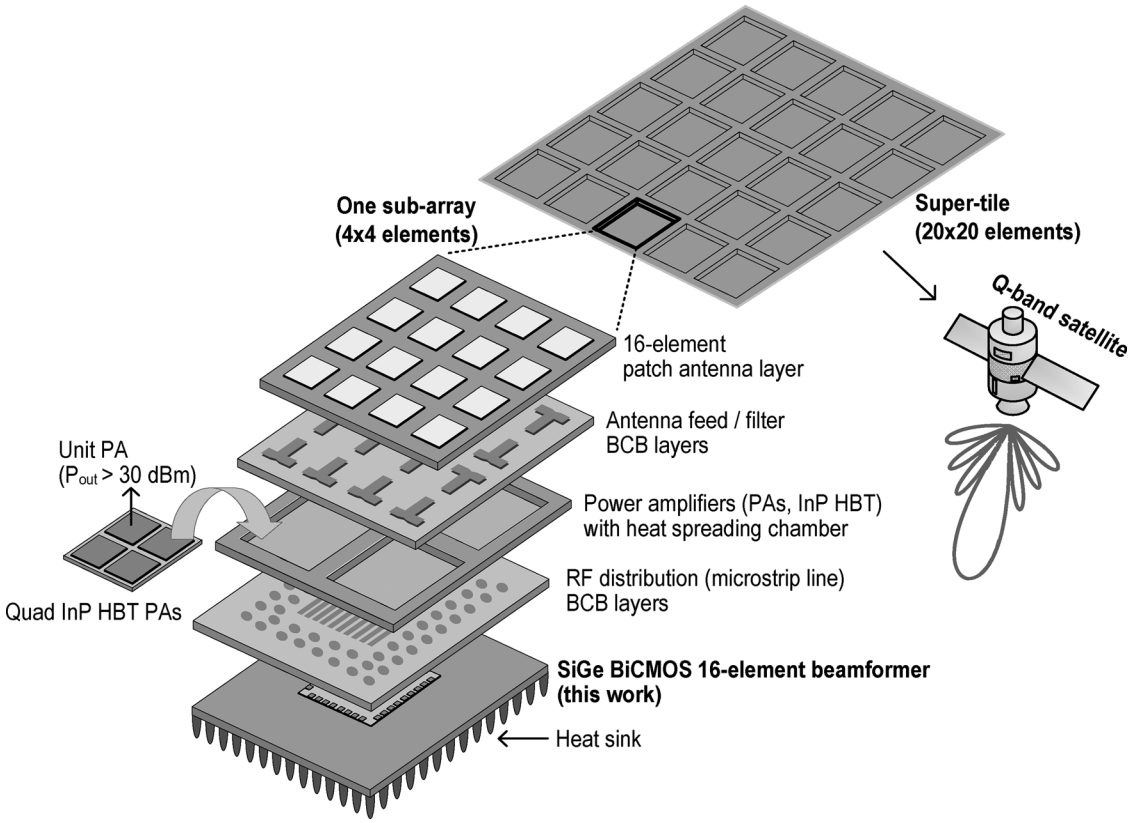

Fig. 1. A tile-based array architecture. One super-tile is composed of 5 × 5 tiles (sub-arrays) and each tile contains 16 elements (4 × 4). Multi-layer integration allows the optimization of each layer in terms of thermal, mechanical and electrical performances.

II. Bandwidth Limitations in Large On-Chip Phased-Arrays (Revisited)

Consider the 16-element phased-array shown in Fig. 2, with an inter-element spacing of $\mathrm{d} = 0.5\ \lambda_o$ at the center frequency (f_o). $\lambda_o\ (= c/f_o, c =$ light speed) is the signal wavelength, and θ_o is the beam steering angle. The input signal V_s, given in (1), has a finite frequency allocation of $f_o \pm \Delta f$ (bandwidth, $f_{\mathrm{BW}} = 2\ \Delta f$), and the phase delay $\Delta\phi_n$ per element is given in (2):

$$V_s = \mathrm{A}\sin 2\pi(f_o + \Delta f)t = \mathrm{A}\sin 2\pi f_o\left(1 + \frac{\Delta f}{f_o}\right)t \quad (1)$$

$$\Delta\phi_n = n2\pi f_o\left(1 + \frac{\Delta f}{f_o}\right)\Delta\tau = nkd\sin\theta_o\left(1 + \frac{\Delta f}{f_o}\right) \quad (2)$$

where $n = 0, 1, 2, \ldots, N-1$ ($N = 16$, total number of array elements), $k = 2\pi/\lambda_o$, and $\Delta\tau = d\sin\theta_o/c$ is the time-delay difference between two adjacent elements. The phase distribution $(\Delta\phi_0, \Delta\phi_1, \ldots, \Delta\phi_{N-1})$ must be linear over the entire array both in frequency and in space domain to ensure perfect true-time-delay (TTD) operation of the phased-array. This guarantees that the output signals from all the array elements are in phase (or congruent in time) in the θ_o direction [18]–[20]. However, due to on-chip area limitation, the phase shift is not only constant versus frequency but also covers only 0–360° [7], [8]. The phase shifting value per element is therefore chosen at f_o and is given in (3). This results in a phase quantization error, $\Delta\phi_{\mathrm{error},n}$ which is expressed as (4), at $f_o \pm \Delta f$ across the array.

$$\Delta\phi_{o,n} = \left|nkd\sin\theta_o - \mathrm{modulus}(2\pi)\right|. \quad (3)$$

$$\begin{aligned}\Delta\phi_{\mathrm{error},n} &= \left|\Delta\phi_n - \Delta\phi_{o,n}\right| \\ &= \left|nkd\sin\theta_o\frac{\Delta f}{f_o} - \mathrm{modulus}(2\pi)\right|. \end{aligned} \quad (4)$$

The $\Delta\phi_{\mathrm{error},n}$ causes a beam pointing error versus frequency, θ_{error} in Fig. 2, where the beam points in slightly different directions at different frequencies (see [20] for more details). References [12] and [21] suggest that the θ_{error} should be less than half of the 3-dB beamwidth, and this results in the maximum allowable bandwidth for a given array size as expressed in (5) where Nd is the total length (L) of the array:

$$\frac{f_{\mathrm{BW}}}{f_o} \le 0.886\frac{\lambda_o}{Nd\sin\theta_o}. \quad (5)$$

It is seen that if the array does not scan $(\theta_0 = 0°)$, then an infinite bandwidth can be tolerated. However, for a phased-array with a length L and θ_0 scan angle, the 3-dB bandwidth is proportional to $1/(L\sin\theta_o)$ for constant 0–360° phase shifters.

Fig. 3 presents the array factor for a uniformly-fed linear 16-element array scanned to $\theta_o = 45°$ ($\Delta\phi_{o,n} = n\pi\sin\theta_o \approx n \times 127.3°$) and a fractional bandwidth (f_{BW}/f_o) of 2.5%, 5%, 10%, and 20% [18]. The beams are squinted especially at the upper and lower bandwidth frequencies ($f_{\min}$ and $f_{\max}$) due to the non-optimal phase delays: for example, for a 10% fractional bandwidth system, the main beam from the 16-element array is diverted by $\theta_{\mathrm{error}} \approx \pm 3°$ from 45° at the band edges, and results in 1.13 dB of pattern loss at the 45° scan angle for $f_{\min}$ and $f_{\max}$. The f_{BW} is proportional to 1/N, and an 8- or 4-element array can tolerate 2 or 4 times larger bandwidth than

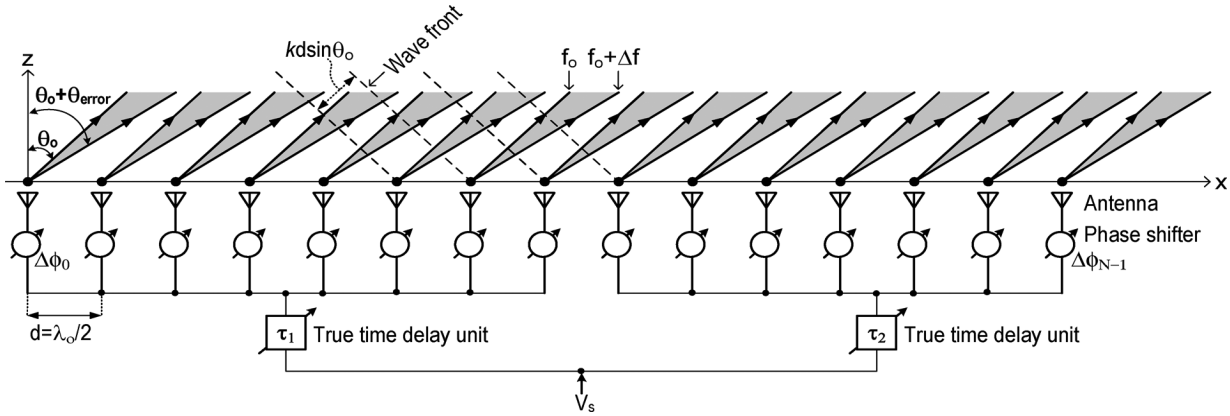

Fig. 2. 16-element phased-array with a combination of phase shifters at the element level and true time delay (TTD) units at the sub-array level for wideband operation ($N = 16$).

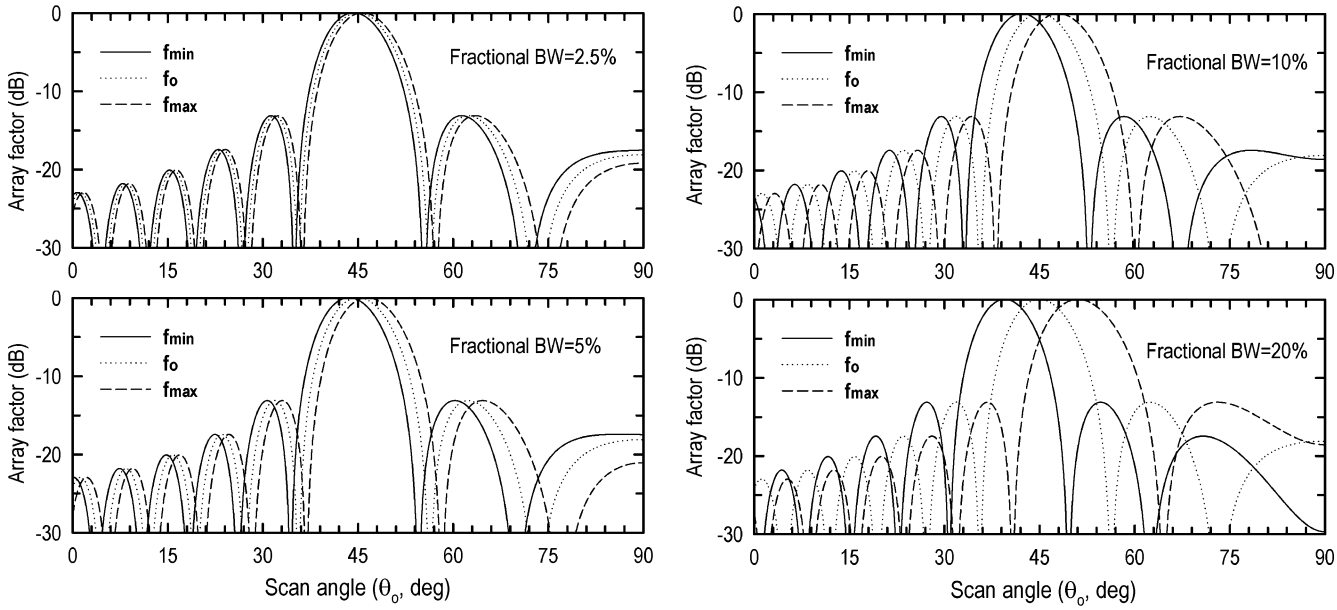

Fig. 3. Array factors for a 16-element linear phased-array for different fractional bandwidths (scan angle $= 45°$).

a 16-element array. Therefore, one can conclude from Fig. 3 that on-chip phased-arrays with 0–360° phase shifters can drive 4×4 or even 8×8 elements with virtually no penalty for a system with up to 10% bandwidth.

As a final note, TTD units are imperative at the sub-array level to cover more than 10% bandwidth for 8×8 arrays (Fig. 2). In this case, the TTD units must result in a phase difference of $8 \times \Delta\phi$ (center-to-center at the 8-element level, $\Delta\phi =$ phase difference between adjacent elements). These TTD units are based on switched transmission lines in low dielectric constant substrates and are quite large due to the large required phase shift [22]. However, only one of them is needed for every 8×8 elements [19].

III. 16-Element Phased-Array Transmitter Architecture

Fig. 4 presents the functional blocks of the 16-element phased-array transmitter based on the corporate-feed approach with active RF phase shifters. The RF input signal is transformed into a balanced signal using an active balun, and the input and output of the balun amplifier are matched to 50 Ω with inductive transmission line stubs [23]. The 1:16 signal divider constitutes the core part of the corporate-feed network, and is realized using a combination of active (1:2) and passive (1:8) designs for a compromise between loss, linearity and power consumption. To minimize area, the 1:8 passive dividers are realized with shielded differential transmission lines (similar to a coaxial line configuration) which are detailed in the next section.

After the dividers, each array element is composed of a loss-compensation amplifier (LCA), a 4-bit phase shifter and a 50-Ω driver. The LCA compensates for the 9 dB of power division loss from the 1:8 passive divider and drives an I/Q network inside the phase shifter. The active phase shifter is based on a phase interpolation technique where differential I/Q signals are added with appropriate weights to generate necessary phase, and a DAC controls the amplitude weights for 4-bit phase quantization [7]. The phase shifters are controlled independently using 4-bit digital data input from an array decoder. The array decoder is composed of a 4-to-16 address decoder and 4-bit register cells ($\times 16$) are used to access each array element [8]. Finally, a 50-Ω driver converts the differential signal into a single-ended one

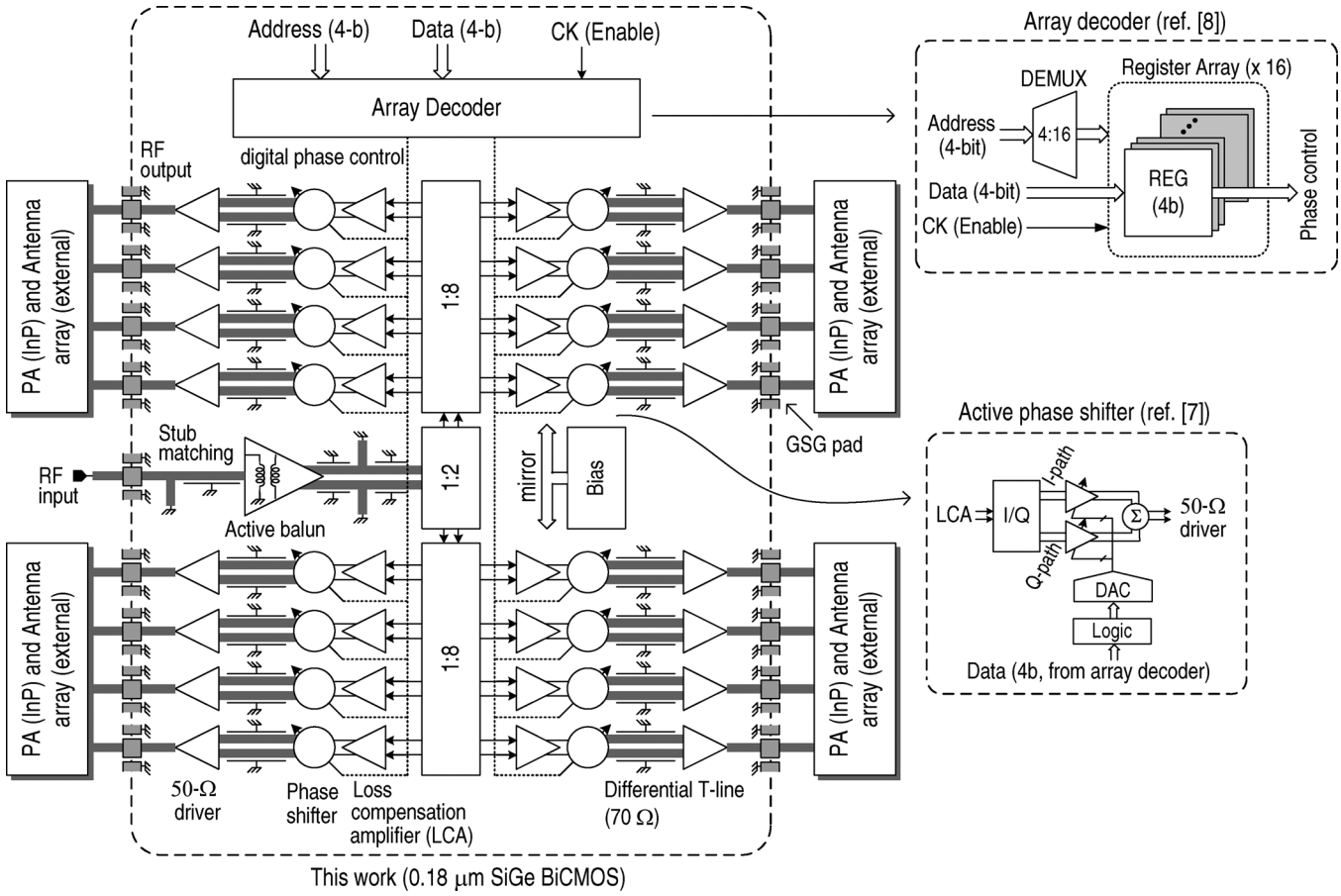

Fig. 4. The functional block of the 16-element phased-array beamformer in 0.18-μm SiGe BiCMOS technology.

and drives the transmission lines in the BCB layer with wide-band 50-Ω matching (see Fig. 1). The transmitter chip is followed by high-efficiency external InP PAs and microstrip antennas built using interconnection BCB layers.

IV. Functional Block Design

A. Active Balun Amplifier

A differential system is more robust to parasitic coupling than a single-ended one for high frequency applications. In this design, the balun function is realized using a standard differential amplifier with emitter coupling by grounding one of the differential inputs (Fig. 5). At millimeter-wave frequencies (>30 GHz), a small parasitic layout inductance can cause a moderate reactive impedance. For instance, when a line length, l, is much shorter than the wave length, λ, the line inductance can be approximated by (6) where Z_o is the characteristic impedance of the line. Typical values of $Z_o = 100\ \Omega$ and $l = 100\ \mu$m ($\approx \lambda/42$ at 44 GHz, $SiO_2\ \epsilon_r = 4.2$) results in $L \approx$ 68 pH corresponding to $j19\Omega$ at 44 GHz, which is comparable to the $1/g_m$ of an HBT biased at >1 mA. When present at the emitter side, this parasitic reactance lowers the gain and increases linearity a bit.

$$L = \frac{Z_o \tan(\beta l)}{\omega} \approx \frac{Z_o \beta l}{\omega} = \frac{Z_o \sqrt{\varepsilon_r}}{c} l, \quad \text{where } \beta = \frac{2\pi}{\lambda}. \quad (6)$$

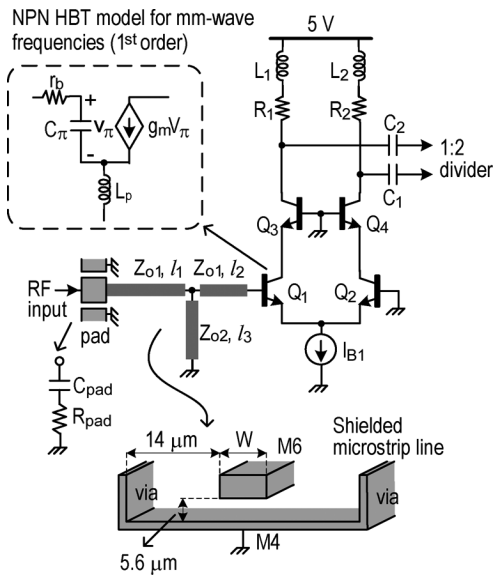

Fig. 5. The active balun amplifier, microstrip line structure (not to scale) and small signal NPN HBT model which includes an inductance, L_p, to account for parasitic layout inductance for this work.

To account for the parasitic layout inductance, the first-order small-signal model includes an inductor, L_p in Fig. 5, and this inductance is extracted from full-wave electromagnetic (EM) simulations using Sonnet [24].

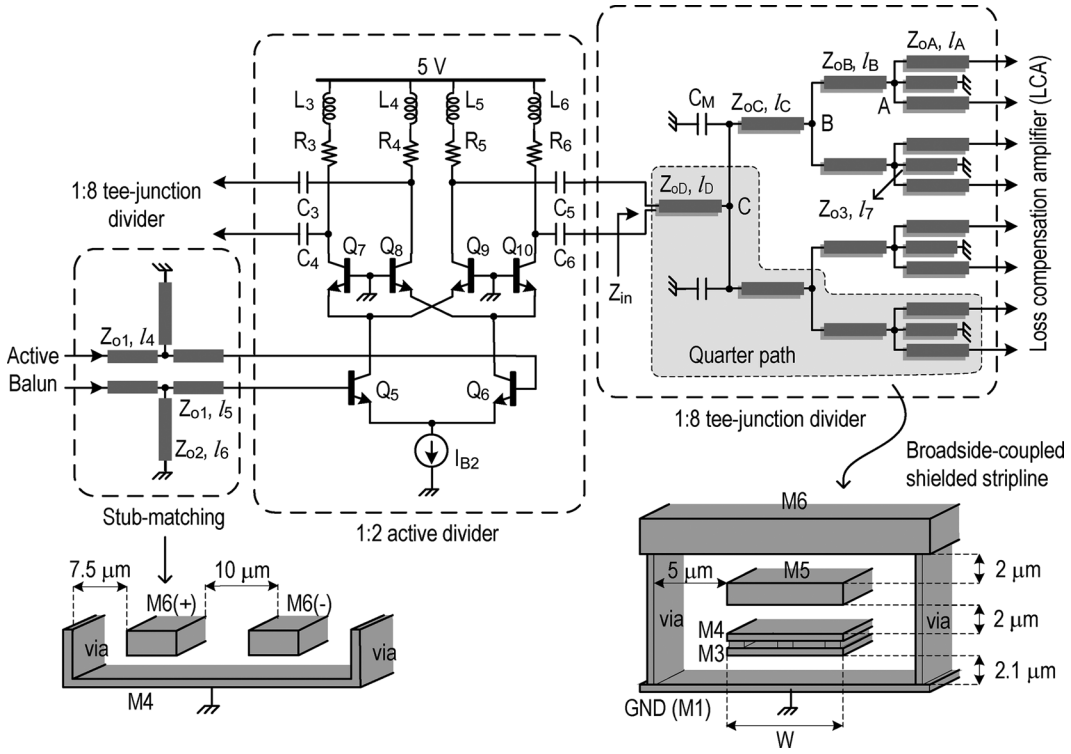

Fig. 6. The 1:2 active divider, differential microstrip line structure (not to scale), 1:8 passive tee-junction dividers (only one is shown) and broadside-coupled stripline structure (scaled, M5 thickness: 1.6 μm, thickness of M4 and M3 with vias: 1.9 μm).

The input port is matched to 50 Ω at 39–60 GHz ($S_{11} < -10$ dB) using short transmission lines ($Z_{o1} = 50\ \Omega$, $l_1 = 390\ \mu$m and $l_2 = 230\ \mu$m) and a grounded inductive matching stub ($Z_{o2} = 75\ \Omega$, $l_3 = 380\ \mu$m, $L_{\text{eff}} = 190$ pH, Q = 13.2 @ 45 GHz). The transmission lines and inductive stubs are realized using shielded microstrip-mode lines. Typical line widths, W in Fig. 5, are 8 μm and 4 μm for the 50 Ω and 75 Ω lines, respectively. The input transistors ($Q_{1,2}$) are biased with 2.5 mA ($I_{B1} = 5$ mA) to achieve a peak f_t of 150 GHz. The emitter lengths (l_E) of $Q_{1,2}$ and $Q_{3,4}$ are 5.1 μm and 3.4 μm, respectively (emitter width $= 0.2\ \mu$m). The output is matched to 100 Ω differentially with $L_{1,2} = 200$ pH (Q = 16 @ 45 GHz) and $C_{1,2} = 33.6$ fF, and $R_{1,2} = 25\ \Omega$ of series resistance is used for lowering Q and extending gain bandwidth. All the RF pads are modeled as S-parameters using EM simulation (nominal model: $C_{\text{pad}} = 30.8$ fF and $R_{\text{pad}} = 260\ \Omega$). The voltage gain from the single-ended input to the differential output is 6 dB at 45 GHz and the 3-dB gain bandwidth is 30–57 GHz in SPECTRE simulation. The simulated differential gain mismatch is 2 dB and the phase imbalance is 2.7–4.4° at 40–50 GHz.

B. Corporate-Feed Network

Fig. 6 presents details of the 1:16 signal feed network composed of a 1:2 active divider and two 1:8 passive tee-junction dividers.

Active 1:2 Divider: The active divider provides additional common-mode rejection, correcting the differential errors from the active balun. The RF input signal is divided into two in the current domain at the cascode nodes (l_E of $Q_{7-10} = 3.4\ \mu$m). The input of $Q_{5,6}$ ($l_E = 10.7\ \mu$m) is matched to differential 100 Ω using shielded microstrip-mode differential transmission lines ($l_4 = 300\ \mu$m and $l_5 = 98\ \mu$m) and inductive stubs ($l_6 = 300\ \mu$m, $L_{\text{eff}} = 145$ pH, Q = 14.1 @ 45 GHz). Typical line width for the differential line is 7 μm for a differential mode 50 Ω. To simplify the design of the passive dividers, the output of the active divider is also matched to 100 Ω differentially with $L_{3-6} = 200$ pH (Q = 16 @ 45 GHz) and $C_{3-6} = 29$ fF. A $R_{3-6} = 15\ \Omega$ increases the match bandwidth. The voltage gain of the active divider is 12 dB at 45 GHz for $I_{B2} = 15$ mA and the 3-dB gain bandwidth is 38.5–52.3 GHz. All the layout parasitics are extracted as S-parameters using Sonnet and included in the SPECTRE simulations.

Passive 1:8 Tee-Junction Dividers: The passive dividers in Fig. 6 utilizes the 3-dimensional metal stack structure to realize compact and tightly coupled differential transmission lines, called broadside-coupled shielded striplines (BCS-lines) [25], [26]. Theoretical analysis and measured performance of the BCS-lines are presented in [26]. The M5 thickness is 1.6 μm in the BCS-line structure in Fig. 6, and to minimize geometrical asymmetry, M3 and M4 are connected together with via resulting in an equivalent thickness of 1.9 μm. A distance of 5 μm between the signal lines and the shielding via was found to be adequate using EM simulations, resulting in a total BCS-line width of 15 μm (for W = 3 μm in Fig. 6) and this is much less horizontal space than typical coplanar waveguide (CPW) lines. The line impedance can be set by the line width W. Typical differential mode characteristic impedances are 42–64 Ω for W = 2–4 μm, and the measured loss is about 3–3.5 dB/0.5 mm for a 64 Ω line at 45 GHz and is due to finite ohmic resistance of the signal lines [26]. The fundamental merit of the BCS structure is that the shielded ground plane surrounding the

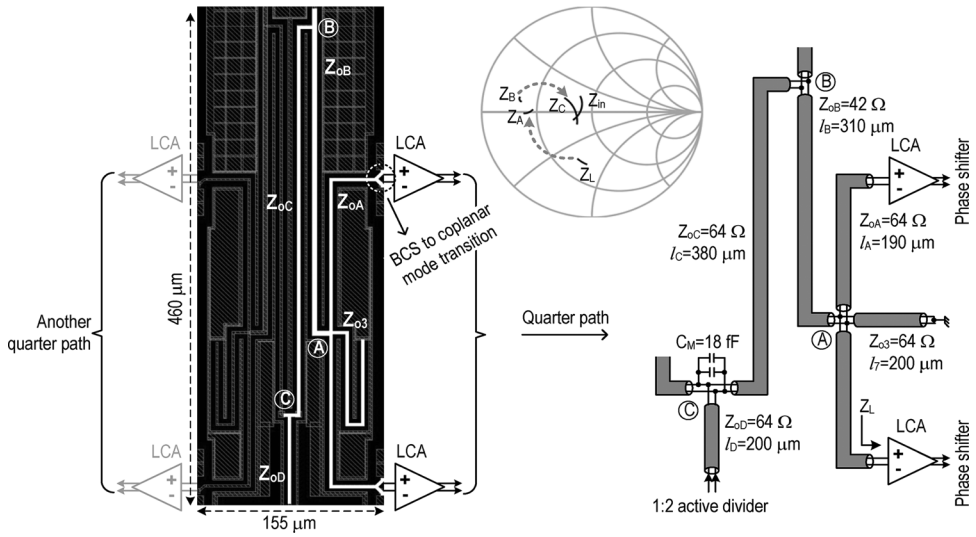

Fig. 7. The layout of the quarter path shown in Fig. 6 and its detailed description (all impedances are odd-mode impedances). The frequency range of the impedances in the Smith chart ($Z_o = 100\ \Omega$) is 40–50 GHz.

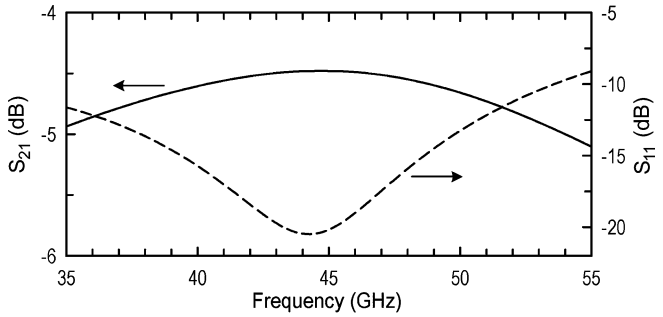

Fig. 8. The simulated S_{21} and input reflection coefficient (S_{11}) of the passive 1:8 tee-junction divider. Input port impedance $= 100\ \Omega$ and output load impedance $= 55 - j65\Omega$ at 45 GHz. The S_{21} does not include the 9 dB 1:8 splitter loss. (Port-1: input port, Port-2: one of the 8 output ports).

differential signal lines allows excellent line-to-line isolation in a very compact structure. This makes possible to integrate the 1:8 tee-junction divider in a small area (see Fig. 11).

The layout details of the passive divider are presented in Fig. 7 where only a quarter path is illustrated for simplicity. The Smith chart shows impedances at the junction points of the divider. The loading impedance (Z_L) from the LCA input is $Z_L = 55 - j65\Omega$ at 45 GHz. The capacitive reactance of Z_L is tuned out using a BCS-line ($Z_{oA} = 64\ \Omega$, $l_A = 190\ \mu$m) in parallel with an inductive stub ($L_{\text{eff}} = 260$ pH @ 45 GHz, $Z_{o3} = 64\ \Omega$, $l_7 = 200\ \mu$m). With two of these BCS-lines in parallel, the odd-mode characteristic impedances at node A is $Z_A \approx 40\,\Omega\,(Z_{oB} = 42\,\Omega, l_B = 310\,\mu\text{m})$. The impedance seen at node B, then, is $Z_B \approx 20\,\Omega$, and is matched to $Z_C \approx 71\ \Omega$ at node C using a BCS-line ($Z_{oC} = 64\,\Omega, l_C = 380\,\mu$m) followed by a shunt capacitor ($C_M = 18$ fF). After another BCS-line section of $Z_{oD} = 64\ \Omega$ and $l_D = 200\ \mu$m, the final input impedance is $Z_{\text{in}} = 83\,\Omega$ at 45 GHz and this results in less than -15 dB input return loss at 39–49 GHz for a $100\,\Omega$ source impedance (Fig. 8). The output return loss is ≤ -10 dB at 30–53 GHz for the load impedance of Z_L. The estimated power loss in the 1:8 passive divider is 4.5–4.8 dB per path above the ideal 9 dB power split loss at 40–50 GHz (Fig. 8). The entire passive 1:8 divider occupies an area of only 0.15×1.05 mm^2.

C. Array Element Design

Loss-Compensation Amplifier (LCA): The LCA compensates the power loss from the passive power dividers (Fig. 9). The inductively loaded common-emitter (CE) stage provides a peak voltage gain of 9 dB at 46 GHz with a DC current of $I_{B3} = 10$ mA (l_E of $Q_{11,12} = 8\ \mu$m and l_E of $Q_{13,14} = 5.3\ \mu$m), and the common-base (CB) stage contributes another 3 dB gain for $I_{B4} = I_{B5} = 2$ mA (l_E of $Q_{15,16} = 3.4\ \mu$m). A low impedance is better for stable operation under finite node parasitics at high frequencies. Therefore, the CE and CB interstage impedance is chosen to be $50\,\Omega$ (differentially $100\,\Omega$): $L_{7,8} = 200$ pH, $C_{7,8} = 33.6$ fF, $R_{7,8} = 12.5\ \Omega$, $C_{9,10} = 100$ fF, and $R_{9,10} = 12\ \Omega$. The size of the active inductor loads composed of $Q_{17,18}$ ($l_E = 3.4\ \mu$m) and $R_{11,12}$ (124Ω) are optimized to have a peak gain at around 40–41 GHz, resulting in a 36.5–49 GHz of 3-dB gain bandwidth in the gain stage.

The output LCA stage utilizes the totem-pole technique [27] and drives the quadrature all-pass filter (QAF) having an input impedance of $\sim 32\ \Omega$ (differential) [7]. When driving a low impedance load, a standard CE amplifier or emitter-follower usually suffers from the limited current sourcing or sinking to (and from) the load, resulting in signal nonlinearity. In the output driver, the transistors $Q_{19,20}$ ($l_E = 3.4\ \mu$m) and $Q_{21,22}$ ($l_E = 3.4\ \mu$m) operate in a push-pull manner and improve the current driving to the heavy load: i.e., when the Q_{21} pulls the load down by sinking current ΔI, Q_{19} also senses the input signal with opposite polarity and pulls another ΔI approximately from the load. As a consequence, the net current pulled from the load is doubled and so is the voltage gain. An $R_E = 25\ \Omega$ is chosen for better 3rd-order linearity. C_d (0.5 pF) and $C_{s1,2}$ (50 fF) are DC blocking capacitors and $C_{s1,2}$ also resonates out the parasitic active inductance caused by the emitter followers, $Q_{19,20}$. The output driver consumes

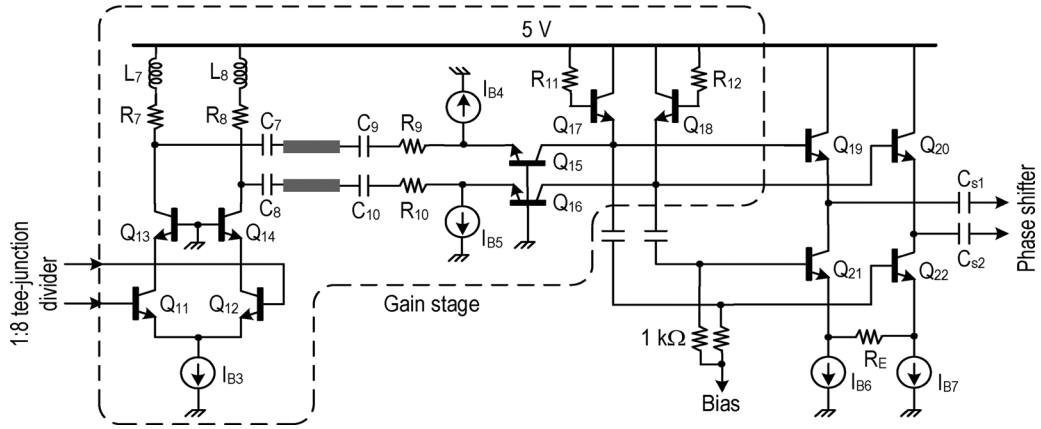

Fig. 9. The loss-compensation amplifier (LCA) composed of gain stage (common emitter and common base stage) and an output low-impedance driver for the following phase shifter.

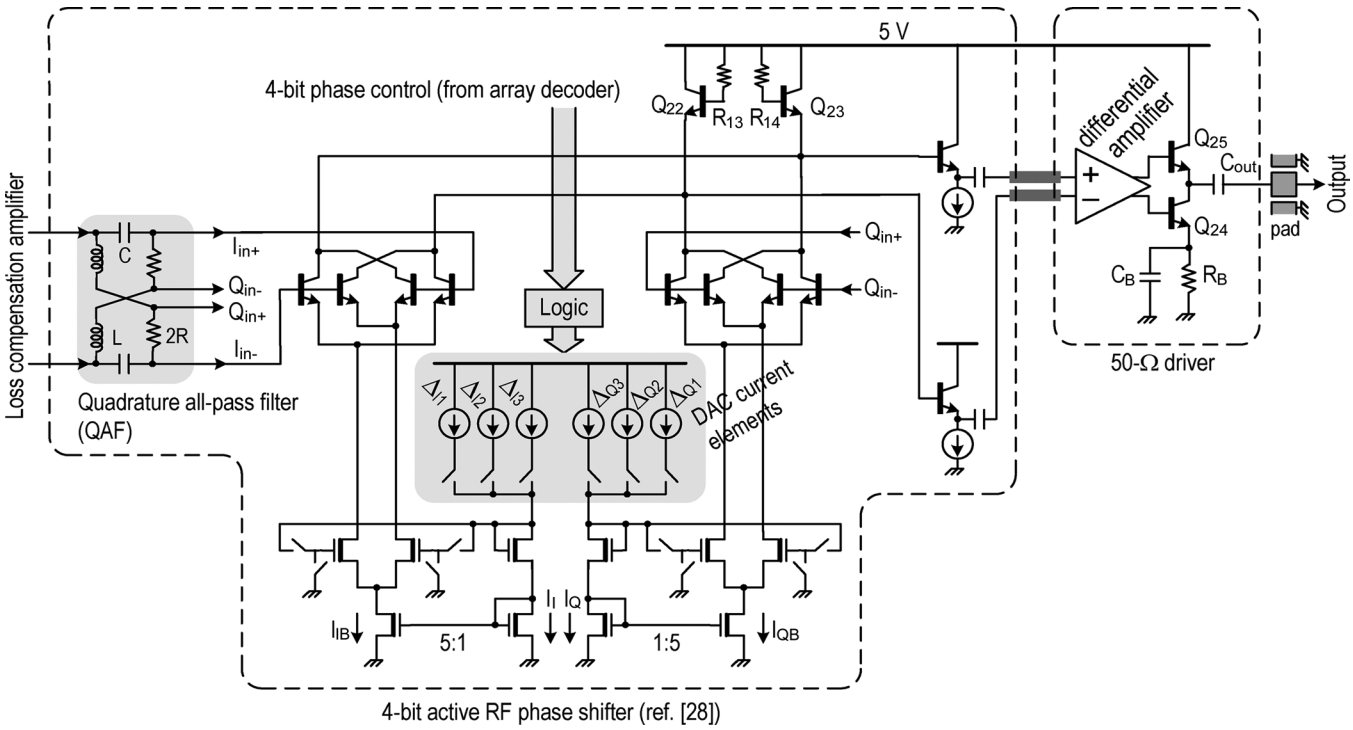

Fig. 10. The active 4-bit RF phase shifter and 50-Ω output driver.

6 mA of DC current ($I_{B6} = I_{B7} = 3$ mA) with unity voltage gain for a 32 Ω load.

Four-Bit Active Phase Shifter: The active phase shifter is realized in the same manner as in [7], [8], and [28] (Fig. 10). The I/Q phase accuracy of the QAF is important since it provides the reference quadrature phases for further fine phase quantization, while the I/Q amplitude mismatch can be offset by adjusting gain of the I/Q VGAs accordingly. A low impedance of $\sqrt{L/C} = 27\,\Omega$ is chosen for QAF to increase the I/Q phase accuracy under about 70 fF of loading capacitance ($\mathrm{L} = 93.4$ pH, $\mathrm{C} = 125.4$ fF, and $2\mathrm{R} = 62.5\,\Omega$), resulting in $\leq 5^{\circ}$ of I/Q phase error at 37–48 GHz in the QAF. Compared with the designs in [7] and [8], this design integrates two separate current-scaled DACs to control I_{IB} and I_{QB}, which enables to control the I- and Q-path gain independently so as to accommodate the I/Q amplitude mismatch in the QAF. Contrary to CMOS designs in [7] and [8], the base-emitter diffusion capacitance ($\mathrm{C_{diff}} \propto g_m \propto I_{\mathrm{bias}}$) of the input HBT transistors ($l_E = 3.4\ \mu$m) can be modulated when changing the bias current necessary for phase control, causing non-negligible phase errors at the design frequency [28]. Therefore, the sizes of DAC current sources (Δ_{I1-3} and Δ_{Q1-3}) are optimized using SPECTRE to achieve 4-bit phase accuracy with less than ±1.5 dB gain variations for all 4-bit phase states. The SPECTRE optimization effectively included all the error effects including I/Q amplitude and phase mismatches from the quadrature generator, base-emitter capacitance modulation effects in the vector summer, and was done over the target frequency bandwidth. The current consumption

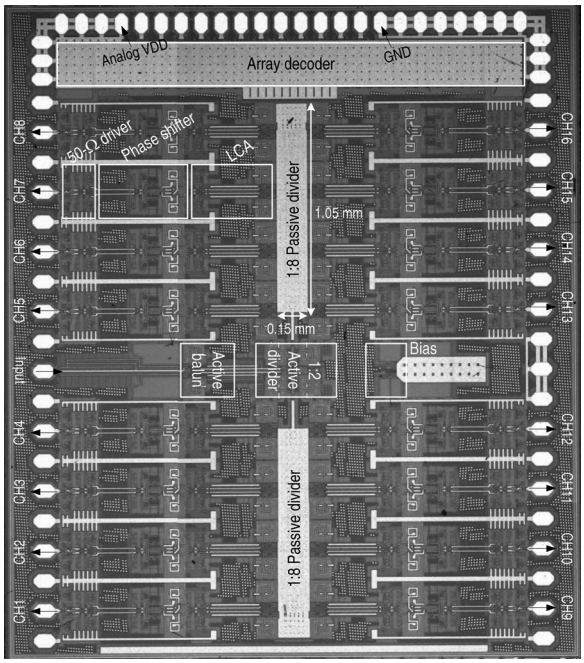

Fig. 11. Chip photograph of the 16-element Q-band phased-array transmitter (area $= 2.6 \times 3.2$ mm^2).

in the phase shifter including the buffer is 8 mA, and the size of the active inductor composed of $Q_{22,23}$ ($l_E = 3.4$ μm) and $R_{13,14}$ (125 Ω) is set to have a 2–3 dB voltage gain at 39–46 GHz.

50-Ω Driver: The 50-Ω driver in Fig. 10 compensates about 3 dB of line loss to the external InP PA. A standard differential amplifier with resistive emitter-degeneration is first used and provides 3–4 dB voltage gain at 39–53 GHz for a bias current of 10 mA [29]. The NPN-based push-pull output stage ($Q_{24,25}, l_E = 3.4$ μm) converts the differential input to a single-ended one and drives the external 50 Ω transmission line at the expense of 6 dB loss for impedance matching [8], [28]. A 3 mA of bias current sets the matching impedance and the output return loss is ≤ -10 dB @ 36–53.5 GHz in simulation including the pad parasitics. R_B (50 Ω) and C_B (100 fF) are used for biasing and AC bypassing, respectively. The output DC blocking capacitor ($C_{\text{out}} = 60$ fF) is also used for compensating a finite active inductance caused by Q_{25} at the design frequencies.

V. Measured Results and Discussion

The phased-array transmitter is realized in a 0.18 μm SiGe BiCMOS process (1P6M, SiGe HBT $f_t \approx 150$ GHz) and the chip microphotograph is shown in Fig. 11. The overall chip size is 2.6×3.2 mm^2. The electrical distances between the input port and all output channels are virtually identical due to the corporate-feed layout. A ground barrier (grounded via stack from substrate to top metal) is placed between channels to reduce parasitic substrate coupling among adjacent channels. The total current consumption is 720 mA from a 5 V supply voltage, and agrees well with simulation. Several DC pads are tied together for the supply and ground pads to satisfy the current density requirement. The DC current is divided as 5 mA for the active balun, 15 mA for the 1:2 active divider and 44 mA ($\times 16$) for each array element. The digital logic uses a 3.3 V of separate supply voltage. The transmitter was measured on-chip after a standard SOLT calibration to the probe tips using a vector signal network analyzer (Agilent, PNA-E8364B).

A. Single Channel Characterizations

Fig. 12 presents the measured S-parameters for all 4-bit phase states of a single path (*Channel-16*, address:1111) in the 16-element array. In this case, the outputs of all other channels are left open-circuited. The measured average power gain is 12.5 dB at 42.5 GHz and the 3-dB gain bandwidth is 39.9-45.6 GHz [Fig. 12(a)]. The discrepancy from simulations above 45 GHz could be due to the inaccurate HBT model at these frequencies together with process variations and errors in the parasitic estimation using EM simulations. The peak-to-peak gain variation for all 4-bit phase states is about 3 dB at 40–45 GHz, and the RMS gain variation (error) is < 1.3 dB up to 50 GHz. The measured input return loss is < -10 dB at 36.6–50 GHz, and output return loss is < -10 dB at 37.6–50 GHz. The isolation from output to input is below -55 dB at 30–50 GHz [Fig. 12(a)].

The 4-bit phase response is measured from 35–50 GHz using the digital control from the array decoder without any calibration, i.e., no DAC compensation is used [Fig. 12(b)]. The 0°-bit phase response is subtracted from all the measured 4-bit phase responses and the phase shifters show a constant wideband relative 4-bit phase states (Fig. 13). The measured RMS phase error from the ideal 4-bit phase states (with a reference to the measured 0°-bit phase) is $< 8.8°$ up to 50 GHz. The wideband characteristic is an inherent nature of the active phase shifter, since the phase interpolation technique is a linear process independent of the operating frequency, and the bandwidth is mainly limited by the I/Q network. The RMS phase error is much less than the 4-bit phase quantization level of 22.5°. The group delay is measured by a derivative of the measured phase responses and averaged by 5-point moving average with 100 MHz step [Fig. 12(b)]. The group delay is 150 ps at 44 GHz and its variation at 40–45 GHz is ± 20 ps.

The I/Q phase accuracy of the QAF is measured indirectly by comparing the phases of the 0°, 90°, and 270°-bit settings at the outputs. The I/Q phase error is $\leq 5°$ at 30–46.5 GHz (Fig. 14). The output $P_{-1\text{dB}}$, which is measured at the peak gain frequency of 42.5 GHz, is -5 ± 1.5 dBm and the maximum output power is -2.5 ± 1.5 dBm for all 4-bit phase states (Fig. 15). A $\mathbf{P}_{-1\text{dB}}$ analysis of the individual stage in the phased-array transmitter indicates that the output $\mathbf{P}_{-1\text{dB}}$ is limited by the current at the output stage.

B. Array Characterizations

Channel-to-Channel Mismatches: The output impedance matching of all the other channels is nearly identical to *Channel-16*. The gain and phase mismatches between the 16 different channels are measured by comparing the gain and phase response of the 0°, 22.5°, 45°, 67.5°, and 90°-bit S-parameters of all the 16 channels. Other phase settings follow similar mismatches. The measured raw RMS gain mismatch is ≤ 1.8 dB and the RMS phase mismatch is $\leq 7°$ at 40–50 GHz (Fig. 16). The transmitter array shows larger channel mismatches compared with the results in [8]. The

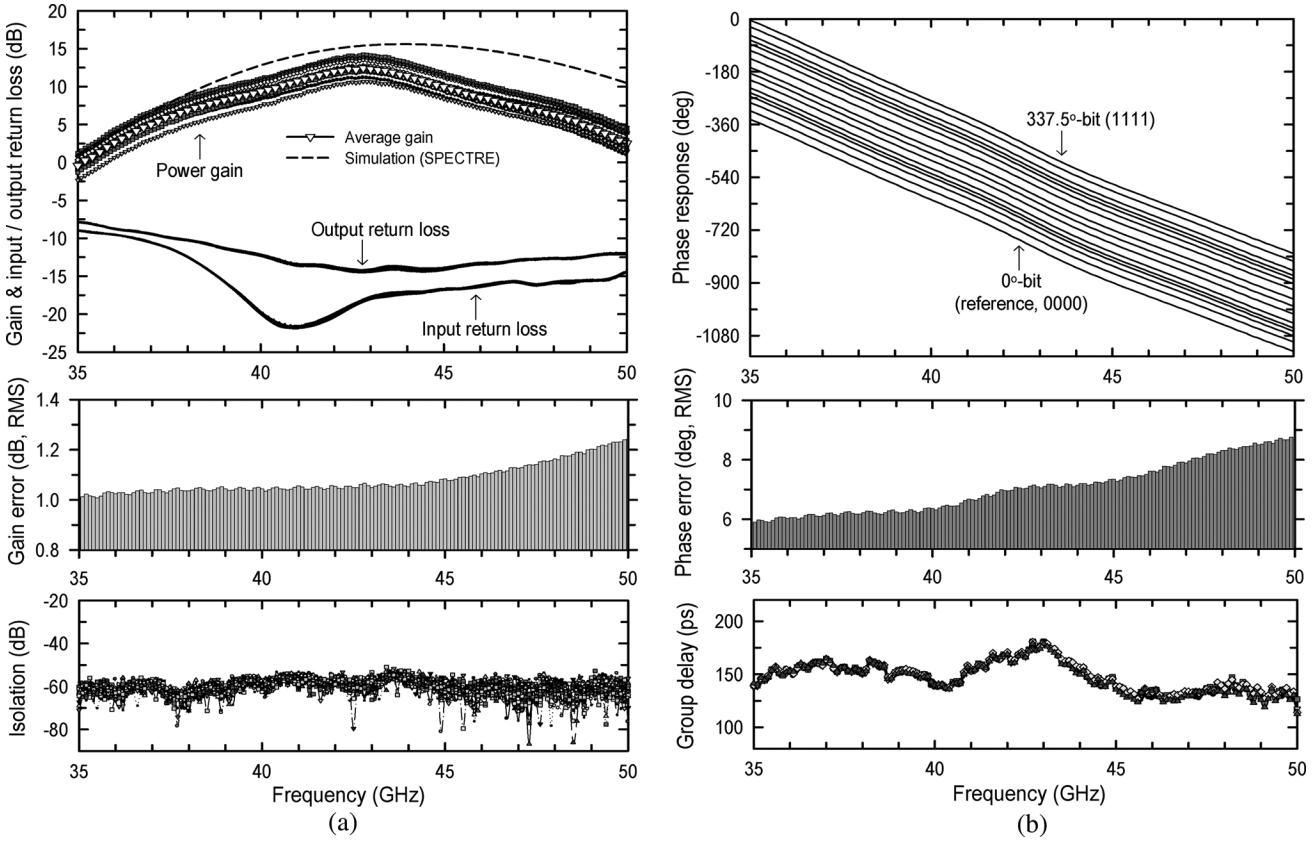

Fig. 12. The measured single channel (*Channel-16*) characteristics. (a) Input and output matching, power gain, RMS gain error and output-to-input isolation characteristics for all 4-bit phase states. (b) 4-bit phase responses, RMS phase error (from ideal 4-bit phases) and averaged group delays for 0°, 22.5°, 45°, 67.5°, and 90°-bit phase states.

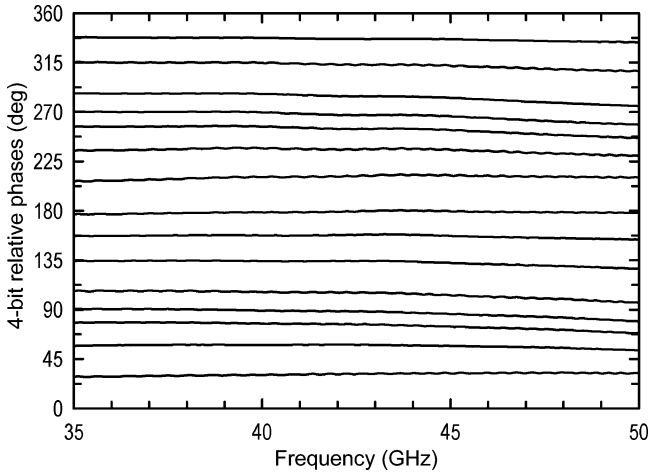

Fig. 13. The measured 4-bit relative phase states [reference: 0°-bit phase state in Fig. 12(b)].

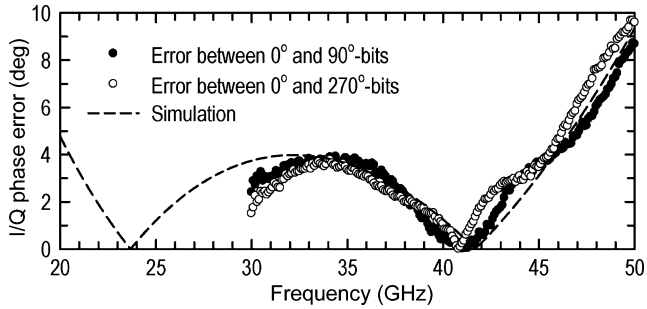

Fig. 14. The measured I/Q phase imbalance in the QAF.

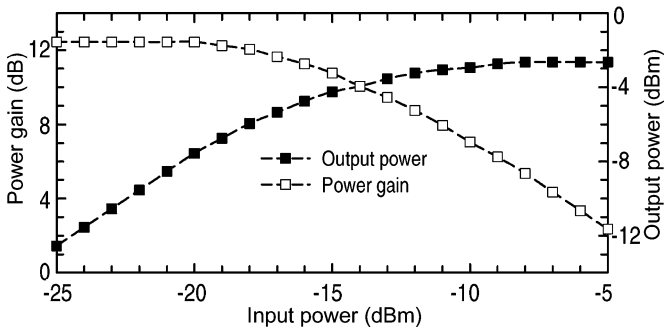

Fig. 15. The measured nominal power gain and output power per channel at 42.5 GHz versus RF input power.

reason is that a large bias current of 720 mA is supplied from the chip corner (Fig. 11, top, analog VDD pin), and there is a voltage drop across the array due to the distributed bias-line resistance inside the chip. This induces supply voltage and ground resistance variations between the different channels, and results in gain variations among the array elements. Actually, the measured power gains of Channel-8 and Channel-16 (upper parts of the chip in Fig. 11) are higher than those of Channel-1 and Channel-9 (lower parts of the chip in Fig. 11), due to the higher supply voltage and lower ground resistance in the upper parts of the transmitter array. The peak-to-peak

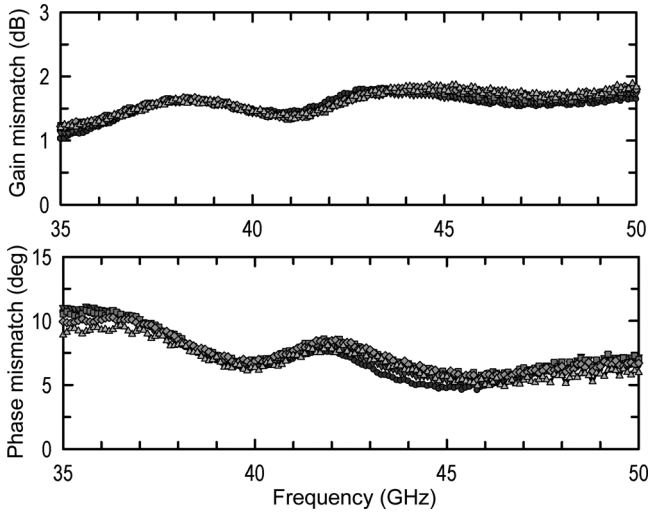

Fig. 16. The measured channel-to-channel RMS gain and phase mismatches between the 16 channels for 5 different phase states (0°, 22.5°, 45°, 67.5°, and 90°-bit phase states).

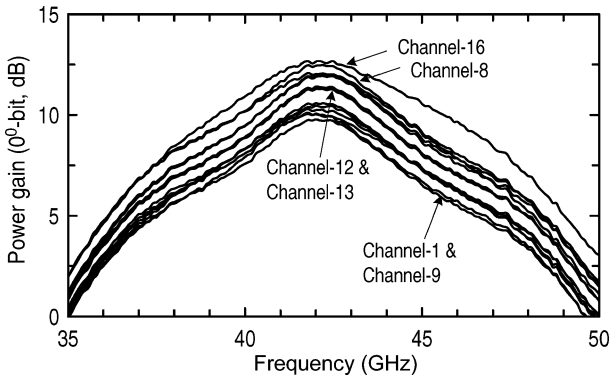

Fig. 17. Gain variation between different channels due to on-chip supply voltage and ground resistance variations (with 0°-bit phase setting).

amplitude variation among the channels is ~4 dB at 35–50 GHz (Fig. 17). It is worthwhile to mention that the measurement of the channel-to-channel mismatches include the mismatches in 1:8 passive dividers. The measured mismatches also include the systematic measurement uncertainties such as cable stability and CPW probe placement errors which could not be calibrated. It is observed that a ±0.3 dB error in the power gain S-parameter measurements depending on different probe placements.

Coupling between Channels: In integrated silicon phased-arrays, the substrate coupling between the channels is a major concern due to the conductive substrate [8], [28], [30]. Compared with an RF CMOS technology where the substrate resistivity (ρ) is 1–2 Ω/cm, the SiGe BiCMOS process provides a relatively high resistivity substrate with $\rho = 8$–10 Ω/cm. This, together with differential signaling and careful isolation consideration in the layout, helps reduce the coupling between channels. A worst case port-to-port coupling (isolation) of -30 dB is measured at 41–43 GHz between adjacent channels and the isolation between the other channel combinations is <-40 dB up to 50 GHz (Fig. 18). As detailed in [8] and [30], the parasitic coupling interactions between channels induce output signal errors.

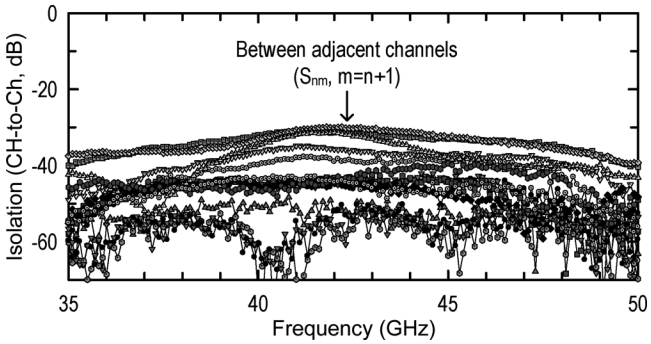

Fig. 18. The measured isolation between channel to channel. The worst case occurs between adjacent channels ($n = 1 - 15$).

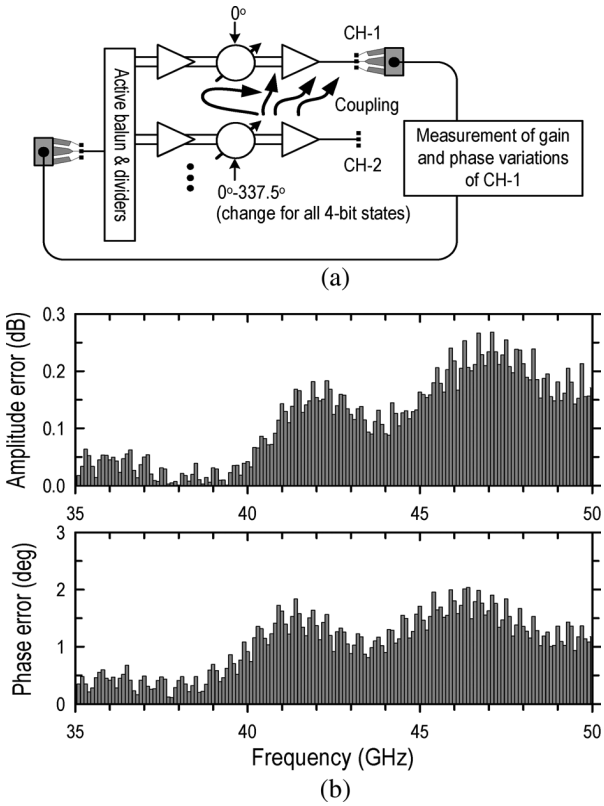

Fig. 19. Coupling characterization. (a) Coupling test setup. (b) The measured output signal errors (amplitude error and phase error).

To investigate the errors, *Channel-1* is set at the 0°-bit state and *Channel-2* is changed for all 4-bit phase states while measuring the gain and phase errors of the *Channel-1* at the same time [Fig. 19(a)]. The output port of *Channel-2* is left in open-circuit for a worst-case test condition [30]. The measured peak gain and phase error is < 0.3 dB and is $< 2°$ at 35–50 GHz, respectively [Fig. 19(b)].

Array Patterns: Fig. 20 presents two cases of synthesized beam patterns (with an assumption of standard linear array with isotropic radiators and $\lambda/2$ spacing between the elements) in ADS at 44 GHz using the measured 256 two-port S-parameters (16 channels × 16 S-parameters). In the ideal case, the phase on each element is changed continuously with an assumption of the same power gain of 11.5 dB for all of the 16 elements (11.5 dB

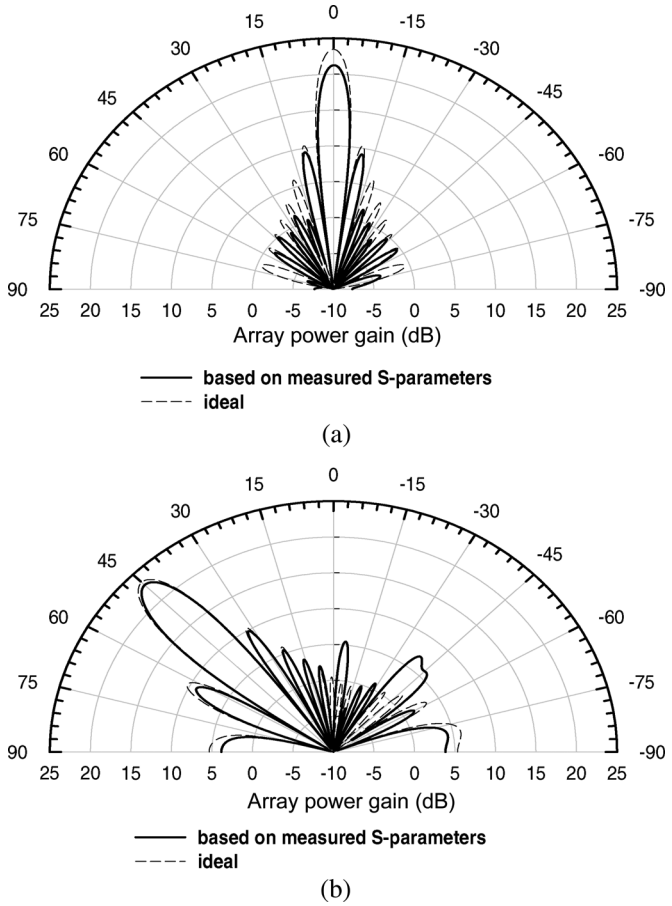

Fig. 20. Array beam scanning characteristics: (a) broadside scan, (b) 45° scan angle at 44 GHz.

is the measured average power gain at 44 GHz). In the measurement case the phase is digitized to the nearest measured 4-bit phase states and the corresponding measured amplitude is used. For broadside scanning [Fig. 20(a)], both results shows 6.4° of 3-dB beamwidth ($= \sin^{-1}(0.891 \times 2/N)$, $N = 16$) and 14.3° of first null-to-null bandwidth ($= 2 \times \sin^{-1}(2/N)$, $N = 16$). For the 45° scan [Fig. 20(b)], the sidelobes at -6° and -45° directions are a little bit larger than the ideal case due to the finite quantized phase states, but are still negligible compared with the main lobe power gain.

The measured results are summarized in Table I.

VI. Conclusion

A millimeter-wave phased-array transmitter is developed with 4-bit RF phase shifters for Q-band (40–45 GHz) satellite communication applications. The 16 array elements and the digital control units are integrated in a chip area of 2.6×3.2 mm^2, achieving the highest integration of mm-wave phased-array elements to-date. This high integration is due to the active phase shifter having very small size $(0.43 \times 0.27$ mm$^2)$ and the compact passive dividers based on the three-dimensional broadside-coupled transmission line. The proposed coaxial-type shielded transmission line structure allows dense integration of differential lines, and is an enabling technology for highly integrated millimeter-wave systems. The phase shifter shows

TABLE I
Summary of the Beamformer Performance

Technology	0.18μm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Frequency band	Q-Band (40-45 GHz)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	720 mA
Chip area	2.6x3.2 mm^2
Single Path Characteristics	
Input return loss	≤ -10 dB @ 36.6-50 GHz
Output return loss	≤ -10 dB @ 37.6-50 GHz
Channel power gain (*ave*)	12.5 dB @ 42.5 GHz (3-dB BW: 40-45 GHz)
Phase resolution	4-bit
Gain error	< 1.3 dB (RMS) @ 35-50 GHz
Phase error	< 8.8° (RMS) @ 35-50 GHz
Output P_{1dB}	-5±1.5 dBm @ 42.5 GHz
Maximum output power (P_{sat})	-2.5±1.5 dBm @ 42.5 GHz
Isolation (output-to-input)	≤ -55 dB @ 35-50 GHz
Array Characteristics	
Phase mismatch (RMS)	≤ 7° @ 40-50 GHz (between all channels)
Amplitude mismatch (RMS)	≤ 1.8 dB @ 40-50 GHz (between all channels)
Isolation (CH-to-CH)	≤ -30 dB @ 35-50 GHz
Array factor directivity	12 dB (16 elements)

$< 8.8^\circ$ of RMS phase error from the ideal 4-bit phase states at 35–50 GHz. The matching between the 16 different channels is very good: RMS gain variation is < 1.8 dB and RMS phase variation is $< 7^\circ$ at 35–50 GHz with no on-chip calibration. The parasitic coupling between the channels is negligible up to 50 GHz. The *All-RF* system architecture enables this design to be extended to 60 GHz or 77 GHz for mm-wave phased-arrays.

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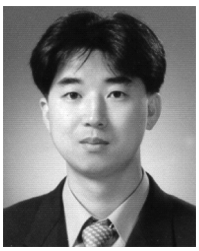

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Prof. Rebeiz is an IEEE Fellow, an NSF Presidential Young Investigator, an URSI Koga Gold Medal Recipient, an IEEE MTT Distinguished Young Engineer (2003), and is the recipient of the IEEE MTT 2000 Microwave Prize. He also received the 1998 Eta Kappa Nu Professor of the Year Award and the 1998 Amoco Teaching Award given to the best undergraduate teacher at the University of Michigan, and the 2008 Teacher of the Year Award at the Jacobs School of Engineering, UCSD. He has been an Associate Editor of IEEE MTT, and a Distinguished Lecturer for IEEE MTT and IEEE AP. He leads a group of 21 Ph.D. students and three Post-Doctoral Fellows in the area of mm-wave RFIC, microwaves circuits, RF MEMS, planar mm-wave antennas and terahertz systems, and is the Director of the UCSD/DARPA Center on RF MEMS Reliability and Design Fundamentals. He is the author of the book *RF MEMS: Theory, Design and Technology* (Wiley, 2003).