Ka-Band Low-Loss and High-Isolation Switch Design in 0.13-μm CMOS

Byung-Wook Min, *Student Member, IEEE*, and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—This paper presents designs and measurements of Ka-band single-pole single-throw (SPST) and single-pole double-throw (SPDT) 0.13-μm CMOS switches. Designs based on series and shunt switches on low and high substrate resistance networks are presented. It is found that the shunt switch and the series switch with a high substrate resistance network have a lower insertion loss than a standard designs. The shunt SPST switch shows an insertion loss of 1.0 dB and an isolation of 26 dB at 35 GHz. The series SPDT switch with a high substrate resistance network shows excellent performance with 2.2-dB insertion loss and $>$ 32-dB isolation at 35 GHz, and this is achieved using two parallel resonant networks. The series-shunt SPDT switch using deep n-well nMOS transistors for a high substrate resistance network results in an insertion loss and isolation of 2.6 and 27 dB, respectively, at 35 GHz. For series switches, the input 1-dB compression point ($\mathrm{IP}_{1\,\mathrm{dB}}$) can be significantly increased to $\sim$ 23 dBm with the use of a high substrate resistance design. In contrast, $\mathrm{IP}_{1\,\mathrm{dB}}$ of shunt switches is limited by the self-biasing effect to 12 dBm independent of the substrate resistance network. The paper shows that, with good design, several 0.13-μm CMOS designs can be used for state-of-the-art switches at 26–40 GHz.**

***Index Terms*—CMOS switch, Ka-band, millimeter wave, RF switch, single-pole double-throw (SPDT) switch, single-pole single-throw (SPST) switch, substrate networks, 0.13-μm CMOS.**

I. Introduction

SWITCHES ARE one of the important building blocks in RF/millimeter-wave systems. Single-pole single-throw (SPST) and single-pole double-throw (SPDT) switches can be used for various applications such as transmit/receive modules, variable attenuators and phase shifters, wideband pulse generators, and multistandard communication systems. The switches are commonly designed using III–V semiconductor-based transistors or diodes. However, as CMOS technology is scaled down and adopted for many RF integrated systems, CMOS transistor-based switches have become great candidates for low-loss designs at dc–5 GHz [1]–[5]. CMOS switch design above 10 GHz is still challenging due to a high insertion loss and low isolation, as well as relatively low power-handling capability [6]–[9]. Therefore, CMOS switches for millimeter-wave frequencies are not reported much even though CMOS integrated circuits have been developed for millimeter-wave systems [10], [11].

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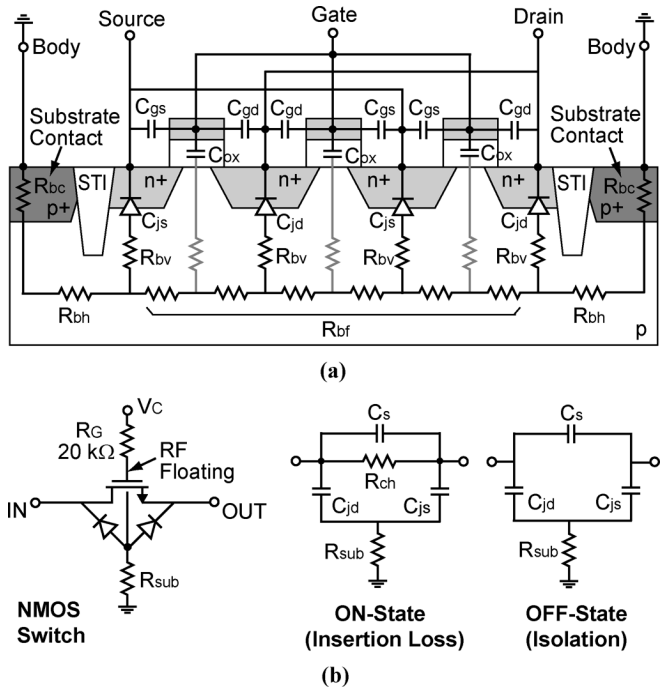

Fig. 1. (a) Cross-sectional view and equivalent-circuit model of nMOS transistor. (b) Schematic of a nMOS switch and its simplified small-signal circuit model of on and off states.

The main limitation of CMOS transistors when used as a switch is the junction diode between the source/drain node and the substrate (Fig. 1). The junction diodes increase the signal loss and also limit the signal voltage swing. Since the impedance of the junction capacitance is very low at millimeter-wave frequencies, the substrate resistance network (R_{sub}) from the junction to the substrate ground is also an important issue [12]. In this paper, various CMOS SPST and SPDT switches are designed at 35 GHz with careful consideration to the substrate resistance network. In Section II, the effect of the substrate resistance network for CMOS switch design is explained, and the designs and measurements are presented in Sections III and IV.

II. CMOS Switches

A. CMOS Transistor and Substrate Network

Fig. 1(a) shows a simplified equivalent circuit of an nMOS transistor with three gate fingers. The nMOS transistor is a four-port device with a body node connected to the substrate contact, as well as the gate, source, and drain nodes. C_{js} and C_{jd} are

junction capacitances of the source and drain junction diodes, and $C_{\rm gs}$ and C_{gd} are the parasitic capacitance between the gate and the source and drain. There are substrate-related resistances between the source/drain junction and the body node. This substrate resistance networks include the vertical and horizontal resistances ($R_{\rm bv}$ and $R_{\rm bh}$), the resistance between the junctions of gate fingers ($R_{\rm bf}$), and the substrate contact resistance ($R_{\rm bc}$).

The substrate resistance network significantly affects the transistor characteristics at millimeter-wave frequencies, and depends on many factors such as size and distance of substrate contacts, transistor size, number of gate fingers, and even nearby circuit elements [13], [14]. Since these factors are related to a specific circuit layout, the substrate resistance network is not usually modeled in a CMOS process. Recent transistor models provide simplified model parameters for the substrate resistance networks, and the parameters can be used for modeling a transistor pre-laid out with substrate contacts [15]. However, the simplified model can be inaccurate and cannot take into account nearby circuit elements. Computing a distributed network of the substrate resistance networks has been tried, but takes a long simulation time or is limited to simple layouts [16]–[18]. Therefore, one way of minimizing the uncertainty in the substrate resistance network is to design circuits with either a very low (minimizing) or very high (maximizing) substrate resistance network.

B. CMOS Switch Model

A nMOS transistor can be used as a switch by controlling the gate voltage, and a gate resistor, i.e., $R_G = 20$ kΩ, is required in order to prevent signal leaking and oxide breakdown. The simplified equivalent circuit of the nMOS switch is shown in Fig. 1(b). C_s is the series capacitance due to $C_{\rm gs}$ and C_{gd}, and $R_{\rm ch}$ is the on-state channel resistance. $R_{\rm sub}$ is the resistance due to $R_{\rm bv}$, $R_{\rm bh}$, $R_{\rm bf}$, and $R_{\rm bc}$. This single resistor model for the substrate resistance network has been shown to be accurate up to 10 GHz. Three or five resistor models can represent the substrate resistance network more accurately [19]–[21], but the resistance values of these models depend on the layout and cannot be provided in a transistor model.

To improve the insertion loss of an nMOS switch, $R_{\rm ch}$ of the nMOS transistor is usually reduced by enlarging the gatewidth even though the isolation is sacrificed. However, the enlarged junction capacitances ($C_{\rm js}$ and $C_{\rm jd}$) also increase the capacitive coupling to the substrate, resulting in an increase of the signal loss, especially above 10 GHz. This means that there is an optimum value for the gatewidth in order to minimize the insertion loss at a given frequency and port impedance [22]. Fig. 2 shows that, in the case of $R_{\rm sub} = 50\ \Omega$, the insertion loss at 35 GHz is minimized when the gatewidth is 20–26 μm. When $R_{\rm sub}$ is much higher than the port impedance ($R_{\rm sub} = 1$ kΩ, $Z_{\rm o} = 50\,\Omega$), the insertion loss keeps decreasing as the gatewidth is enlarged even to $> 120\ \mu$m. This is because the common node of $C_{\rm js}$ and $C_{\rm jd}$ is floating, and $C_{\rm js}$ and $C_{\rm jd}$ couple the RF signal between the input (drain) and output (source) without leaking to the substrate. However, for the same reasons, the off-state isolation is significantly worse than that of the nMOS switch with a low $R_{\rm sub}$.

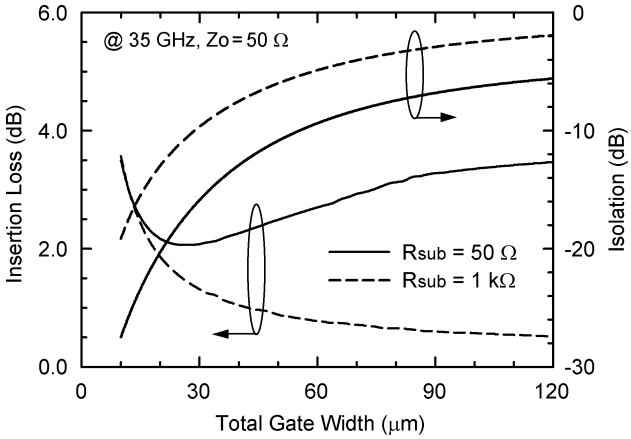

Fig. 2. Simulated insertion loss and isolation of an intrinsic nMOS switch at 35 GHz versus the gatewidth with a referenced port impedance of 50 Ω.

III. SPST and SPDT Switch Design

Various SPST and SPDT switches are designed using a 0.13-μm BiCMOS process (IBM 8HP) for Ka-band frequencies ($f_{\rm o} = 35$ GHz). For the CMOS transistors, the BSIM4v2 model is provided by the design kit. However, the substrate resistance network is not modeled, and the single resistor model ($R_{\rm sub}$) is left to be defined by the user [23]. At Ka-band frequencies, this $R_{\rm sub}$ value has to be considered carefully for a low-loss switch design because of the low impedance of the junction capacitance ($C_{\rm js}$ and $C_{\rm jd}$).

A. Low-$R_{\rm sub}$ Series SPST Switch

To reduce the signal loss due to $C_{\rm js}$ and $C_{\rm jd}$, inductors (L_M) can be placed at the input and output of an nMOS switch as a matching circuit [see Fig. 3(a)]. If $R_{\rm sub} \approx 0$, one can increase the gatewidth higher than the optimum value of Fig. 2, and match $C_{\rm js}$ and $C_{\rm jd}$ using series inductors. However, $R_{\rm sub}$ is roughly estimated to be 30–100 Ω even with a very large substrate contact, and therefore, a lossless matching network is not possible due to the low circuit quality factor ($Q = 1/\omega R_{\rm sub} C_{\rm js}$). With an estimation of $R_{\rm sub} \approx 50\ \Omega$, L_M and the gatewidth for minimum insertion loss are found to be 50 pH and 28 μm ($N_f = 15$, $w = 1.9\ \mu$m), respectively. For $R_{\rm sub} \approx 50\ \Omega$, the transistor is entirely surrounded by a large substrate contact ($90 \times 25\ \mu$m^2) placed very closely to the transistor [see Fig. 3(b)]. The simulated insertion loss and isolation are 2.6 and 10 dB, respectively. The isolation of the series SPST switch is lower than the isolation of the intrinsic nMOS switch of Fig. 2 since L_M matches $C_{\rm js}$ and $C_{\rm jd}$ also in the off state. To increase the switch isolation, a shunt switch is often used together with a series switch, especially for an SPDT switch. However, the insertion loss of the series-shunt switch cannot be lower than that of the series SPST switch.

B. Low-$R_{\rm sub}$ Shunt SPST and SPDT Switches

NMOS switches can be used as shunt elements for a low-loss SPST switch, and the circuit is shown in Fig. 4(a). $C_{\rm eq}$ and $R_{\rm eq}$

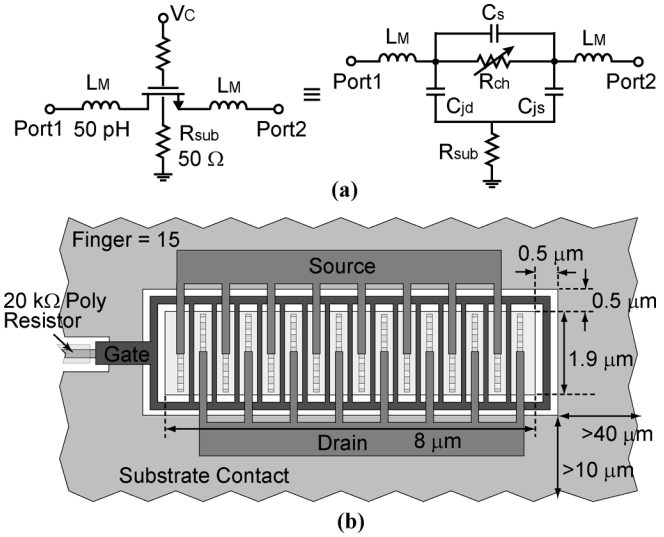

Fig. 3. (a) Schematics of the low-$R_{\rm sub}$ series SPST switch. (b) nMOS transistor layout for the switch.

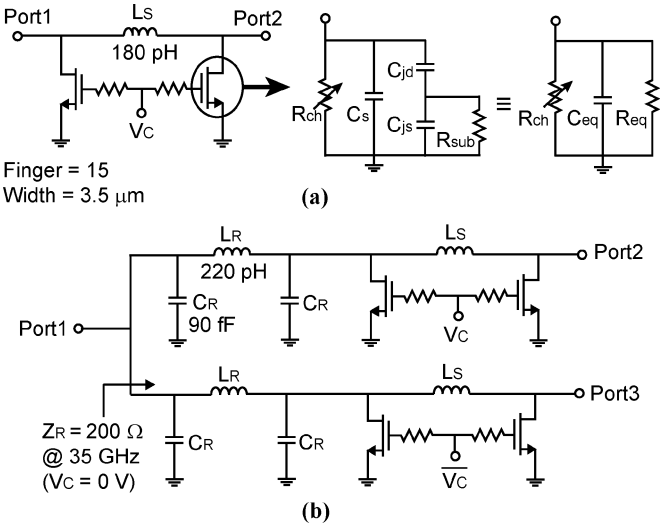

Fig. 4. Schematics of the low-$R_{\rm sub}$ shunt: (a) SPST and (b) SPDT switches.

of the equivalent circuit are calculated using

$$R_{\rm eq} = \frac{4\omega^2 R_{\rm sub}^2 C_j^2 + 1}{\omega^2 R_{\rm sub} C_j^2} > \frac{4}{\omega C_j} \tag{1}$$

$$C_{\rm eq} = \frac{C_j + 2\omega^2 R_{\rm sub}^2 C_j^3}{4\omega^2 R_{\rm sub}^2 C_j^2 + 1} + C_s \tag{2}$$

where $C_j = C_{\rm js} = C_{\rm jd}$. $R_{\rm eq}$ is usually large ($> 500\ \Omega$) unless the transistor is very wide. Therefore, the gatewidth of the shunt switch can be chosen to be larger than that of the series switch, and the shunt capacitance $C_{\rm eq}$ can be matched using inductors. Π-type matching with two shunt switches and a series inductor (L_S) is preferred over T-type matching with one shunt switch since it requires only one inductor and provides a higher isolation. The isolation of Π-type matching with two nMOS($1\times$) switches is higher by ~ 10 dB at 35 GHz than that of T-type matching with a twice wider nMOS($2\times$) switch due to

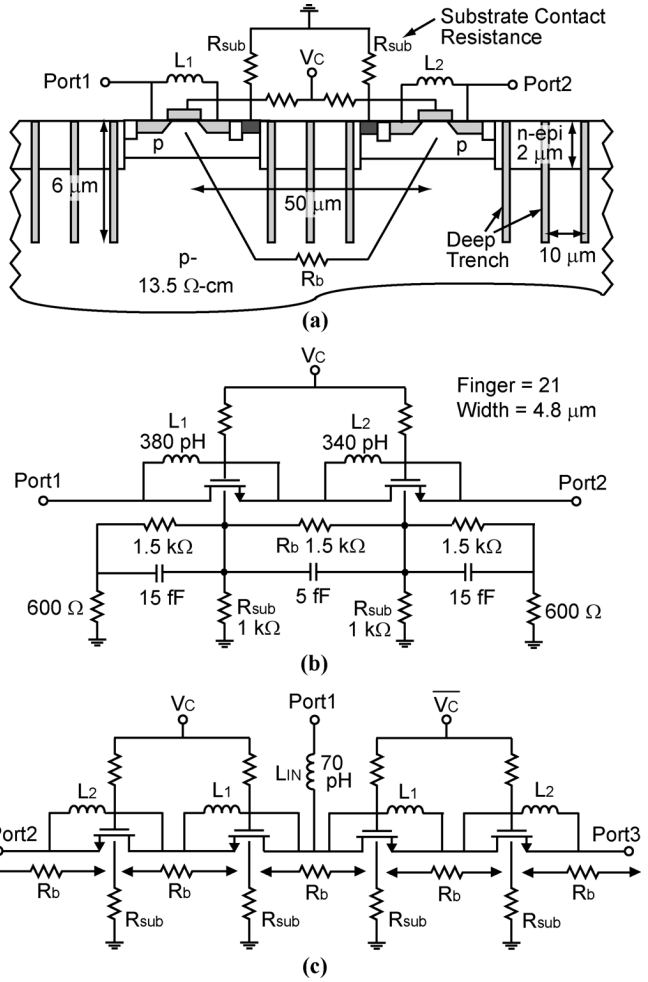

Fig. 5. (a) Cross-sectional view and (b) schematic of the high-$R_{\rm sub}$ series SPST switch. (c) Schematic of the high-$R_{\rm sub}$ series SPDT switch.

the impedance transformation of the Π-network (L_S and $C_{\rm eq}$'s). In this shunt switch design, $R_{\rm sub}$ is estimated to be 50 Ω, and the gatewidth of 52.5 μm ($N_f = 15$, $w = 3.5$ μm) is chosen to provide $>$ 25-dB isolation at 35 GHz.

Fig. 4(b) shows an SPDT switch design using two shunt SPST switches. C_R–L_R–C_R Π-network acts as a $\lambda/4$ transmission line and transforms the low impedance of the off-state SPST switch to a high impedance ($Z_R \approx 200\ \Omega$) at the common node of the SPDT switch. The impedance, i.e., Z_R, is limited by the input impedance of the off-state SPST switch. The simulated loss of the Π-network is $<$ 0.5 dB and is lower than the loss of the low-$R_{\rm sub}$ series switches. Therefore, at millimeter-wave frequencies, it is better to use $\lambda/4$-based designs for relatively narrowband applications rather than a traditional low-$R_{\rm sub}$ series-shunt SPDT design.

C. High-$R_{\rm sub}$ Series SPST and SPDT Switches

Even if the capacitive coupling due to the junction capacitances of the nMOS switch can be minimized by increasing $R_{\rm sub}$, it was shown in Section II-B that the high-$R_{\rm sub}$ design significantly decreases the series switch isolation (see Fig. 2). In this case, the isolation can be greatly improved by adding an inductor between the source and drain nodes, which resonates

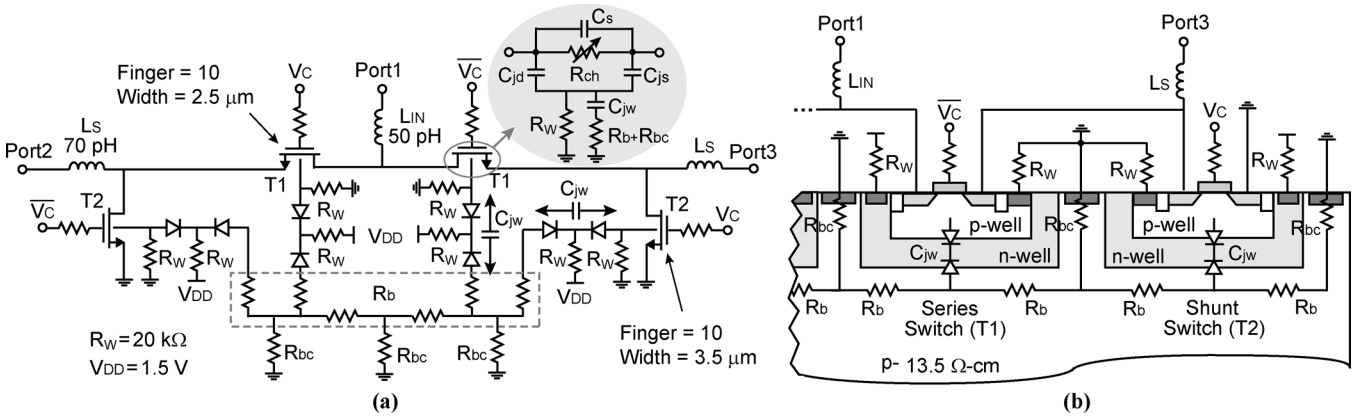

Fig. 6. (a) Schematic and (b) cross-sectional view of the series-shunt SPDT switch using deep n-well nMOS transistors (half-circuit is shown).

with the total series capacitance C_t (see Fig. 1)

$$C_t = \frac{C_{\rm js} \times C_{\rm jd}}{C_{\rm js} + C_{\rm jd}} + C_s \tag{3}$$

at a desired frequency [12], [24].

Fig. 5(a) and (b) presents the high-$R_{\rm sub}$ series SPST switch at 35 GHz. In order to increase $R_{\rm sub}$, the substrate contact resistance ($R_{\rm bc}$) of Fig. 1(a) is increased by adopting a very small substrate contact (0.28×5 μm^2) close to the nMOS transistor. The SPST switch consist of two series nMOS transistors with a large gatewidth of 100 μm ($N_f = 21$, $w = 4.8$ μm). The resonant inductors ($L_1 = 380$ pH, $L_2 = 340$ pH) are connected between the source and drain to increase the isolation. L_1 and L_2 have different sizes, and resonate with the series capacitances at two different frequencies (34 and 36 GHz) to increase the total isolation bandwidth. For the same insertion loss, two large nMOS($2\times = 100$ μm) switches in series are preferred than one small nMOS($1\times = 50$ μm) switch since L_1 and L_2 values are more reasonable and the total isolation bandwidth is wider.

The nMOS transistors are separated 50 μm away for high isolation between the junctions [see Fig. 5(a)]. Since $R_{\rm sub}$ is very high, the substrate resistance R_b between the junctions of the two nMOS transistors also has to be as high as possible. To increase R_b, the nMOS transistors are surrounded by an isolation moat (n-type epitaxial layer) and deep trenches. The isolation moat and deep trench have a thickness of 2 and 6 μm, respectively, and also prevent the nMOS transistors from latch-up and coupling with other circuits around the switch. The simulated insertion loss and isolation at 35 GHz are 1.9 and $>$ 30 dB with the assumption of $R_b = 1$ kΩ. The high-$R_{\rm sub}$ series SPDT switch is also implemented using two SPST switches [see Fig. 5(c)]. The shunt capacitance of the capacitive T-junction is matched using a meander line inductor $L_{\rm IN} = 70$ pH.

D. High-$R_{\rm sub}$ Deep n-Well Series-Shunt SPDT Switch

Another way to obtain a high $R_{\rm sub}$ is with the use of a deep n-well nMOS transistor (Fig. 6) [5], [8]. The isolated p-well and the deep n-well are biased with large resistors ($R_W = 20$ kΩ) to 0 and 1.5 V, respectively, to establish a reverse-bias junction without decreasing $R_{\rm sub}$. To increase the low isolation of the high-$R_{\rm sub}$ series switch, a shunt switch is also required, resulting in a series-shunt design. The SPDT switch are designed to achieve an isolation of $\sim$ 30 dB at 35 GHz, and the series and shunt transistor sizes (*T1* and *T2*) are optimized for the lowest insertion loss. The capacitive T-junction and the capacitance of shunt switches are matched by inductors $L_{\rm IN}$ and L_S, respectively.

Even though the $R_{\rm sub}$ value of the deep n-well series-shunt switch is increased using R_W, the effective impedance from the source and drain junctions to ground is lower than R_W due to the junction capacitances of the deep n-well (C_{jw}). C_{jw} depends on the deep n-well area and the bias voltages, and the C_{jw} of *T1* is approximately 45 fF ($j100$ Ω at 35 GHz) for an applied voltage of 0 and 1.5 V for the p- and n-well, respectively. (C_{jw} can be reduced with higher reverse bias voltages, but this requires special voltage levels.) Therefore, the effective $R_{\rm sub}$ value using a deep n-well process is limited by C_{jw} at millimeter-wave frequencies. The effective $R_{\rm sub}$ value can be increased with a high R_b and $R_{\rm bc}$, but the nMOS transistors and nearby circuits have to be well separated, as in the case of the high-$R_{\rm sub}$ series switch, resulting in a relatively large chip area. To achieve a small chip area in this design, relatively good substrate contacts (3×11 μm^2) are placed at both sides of the transistors for a device isolation, even though the effective $R_{\rm sub}$ value is lowered to $\sim$ 300–500 Ω.

IV. Simulated and Measured Results

All inductors and interconnecting lines were simulated using full-wave electromagnetic (EM) software (Sonnet[1]), and the CMOS model provided by the IBM 8HP design kit was used. The CMOS switches were measured on-chip with Agilent E8364B network analyzer using short-open-load-thru (SOLT) calibration to the probe tips. The pad transitions are deembeded using measured back-to-back transitions (0.18-dB loss at 35-GHz per pad transition), and the reference planes are shown in Fig. 7 together with the locations of nMOS transistors and chip sizes.

A. SPST Switches

Fig. 8 presents the measured and simulated insertion loss and return loss of the three different SPST switches. Since there is no deterministic way to calculate the substrate resistance networks,

[1]Sonnet, ver. 10.53, Sonnet Software Inc., Syracuse, NY, 1986–2005.

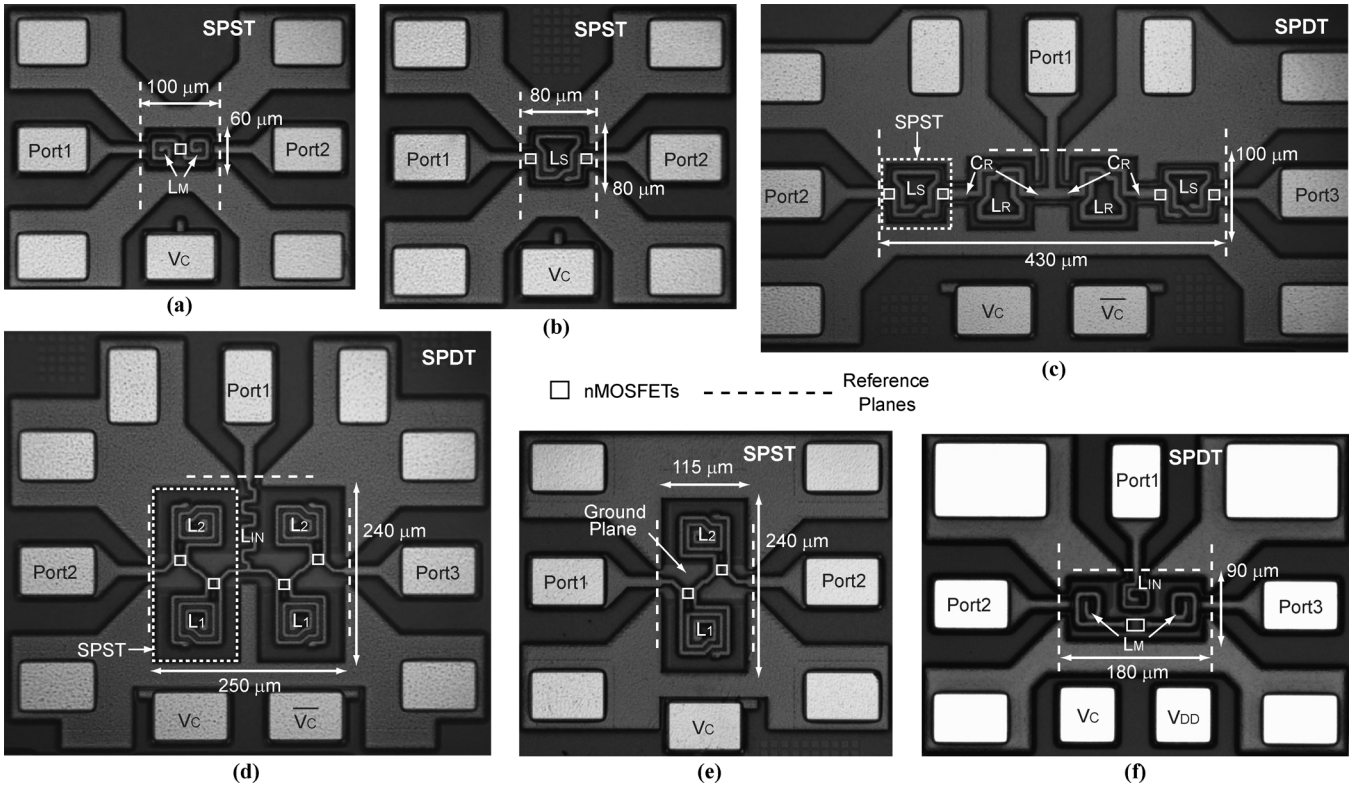

Fig. 7. Microphotograph of the: (a) low-$R_{\rm sub}$ series SPST, (b) low-$R_{\rm sub}$ shunt SPST, (c) low-$R_{\rm sub}$ shunt SPDT, (d) high-$R_{\rm sub}$ series SPDT, (e) high-$R_{\rm sub}$ series SPST, and (f) deep n-well series-shunt SPDT switches.

$R_{\rm sub}$ is assumed to be 50 Ω in the simulation of the low-$R_{\rm sub}$ series and shunt SPST switches. For the case of the high-$R_{\rm sub}$ series switch, the modeled substrate resistance network is shown in Fig. 5(b), where the capacitance due to the deep trenches are also considered.

The measured insertion loss of the low-$R_{\rm sub}$ series switch is 2.6 dB at 35 GHz with a isolation of 10 dB (Fig. 9). The low-$R_{\rm sub}$ Π-shunt switch has only 1.0-dB insertion loss and 26-dB isolation at 35 GHz, and shows the state-of-the-art performance. The measured insertion loss of the high-$R_{\rm sub}$ series switch is 1.8 dB at 35 GHz, and each nMOS transistor switch accounts for 0.9-dB loss. The associated isolation shows the tuned resonances and is $>$ 25dB at 34–42 GHz. This proves that the substrate resistance between the transistors is very high ($R_b \approx 1.5$ kΩ). All the SPST switches have a return loss < -18 dB at 35 GHz. Among the different SPST switch configurations, the low-$R_{\rm sub}$ Π-shunt switch has the best overall performance. As discussed in Section III-B, $R_{\rm eq}$ of (1) is relatively high for the low-$R_{\rm sub}$ Π-shunt switch, but can be increased even higher with a high-$R_{\rm sub}$ design, resulting in a lower insertion loss. Simulations indicate that the high-$R_{\rm sub}$ Π-shunt switch results in an insertion loss improvement of 0.5 dB at 35 GHz without a degradation in isolation.

B. SPDT Switches

The measured insertion loss and return loss of the low-$R_{\rm sub}$ shunt SPDT switch are shown in Fig. 10(a). The insertion loss and return loss are 2.4 and -15 dB, respectively, at 35 GHz with an isolation of 31 dB (Fig. 11). The insertion loss of this design is a little higher than the shunt SPST switch due to the relatively low impedance of the off-state SPST switch at the T-junction [$Z_R = 200$ Ω, see Fig. 4(b)]. Simulations of the high-$R_{\rm sub}$ shunt SPDT switch also show that the insertion loss can be improved by 0.5 dB without a degradation in isolation.

The high-$R_{\rm sub}$ series SPDT switch with a parallel resonant network has a measured insertion loss of 2.2 dB and a return loss of -21 dB, respectively, at 35 GHz [see Fig. 10(b)]. The measured isolation is $>$ 30 dB at 34–39 GHz and $>$ 25 dB at 33–43 GHz, and shows relatively narrowband performance. The measured insertion loss and return loss of the deep n-well series-shunt SPDT switch are also shown in Fig. 10(c). The insertion loss and return loss are 2.6 and -19 dB, respectively, at 35 GHz with an isolation of 27 dB (Fig. 11).

The low-$R_{\rm sub}$ shunt and high-$R_{\rm sub}$ series SPDT switches have excellent insertion loss and isolation at 35 GHz, but show tuned responses, either due to the C_R–L_R–C_R Π-network or the parallel resonant networks. However, the deep n-well series-shunt SPDT switch shows very wideband performance and occupies a smaller chip area (180×90 μm^2). The deep n-well series-shunt SPDT switch also does not require isolation moats and deep trenches for the isolation with other circuits.

C. Power Handling and Linearity

The main limitation of the power-handling capability is the junction diodes of the nMOS switches, which is forward biased when the peak signal voltage is higher than 0.7 V in the negative swing. In order to increase the power-handling capability of nMOS switches, a high $R_{\rm sub}$ is often used and reduces the effective voltage across the junction diode [3]–[5]. In the case of the

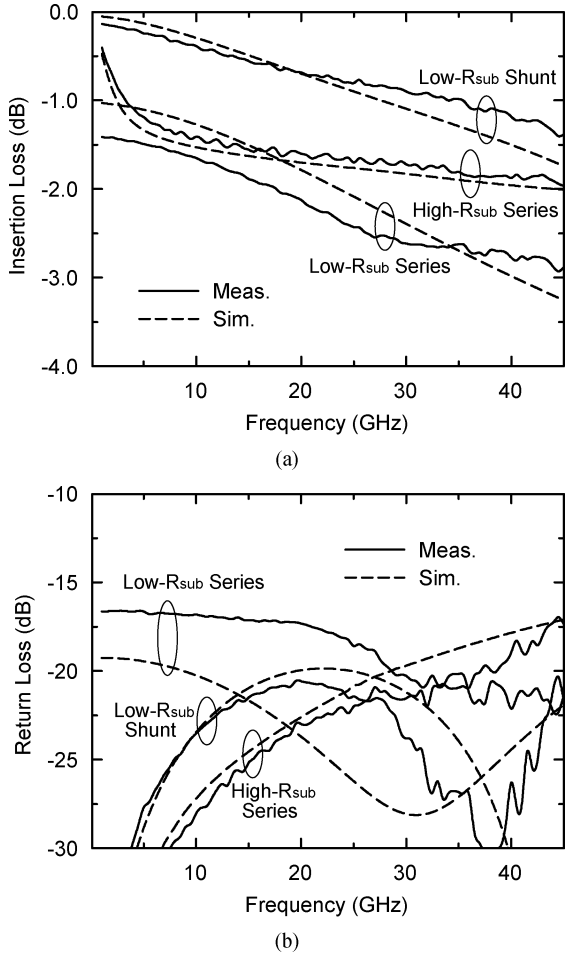

Fig. 8. Measured and simulated: (a) insertion loss and (b) return loss of the SPST switches.

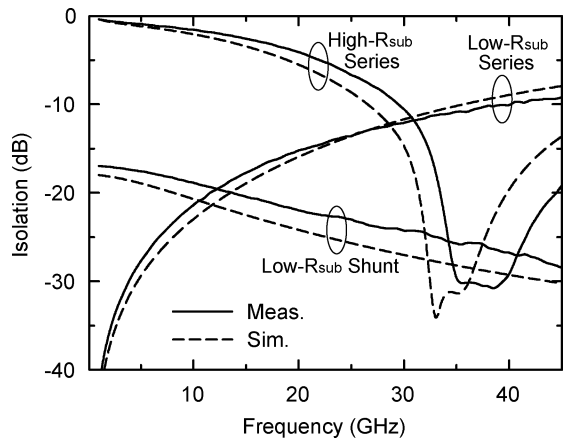

Fig. 9. Measured and simulated isolation of the SPST switches.

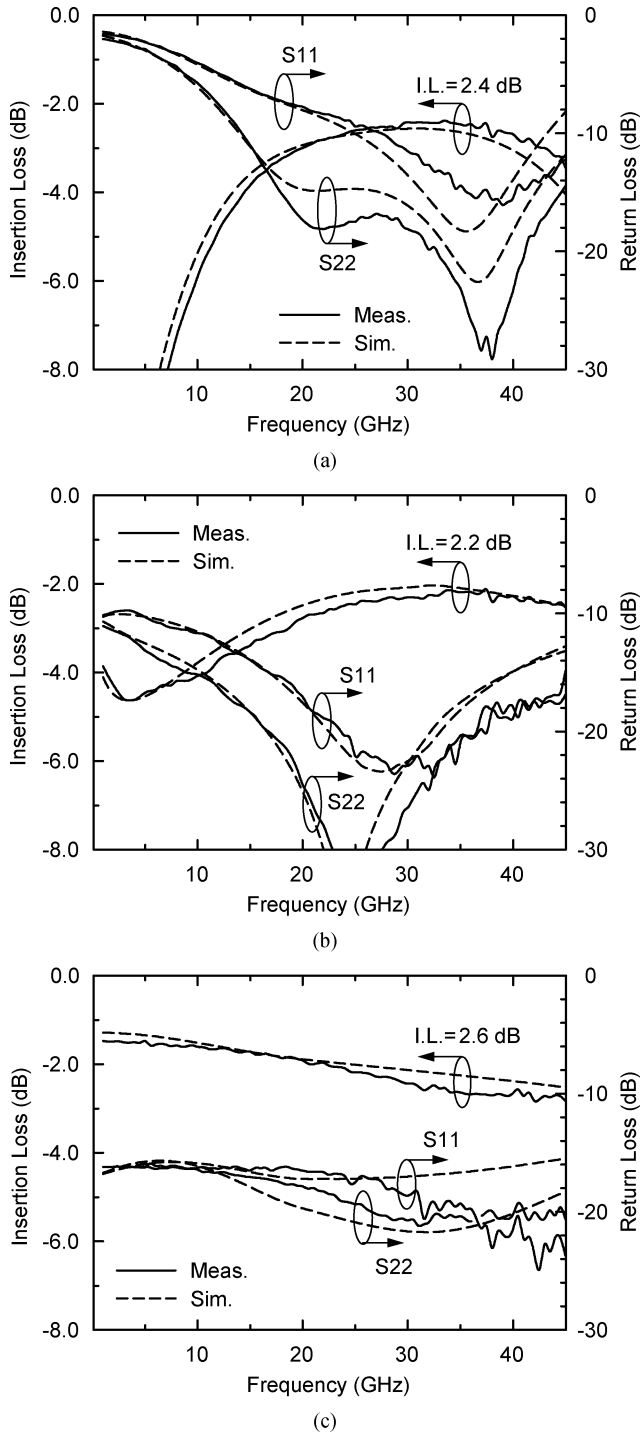

Fig. 10. Measured and simulated insertion loss and return loss of the: (a) low-$R_{\rm sub}$ shunt SPDT, (b) high-$R_{\rm sub}$ series SPDT, and (c) deep n-well series-shunt SPDT switches.

shunt switch, a self-biasing effect can also limit the power-handling capability. The gate voltage of a nMOS switch is bootstrapped by the source and drain voltage due to the gate resistor (R_G) and, therefore, the gate voltage of the shunt switch is the half of the input (drain) voltage because the source is grounded. Therefore, the shunt switch is self-biased when the input voltage is higher than twice the threshold voltage of the nMOS transistor.

Fig. 12(a) shows the measured insertion loss and isolation of the SPST switches versus the input power at 35 GHz. The input 1-dB compression point ($\mathrm{IP}_{1\ \mathrm{dB}}$) of the low-$R_{\rm sub}$ series and Π-shunt SPST switches are 15 and 12 dBm, respectively. The shunt SPST switch has a lower $\mathrm{IP}_{1\ \mathrm{dB}}$, and the gain compresses a little faster due to the self-biasing effect. The gain (insertion loss) of the high-$R_{\rm sub}$ series SPST switch does not compress up to 22 dBm of input power due to the high-$R_{\rm sub}$ value.

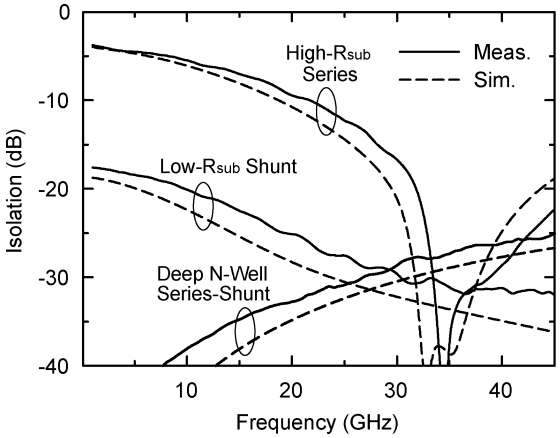

Fig. 11. Measured and simulated isolation of the SPDT switches.

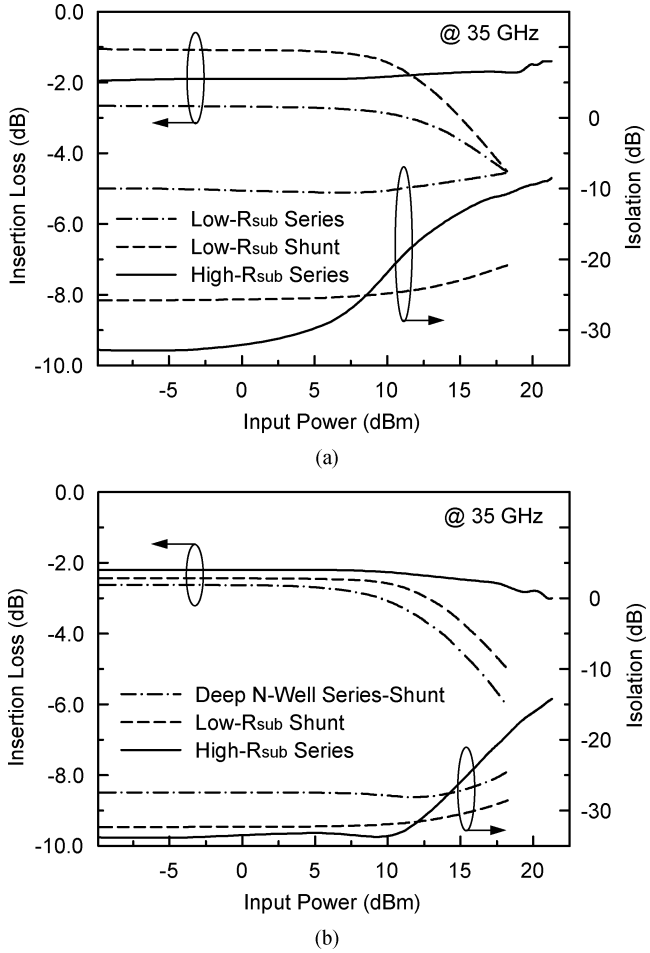

Fig. 12. Measured insertion loss and isolation versus input power of the: (a) SPST and (b) SPDT switches.

However, the off-state gain (isolation) of the high-$R_{\rm sub}$ series SPST switch expands as the input power is increased. This is explained by the high isolation of this switch, which results in a large voltage between the drain (input) and source (output) of the off-state switch at an input power of $>$ 5 dBm and the self-biasing effect.

TABLE I
PERFORMANCE SUMMARY OF THE Ka-BAND CMOS SWITCHES.

	@ 35 GHz	I.L. (dB)	R.L. (dB)	Isol. (dB)	IP1dB (dBm)	P25dB* (dBm)	IIP3† (dBm)
SPST	Low-Rsub Series	2.6	−21	10	15	n/a	26
	High-Rsub Series	1.8	−20	32	>22	8	31
	Low-Rsub Shunt	1.0	−27	26	12	9	31
SPDT	High-Rsub Series	2.2	−21	>32	~23	16	32
	Low-Rsub Shunt	2.4	−15	31	14	>19	31
	Deep N-Well Series-Shunt	2.6	−19	27	12	18	26

*Maximum input power for a isolation of >25 dB.
†Measured with a input power of <−3 dBm.

Fig. 12(b) shows the measured insertion loss and isolation of the SPDT switches versus the input power at 35 GHz. The $\rm IP_{1\ dB}$ of the Π-shunt SPDT switch is 14 dBm. The $\rm IP_{1\ dB}$ of the high-$R_{\rm sub}$ series SPDT is approximately 23 dBm. The gain (insertion loss) of the high-$R_{\rm sub}$ SPDT switch compresses because the isolation of the off-state SPST switch decreases when the input power is increased. The gain (isolation) expansion of the high-$R_{\rm sub}$ series SPDT switch occurs at a higher input power than the SPST switch. This is because the SPDT switch always has a 50-Ω input impedance, but the SPST switch has a high input impedance when the switch is off. For the high-$R_{\rm sub}$ SPDT switch, the isolation is better than 25 dB up to an input power of 16 dBm. The deep n-well series-shunt switch has an $\rm IP_{1\ dB}$ of 12 dBm, and changes little in isolation versus input power.

The input third-order intermodulation intercept points (IIP3s) are also measured at 35 GHz with an offset frequency of 1 MHz, and all the results are summarized in Table I.

V. CONCLUSION

This paper has presented several 0.13-μm CMOS SPST and SPDT switches operating for Ka-band applications. It is found that the substrate resistance network of CMOS transistors is a very important factor for millimeter-wave CMOS switch designs. For SPST switches, the shunt topology (low and high $R_{\rm sub}$) results in superior performance compared to series designs. However, the series switch isolation and power handling can be improved with the use of a high-$R_{\rm sub}$ design and parallel resonant networks, but at the expense of isolation bandwidth. For the SPDT case, the high-$R_{\rm sub}$ deep n-well switch results in very small chip area and wideband performances. If high power handling is desired, the high-$R_{\rm sub}$ series SPDT switch is recommended, but results in narrow isolation bandwidth.

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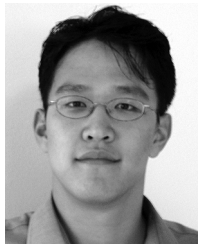

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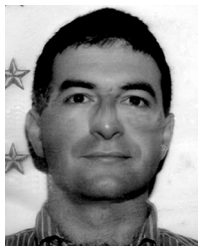

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