# Design of High-Efficiency Millimeter-Wave Microstrip Antennas for Silicon RFIC Applications

Ramadan A. Alhalabi
Cavendish Kinetics, Inc.
San Jose, CA, USA

Gabriel M. Rebeiz
Electrical and Computer Engineering Department
University of California, San Diego
San Diego, CA, USA

***Abstract*— This paper presents the design information for a W-band high-efficiency, electromagnetically-coupled on-chip silicon microstrip antenna. The antenna is composed of a quartz substrate placed on top of a commercial low-resistivity SiGe BiCMOS silicon chip. Design criteria for the microstrip antenna taking into account the dielectric and metal-density rules for the different layers of the BiCMOS silicon chip are presented. The antenna results in a measured $S_{11}$ bandwidth of 91.5-98.5 GHz, a measured gain of 0.7-3.9 dB and a radiation efficiency of 48 +/- 8% at 91-100 GHz. The design is scalable to NxM elements and to wafer-scale arrays. The application areas are in wafer-scale phased arrays, on-chip low-power sensors, communication systems, and mm-wave collision avoidance radars. To our knowledge, this is the highest gain and efficiency silicon on-chip antenna at mm-wave frequencies.**

***Keywords-component; Automotive radar; integrated antennas; millimeter-wave antennas; planar antennas; on-chip antennas; W-band; 24 GHz; 60 GHz; 94 GHz.***

## I. INTRODUCTION

Silicon substrates introduce special challenges for high efficiency millimeter-wave on-chip antennas. First, their low resistivity of 0.1-10 Ω-cm results in high dielectric loss and significantly reduces the antenna efficiency. Second, TE and TM surface waves are easily triggered in 200-500 μm thick silicon substrates and can have serious detrimental effects on the antenna pattern and efficiency [1, 2].

In the past few years, a lot of work has been done on on-chip antennas. A 24 GHz transmitter with on-chip zigzag dipole with a measured gain around -12 dB is presented in [3]. Zhang, Sun and Guo presented on-chip inverted-F and quasi-Yagi antennas with gains of -19 dB and -12.5 dB at 61 GHz and 65 GHz, respectively [4]. A 60 GHz millimeter-wave on-chip dipole antenna with a gain of -10 dB in a 0.18 μm CMOS process is presented in [5]. Hsu, Wei, Hsu and Chuang presented a 60 GHz CPW-fed on-chip Yagi-Uda antenna with a measured gain of -10 dB [6]. A 140 GHz receiver with -25 dB gain on-chip antenna is presented in [7]. A triangular loop antenna adjacent to a lossy silicon substrate is presented in [8]; the antenna has a simulated gain of -0.4 dB at 60 GHz and a measured gain of 0.9 dB using a scaled model at 2 GHz. A Yagi-Uda array of wire-bond antennas with a measured gain of 8 dB at 40 GHz is presented in [9]. This antenna occupies a large space on wafer, and is not suitable for dense integrated circuits. Wu, Tekle, Nallani, Zhang and K. K. O also presented 60 GHz bond-wire antennas with ~30% efficiency [10]. Hirokawa, Kimishima, Ando and Hirachi presented a dipole antenna on a thick resin layer on the back of a silicon chip with a gain of 3.1 dB at 60 GHz [11]. Except for the bondwire and the thick resin layer antenna, all integrated circuit antennas have low gain and efficiency at mm-wave frequencies.

In this paper, we present the design and measurement of a high-efficiency electromagnetically-coupled W-band on-chip microstrip antenna. The antenna design eliminates the effects of the silicon substrate by shielding the microstrip antenna using a ground plane made from the silicon metallization

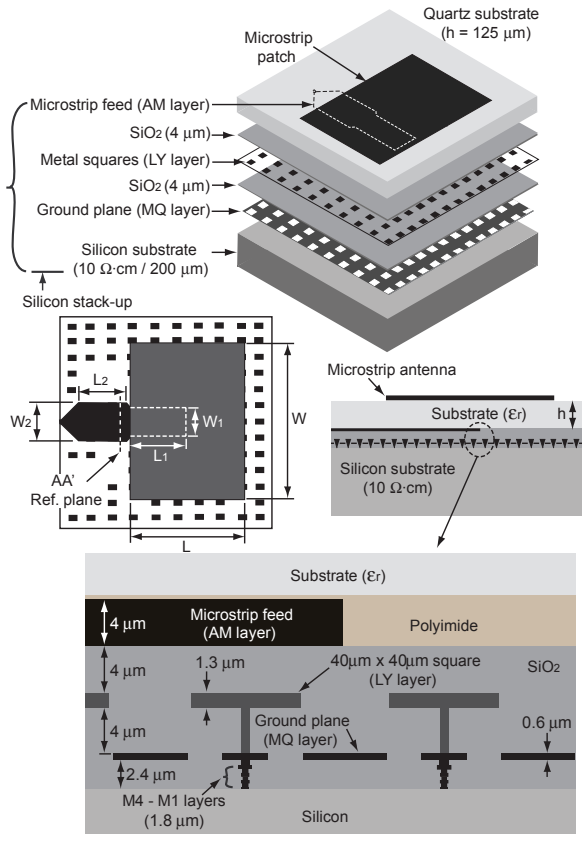


Fig. 1: On-chip EM-coupled microstrip antenna geometry: L = 690, W =970, $L_1$ =350, $W_1$ =180, $L_2$ =310, $W_2$ =230. (all dimensions are in μm)

layers. However, the thickness of the metal/$SiO_2$ layers above the silicon substrate is only 10-12 μm in most RF processes (IBM 8HP, 9RF, etc.) and it is hard to build efficient antennas with such a ground spacing. A 125 μm substrate is therefore added on top of the silicon chip so as to have enough ground-plane spacing for efficient radiation.

## II. Antenna Design

### A. Geometry

Fig. 1 presents the layout of the 94 GHz EM-coupled on-chip microstrip antenna. The microstrip antenna is integrated on a quartz substrate placed on top of silicon RFIC with a thickness h = 125 μm and a dielectric constant $\varepsilon_r = 3.8$ which results in an antenna effective dielectric constant $\varepsilon_{eff} \approx 3.45$. No via holes are used, and the feed between the silicon RFIC top metal layer (AM layer) and the microstrip antenna is achieved using electromagnetic fringing-field coupling. The ground plane of the microstrip antenna and the electromagnetic feed-probe is fabricated using the MQ layer, and isolates the antenna from the silicon substrate. Also, 40x40 μm metal squares are introduced on the LY layer to satisfy the metal density rules which are predominant in the silicon layout rules. These metal squares are tied to the silicon substrate and can have a detrimental effect on the antenna performance if not modeled.

### B. Radiation Efficiency and Input Impedance vs. h and $\varepsilon_r$

It is well known that the radiation efficiency of microstrip antenna increases as $\varepsilon_r$ decreases since the fields become loosely tied to the ground plane and the fringing fields are increased at the antenna edges. The radiation efficiency of the antenna also increases as h increases until the coupling into the $TM_0$ substrate mode starts to become significant [12]. However, for electromagnetically-coupled antennas, the amount of coupling from the feed line to the antenna puts another limit on the allowed antenna substrate thickness and on the dielectric constant. The coupling from the microstrip feed to the antenna increases as h decreases and $\varepsilon_r$ increases.

The thickness and the dielectric constant underneath the feed line also affect the coupling from the microstrip line to the antenna. The fringing field coupling is enhanced by reducing the dielectric constant and increasing the thickness underneath the feed line. However, in silicon chips, the microstrip line is located on $SiO_2$ layer with a dielectric constant of ~ 4. Also, the dielectric thickness underneath the feed line is very low and depends on the process. In most RF CMOS and SiGe processes, the total thickness between the first thick metal layer and the top metal layer is 6-10 μm [15].

Fig. 2(a) presents the HFSS [14] simulated radiation efficiency of the EM-coupled antenna vs. substrate thickness for $\varepsilon_r$ = 1, 2.2, 3.8 and 6.2. The simulations show that an efficiency of ~ 70% is achievable for h = 50-100 μm with $\varepsilon_r$ = 2.2 – 6.2, respectively. The antenna dimensions were modified for each case so that the radiation efficiency peaks at 96-98 GHz. For a small h where the coupling is sufficient (h < 50 μm), an increase in $\varepsilon_r$ reduces the efficiency since it results in a higher Q and more narrowband antenna. However, for a large substrate thickness (h > 75–100 μm), increasing the dielectric constant significantly improves the radiation efficiency by enhancing the fringing field coupling. For example, for h = 100 μm, the simulated radiation efficiency increases from 38% to 73% by increasing $\varepsilon_r$ from 1.0 to 6.2.

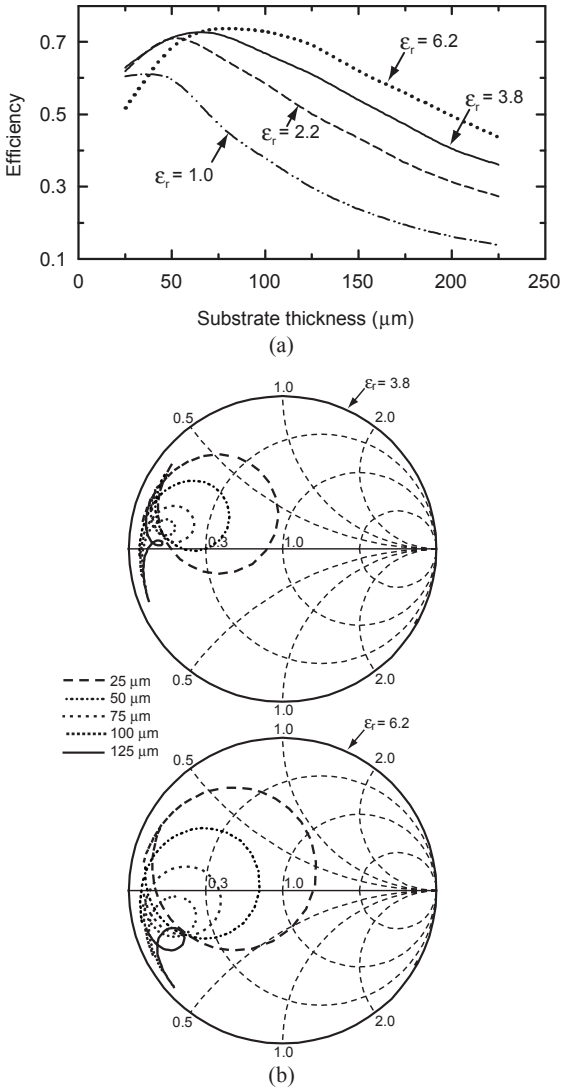


Fig. 2: HFSS simulated: (a) radiation efficiency vs. h for different $\varepsilon_r$, (b) input impedance referenced to 10 Ω for h = 25-125μm with $\varepsilon_r$ = 3.8 and 6.2.

Fig. 2(b) presents the simulated input impedance of the EM-coupled antenna vs. h for $\varepsilon_r$ = 3.8 and 6.2 (Smith-chart $Z_0$ = 10 Ω). It is clear that the antenna input impedance is very low (8–1.2 Ω for $\varepsilon_r$ = 3.8) due to the small separation between the microstrip line and the MQ-layer ground plane (~ 9 μm) compared to the separation between the microstrip line and the antenna (25–125 μm). The input impedance increases as h decreases and also for a higher $\varepsilon_r$ due to the larger fringing-field coupling.

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The low microstrip antenna impedance at plane AA' (see Fig. 1) necessitates a quarter-wave matching network. This is accomplished using a wide microstrip line in the top metal layer. The microstrip antenna impedance at plane AA' is 2–1.2 Ω for h=100-125 μm and $\varepsilon_r$=3.8, and the on-chip λ/4 line impedance is 10–8 Ω ($W_2$ = 150–200 μm, $L_2$=310 μm). The λ/4 line has a simulated loss of 0.66 dB/mm at 94 GHz, and reduces the antenna efficiency from 67–61% to 64–57%.

### C. *Radiation Efficiency vs. $L_1$ and $W_1$*

The antenna radiation efficiency is affected by changing the coupling region length $L_1$ of the microstrip feed line, and also by changing the width of the microstrip line $W_1$ underneath the antenna. Fig. 3 presents the simulated radiation efficiency for different values of $L_1$ and $W_1$. The coupling reaches a maximum value when the feed line open end approaches the middle of the microstrip antenna [13]. The coupling from the feed line to the microstrip antenna is also enhanced as the width of the feed line increases due to the increase in the fringing field area.

### D. *Effect of the LY layer*

Fig. 4 presents the simulated radiation efficiency of the antenna with and without the metal which is required to be present on the LY layer. This layer is between the MQ layer (ground plane) and the AM layer (microstrip feed line) and has its own metal density rules for RFIC fabrication. The antenna radiation efficiency is slightly reduced with 40x40 μm-squares on the LY layer due to the slight reduction of coupling from the microstrip line to the antenna. The metal squares on the LY layer can be either tied to the ground plane (MQ-layer) or go through 44x44 μm-square openings in the MQ layer and are then tied directly to the silicon substrate. The radiation efficiency is a bit lower if the LY squares are tied to the MQ layer ground plane since, in this case, the ground plane is effectively closer to the feed line. Also, since the metal density rules on the MQ layer do not allow for a continuous ground plane metal sheet, the case with openings in the MQ layer and with LY metal layer tied to the silicon substrate was chosen.

## III. MEASUREMENTS

The 94 GHz EM-coupled on-chip microstrip patch antenna fabricated using the IBM 8HP process is shown in Fig. 5(a). A

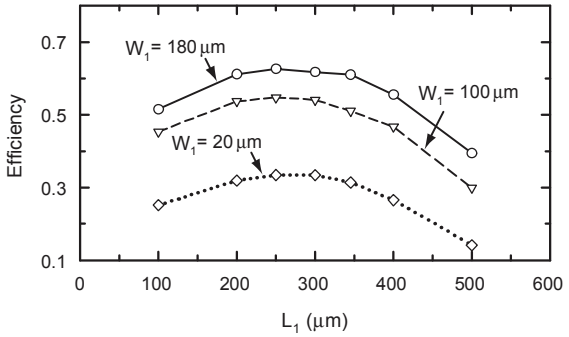



Fig. 3: HFSS simulated radiation efficiency vs. $L_1$ and $W_1$ for h = 125 μm and $\varepsilon_r$ = 3.8.

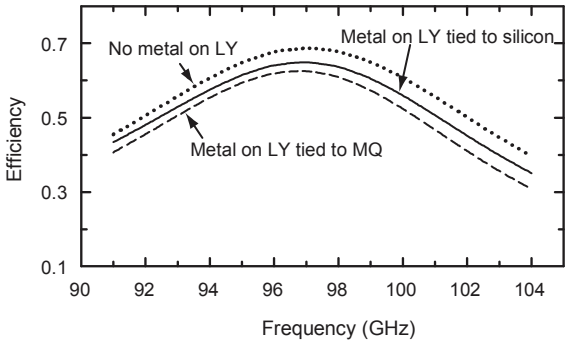
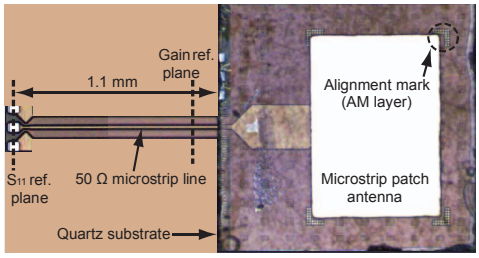
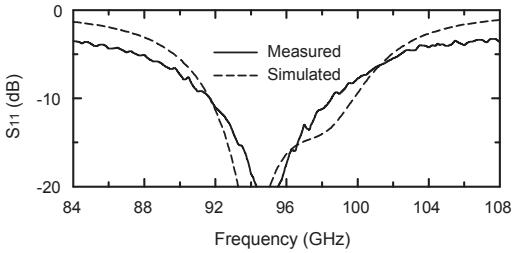



Fig. 4: HFSS simulated radiation efficiency with and without metals on LY layer.




(a)




(b)

Fig. 5: (a) Fabricated on-chip EM-coupled microstrip antenna, (b) measured and simulated $S_{11}$.

125 μm-thick quartz substrate is attached to the silicon chip using a small amount of epoxy placed at the corners. The input impedance of the antenna is measured using a CPW probe located 1.1 mm from the antenna (Fig 5(a)), and the measured $S_{11}$ agrees well with simulations with a measured -10 dB bandwidth of 91.7-98.5 GHz. (Fig. 5(b)).

The H-plane radiation patterns are measured in the receive mode using a waveguide mm-wave diode detector. The diode detector was connected to the antenna feed using a W-band GSG probe. A special circular arm set-up is used above the on-chip antenna and allows for a radial scan in the H-plane.

Fig. 6 presents the measured and simulated radiation patterns at 90-100 GHz and with good agreement. Due to the metal-chuck and CPW probe positioner, one can notice some standing waves in the measured patterns. Also, due to the GSG probe, we could not obtain reliable E-plane patterns measurements.

The absolute gain of the W-band on-chip antenna is measured using power measurements with a calibrated Agilent Power Meter (E4417), and the gain is obtained using the Friis

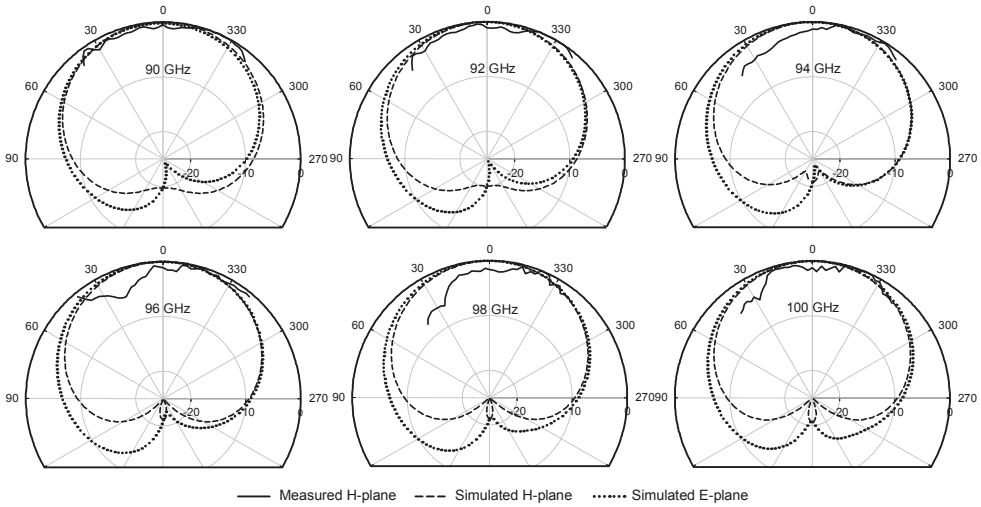



Fig. 6: Measured and simulated radiation patterns of the 94 GHz EM-coupled on-chip microstrip antenna.

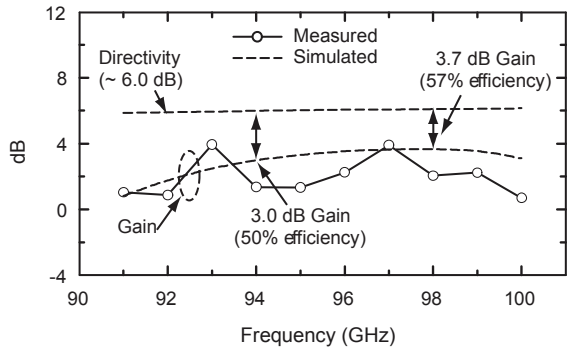



Fig. 7: Measured and simulated gain of the EM-coupled on-chip microstrip antenna.

transmission formula. The loss of the 1.1 mm on-chip microstrip line and the CPW waveguide probe are taken out of the measurement (a back-to-back probe-microstrip-probe was measured independently). Fig. 7 presents the measured gain of the on-chip antenna at 91-100 GHz and agrees well with simulations. The on-chip antenna has an efficiency of 50-57% (3-2.4 dB loss) at 94-98 GHz.

## IV. CONCLUSION

This paper presented the first on-chip high-efficiency mm-wave microstrip antenna to-date. The design is compatible with other antennas such as a differential microstrip antenna or a slot-ring antenna placed on the dielectric substrate. Also, the substrate need not be quartz, but can be Teflon, LTCC (ceramic), or even a high-resistivity silicon wafer. The design can be scaled to different frequencies such as 60 or 200 GHz.

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