60 GHz Active Phase Shifter using an Optimized Quadrature All-Pass Network in 45nm CMOS

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***Abstract*-This paper presents a differential 60 GHz phase shifter based on a vector modulator approach. The inclusion of a series resistor in the all-pass I/Q greatly reduces the effect of the capacitance loading change vs. bias current and results in a wideband phase shifter. The phase shifter achieves a gain of -6+/-2 dB with IP_{1dB} of 0-3dBm at 55GHz, and an rms phase error of <11° at 40-70GHz (P_{DC}=23 mW, V_{DD}=1.5V). This is the first demonstration of a wideband 45nm 60 GHz phase shifter.**

I. Introduction

Phase shifters are essential components in phased arrays that can be built using vector modulators [1-4], reflect [5] and switched-LC networks [6]. The reflect and switched-LC networks are single-ended in nature, but can be made differential at the expense of additional space on-wafer. The vector modulator design is advantageous due to its differential topology and compact size, but is hard to design at millimeter-wave frequencies due to the effect of the capacitive loading on the I/Q network. This paper presents a 60 GHz vector modulator in 45nm CMOS SOI using an optimized all-pass I/Q network which results in wideband operation and low RMS amplitude and phase errors.

II. DESIGN

Fig. 1 presents a block diagram of the all-pass vector modulator phase shifter and Fig. 2 shows a detailed circuit schematic using the IBM 12SOI 45nm CMOS. The metal back-end consists of 11 metal layers where all layers are copper with tungsten vias except the top metal which is an aluminum layer. The technology offers MOM capacitor. The transistor *ft* is specified as 480 GHz when referenced to M1 [7], but S-parameter measurements at UCSD using the interconnects up to the top metal results in an *ft* of 220 GHz for a 30x1 μm transistor [8].

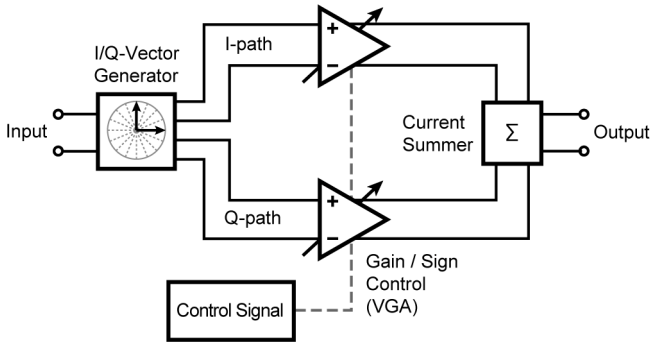

Fig. 1. Block diagram of vector-modulator active phase shifter

The vector modulator is based on the Gilbert cell topology and 20x1 um transistors are chosen for all RF transistors (Fig. 2). The gain in the I (and Q) channel is controlled using a variable current bias and current mirrors. In this design, the DAC is external to the chip so as to have maximum flexibility for testing. The output of the I and Q paths are current summed and connected to a balun for single ended measurements. The all-pass I/Q network is based on an impedance $Z_0=\sqrt{(L/C)}=R=30\ \Omega$ in order to use a relatively large capacitance value (88 fF) and reduce the C_L/C effect on the I/Q network [9].

Fig. 3 presents the simulated capacitance for the I (or Q) VGA under bias conditions from 0 to 2.5 mA. The input capacitance, C_{LI} (or C_{LQ}) varies from 10 to 15 fF, which is negligible for an X to Ka-band design, but has a large effect on a 60 GHz vector modulator with an all-pass network capacitance of C=88 fF. In this case, C_L/C=0.23-0.34 vs. bias

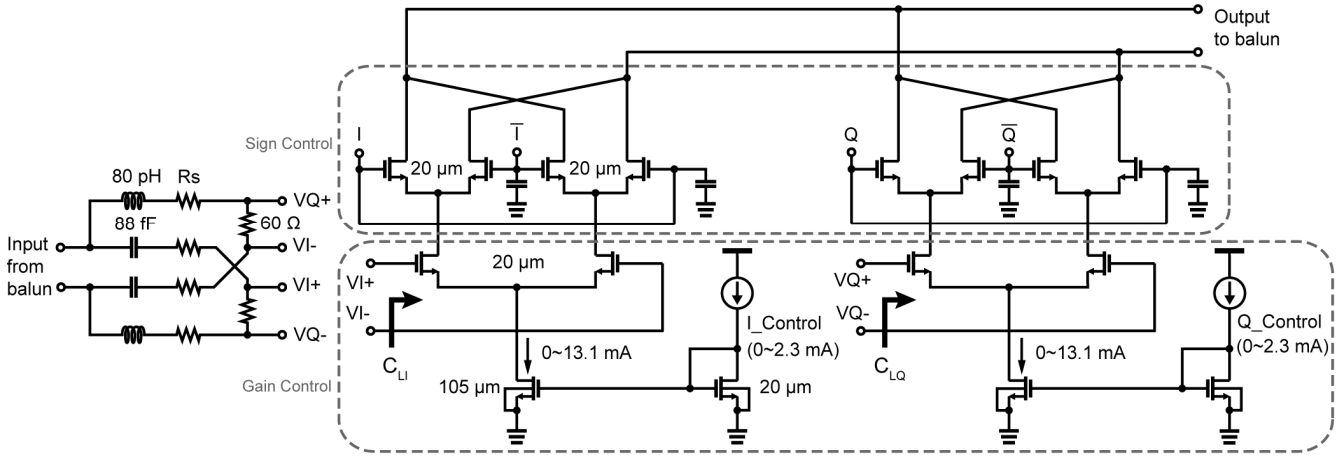

Fig. 2. Circuit schematic of the active phase shifter. (bias circuits not shown).

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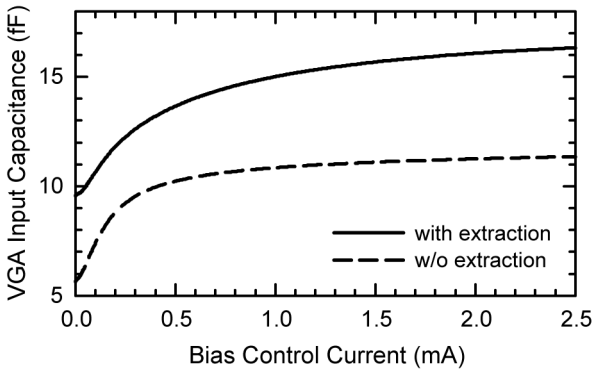

Fig. 3. Simulated I (or Q) VGA input capacitance over current bias.

current (C_L is the single ended loading and is $2xC_{LI}$) and results in significant distortion in the amplitude and phase at the output of the I/Q network. Furthermore, the gain and phase imbalance is dependent on the capacitance difference, C_{LI}-C_{LQ}, and this means that for every phase setting (and different bias currents), there is a varying amplitude and phase error present at the vector modulator I/Q ports.

The inclusion of a series resistor Rs in the all-pass network can enhance the performance of the I/Q network under a large capacitance loading. Figs. 4ab present gain and phase imbalance vs. C_{LI}-C_{LQ} and for C_{LI}=C_{LQ}=13 fF. It is seen that for an Rs=15-20 Ω, the gain imbalance is 0-1 dB, while the phase imbalance varies from 5 to 17° for C_{LI}-C_{LQ}=+/- 6 fF. Fig. 4c presents the I and Q voltage gain of the I/Q network vs. Rs at 60 GHz and equal I and Q amplitudes can be obtained at Rs = 15 Ω.

Table 1 presents the simulated current distribution and input P_{1dB} of the vector modulator for different phase states in the 0-90° range with Rs=20 Ω. The *I* vector, chosen as a reference, is obtained under the bias condition of I,Q = 2.5,0 mA and a C_{LI}-C_{LQ} = +6 fF. On the other hand, the *Q* vector is obtained under the bias condition of I,Q = 0,2.5 mA and a C_{LI}-C_{LQ} = -6 fF. The vector modulator can still be designed under a (near) constant current consumption, but the penalty is a 4 dB variation in the gain and 5.5 dB variation in the P_{1dB}.

A microphotograph of the 60 GHz phase shifter is shown in Fig. 6. The input and output baluns are simulated using Sonnet EM and show a loss of 1 dB (input balun) and 2 dB (output balun) at 60 GHz. (Fig. 7) In this design, the primary coil is defined in the top metal layer and secondary coil uses the second metal layer. The 50 Ω transmission-line is built using 9/8/9 μm CPW lines in the top metal layers with a simulated loss of 0.75 dB/mm at 60 GHz.

The circuit design is based on the design kit transistor models with parasitic extraction using Mentor Graphic's Calibre tools and EM simulation using Sonnet EM for the connections between the top metal layer and the CMOS transistor, I/Q network, and interconnects. The simulated gain vs. phase state is shown in Table 1 (under constant total current with V_{DD}=1.5 V), and the simulated NF is 13 dB at 60 GHz. The phase shifter core occupies an area of 200x300 μm^2.

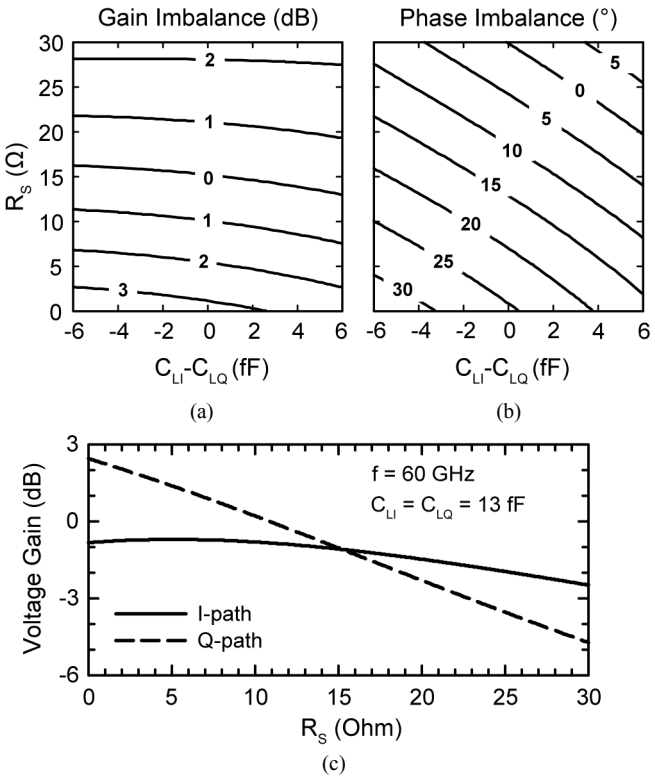

Fig. 4. Simulated 60 GHz (a) gain imbalance, (b) phase imbalance, and (c) voltage gain of the all-pass network vs. Rs and asymmetric capacitive loading. The simulation includes EM and parasitic extraction effects of the I/Q network and the input transistor stages.

III. MEASUREMENTS

Small-signal measurement is done with GSG probes with Agilent VNA. Fig. 7 presents the measured S_{21} – amplitude and phase. The frequency response shifted down to 54 GHz due to modeling and simulation inaccuracy. In this case, the external DACs were set so as to provide a constant total current and a 4 bit phase control. There is 4 dB gain variation in the measured response, as predicted by simulations. The measured phase response shows an RMS variation of 11-12°,

TABLE I
SIMULATED PERFORMANCE FOR SELECTED PHASE STATES

Phase State	I Bias (mA)	Q Bias (mA)	Gain (dB)	IP_{1dB} (dBm)	Power (mW)
0°	2.5	0	-4.0	1.3	22.2
22.5°	2.2	0.27	-7.3	6.0	22.6
45°	1.8	0.5	-7.7	5.0	21.6
67.5°	1.1	1.15	-6.3	1.4	21.9
90°	0	2.5	-3.7	0.6	22.1

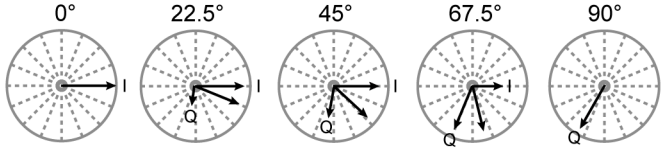

Fig. 5. Phasor diagram of selected phase states illustrating varying I/Q vectors over different phase states.

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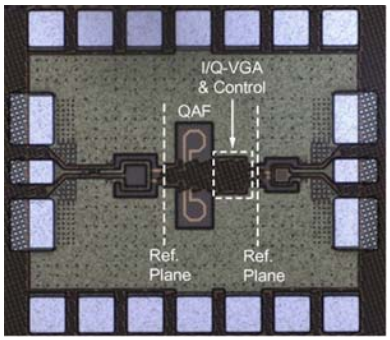

Fig. 6. Phase shifter chip microphotograph (750x680 μm^2 including pads).

meeting the 4-bit specification. Note the wideband response from 40-67 GHz which is due to Rs=20 Ω. To our knowledge, this is the widest band mm-wave phase shifter to-date. Finally, the measured input P_{1dB} at 55 GHz is shown in Fig. 8 and agrees with simulations.

V. Conclusion

This paper presented the first 45nm CMOS phase shifter optimized for 60 GHz operation. Careful analysis was done on the all-pass I/Q network and it was found that the inclusion of a series resistor greatly reduces the effect of the capacitance loading change vs. bias current (and phase state) and results in a wideband phase shifter under constant power conditions. The phase shifter consumes 23 mW for an input P_{1dB} of 0-3 dBm at 55 GHz.

Acknowledgments

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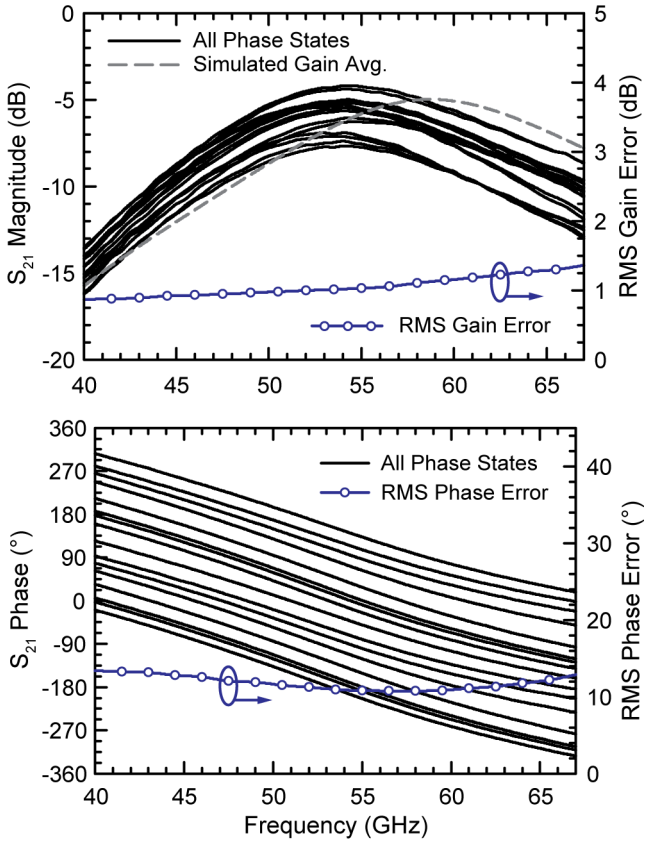

Fig. 7. Measured and simulated gain and phase response of 4-bit operation of the phase shifter

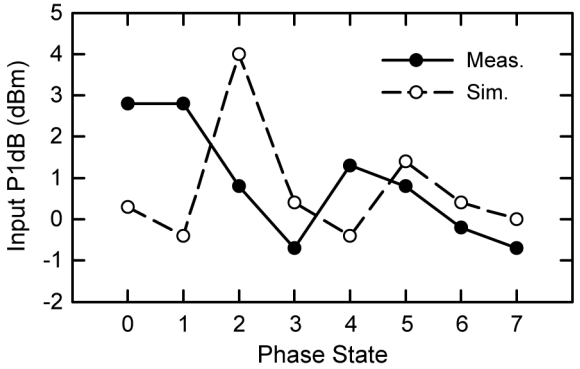

Fig. 8. Measured and simulatd input P1dB at 55 GHz 8 phase states in the 0 - 180° range (0, 22.5, 45, 90, 112.5, 135, 157.5)

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