Design and Analysis of a W-Band SiGe Direct-Detection-Based Passive Imaging Receiver

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***Abstract*—A W-band direct-detection-based receiver front-end for millimeter-wave passive imaging in a 0.18-μm BiCMOS process is presented. The proposed system is comprised of a direct-detection front-end architecture employing a balanced LNA with an embedded Dicke switch, power detector, and base-band circuitry. The use of a balanced LNA with an embedded Dicke switch minimizes front-end noise figure, resulting in a great imaging resolution. The receiver chip achieves a measured responsivity of 20–43 MV/W with a front-end 3-dB bandwidth of 26 GHz, while consuming 200 mW. The calculated NETD of the SiGe receiver chip is 0.4 K with a 30 ms integration time. This work demonstrates the possibility of silicon-based system-on-chip solutions as lower cost alternatives to compound semiconductor multi-chip imaging modules.**

***Index Terms*—Dicke switch, direct detection, low noise amplifier (LNA), passive imaging, power detector, radiometer, silicon-germanium.**

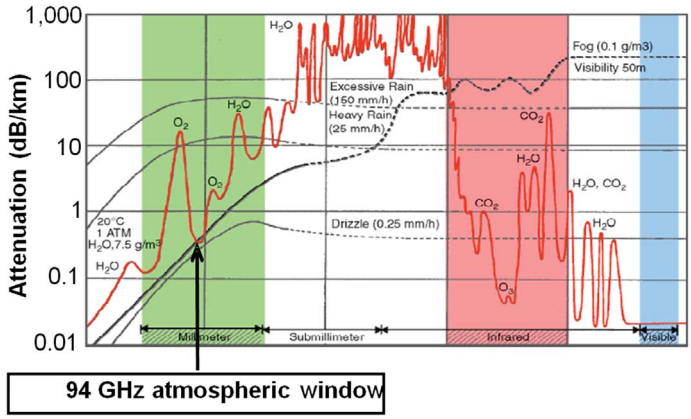

Fig. 1. Attenuation of atmospheric elements across frequency.

I. Introduction

A. Background

THE millimeter-wave (MMW) frequency range from 30–300 GHz has been an active area of research in the fields of high data-rate short-range wireless communication, sensing and radar, and active/passive imaging. In the area of imaging, passive MMW (PMMW) imaging presents a host of advantages compared to an active MMW imaging counterpart, making it a viable candidate for next generation in-vivo low-power sensing. At MMW frequencies, black body radiation is emitted at a nearly constant power spectral density (i.e., white spectrum), which is directly proportional to the temperature and emissivity of the radiating object (Rayleigh-Jeans law). Furthermore, low-attenuation atmospheric windows centered at frequencies of 35-, 94-, 140-, and 220-GHz exist (*cf.* Fig. 1), which provide transmission through obstacles such as clothing, smoke, dust, fog, and clouds. Applications ranging from concealed weapons detection, airplane navigation in low visibility conditions, and satellite surveillance have been targeted for imaging systems at these frequencies [1]. Traditionally, imagers operating at or above the W-band frequency range have been implemented in III-V semiconductor technologies, using a multi-chip system with a module-based level of integration [2]. Indeed, III-V technologies have been the desirable platform to achieve the MMW performance needed to enable sufficient thermal resolutions, typically on the order of 0.5 K [2], [3]. Recently, however, aggressive technology scaling has resulted in advanced silicon processes with f_T/f_{MAX} beyond 200 GHz, allowing them to compete with compound semiconductors in the MMW regime [4]–[6]. Specifically, the lower cost and higher level of circuit integration that silicon offers make it an attractive technology for future multi-antenna PMMW imaging systems, which require massive and sophisticated signal processing, provided that these silicon-based systems can meet the stringent imaging performance requirements.

B. Dicke Switch Architectures

The general equation for the thermal resolution, also known as noise-equivalent temperature difference (NETD), of a PMMW receiver is given by [7]

$$\mathrm{NETD} = T_{\mathrm{SYS}}\sqrt{\frac{1}{BW\cdot\tau}+\left(\frac{\Delta G}{G}\right)^2+\frac{1}{2\tau}\cdot\left(\frac{\mathrm{NEP}}{k_B\cdot G\cdot BW\cdot T_{\mathrm{SYS}}}\right)^2} \quad (1)$$

where T_{SYS} is the noise temperature of the receiver, BW denotes the bandwidth, τ is the back-end integration time, G is the pre-detection gain, ΔG is the rms variation of G, k_B is the Boltzmann constant, and NEP represents the noise equivalent power of the receiver [6]. ΔG is often the dominant term in

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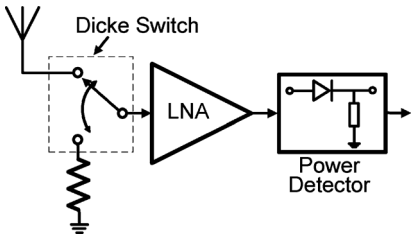

Fig. 2. Traditional Dicke switch architecture.

(1), and can degrade the NETD significantly. As an example, assume a receiver (RX) is designed with the achievable performance capabilities of 20 GHz bandwidth, 30 ms integration time, 30 dB pre-detection gain, and 5,500 K noise temperature. For such an RX, $\Delta G = 0$ would result in an excellent NETD of 0.2 K. However, an rms gain variation as small as 0.01 dB will increase the NETD by over an order of magnitude to 5.5 K. In order to alleviate this problem, a Dicke switch architecture [8] is commonly used.

A Dicke switch topology, shown in Fig. 2, uses a single pole double-throw (SPDT) switch at the input of the LNA in order to continuously switch the LNA input between the antenna and a calibrated reference load. The toggling frequency of the switch should be higher than the $1/f$ noise corner frequency of the RX. In this case, the two detected signals (antenna and reference) can be continuously subtracted, and the detector's output voltage contributions due to low-frequency gain fluctuations are canceled (i.e., $\Delta G \rightarrow 0$). Additionally, if the pre-detection gain block dominates the input referred noise temperature, the NETD can be reduced to [7]

$$\text{NETD} = 2 \cdot T_{\text{SYS}} \sqrt{\frac{1}{BW \cdot \tau}}. \tag{2}$$

The factor of 2 is present, because the Dicke switch is connected to the antenna for half of each cycle. A camera frame rate of 25 frames/s limits the maximum integration time to 40 ms, and further reduction in NETD can only be achieved by improvements in the front-end noise figure (NF) and bandwidth.

C. Traditional III-V Implementation

The goal of this work is to demonstrate the potential of silicon chips as a lower cost alternative to III-V-based imaging chipsets.

Typically, the Dicke switch is implemented as an SPDT switch (Fig. 2) using PIN diodes [3]. This traditional architecture has the drawback of the front-end NF being degraded by the insertion loss of the SPDT switch, which directly results in an increase in NETD. This is not a major problem in III-V technologies, due to the availability of low-loss PIN diode switches [9], and more recently zero-biased diode detectors [2]. However, silicon-based MMW switches exhibit unacceptably high insertion loss ($\sim$5 dB for an HBT switch in the SiGe technology used in this work). System-level analysis indicates that this 5-dB loss prior to the LNA will degrade the receiver NETD approximately by a factor of 3, as shown in Fig. 3. This degradation, coupled with the inherently high NF of silicon transistors, results in an NETD greater than 0.5 K (which is

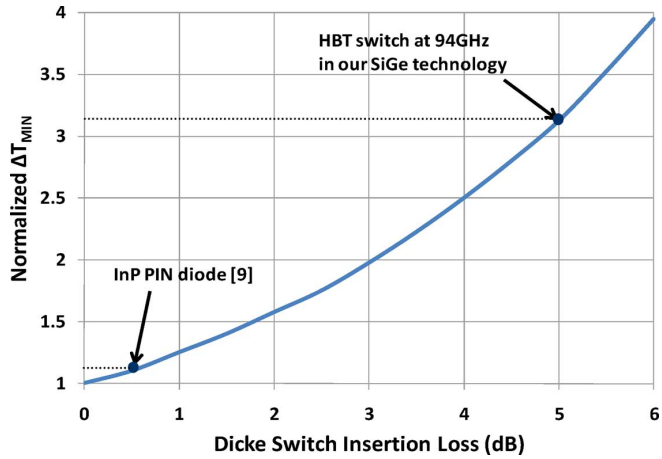

Fig. 3. NETD versus Dicke switch insertion loss.

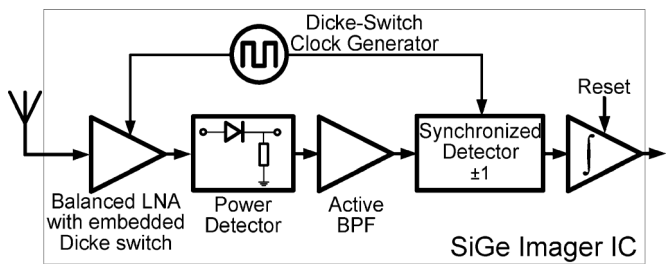

Fig. 4. Proposed SiGe imaging RX.

typically cited as the threshold for acceptable performance in indoor applications [2], [3]). As discussed next, the proposed front-end architecture in Figs. 4 and 5 eliminates the above problem by embedding the Dicke switch functionality within a balanced LNA, such that the switch insertion loss contributes minimal effect on the RX's NF. In this design, the insertion loss of the input coupler directly adds to the front-end NF. Fig. 6 compares the simulated NETD of three different embedded Dicke switch imaging systems designed in both a 65 nm CMOS and a 0.18 μm BiCMOS SiGe technology. Both technologies provide devices with $f_T/f_{\text{MAX}} = 200$ GHz. However, the MOSFET switches have 1 dB less insertion loss than the SiGe HBT switches. But at the same time, the SiGe technology provides a thicker top metal as well as thicker dialectic spacing between the top and bottom metals, which significantly reduces the insertion loss of the SiGe branch-line coupler. The simulation in Fig. 6 shows that the NETD is linearly related to the front-end insertion loss in dB for typical silicon RF performance. Utilizing this balanced LNA architecture, while minimizing the coupler loss, allows the imaging system to achieve the lowest possible NETD for a given technology. To demonstrate this, we have developed a single-chip highly-integrated MMW imaging RX operating in the W band (Fig. 4), fully utilizing the high level of integration that silicon offers.

D. Proposed SiGe RX Chip

As shown in Fig. 4, the imaging RX in this work is based on the direct-detection architecture, thus avoiding the use of mixers and complex LO generation/distribution required by a hetero-

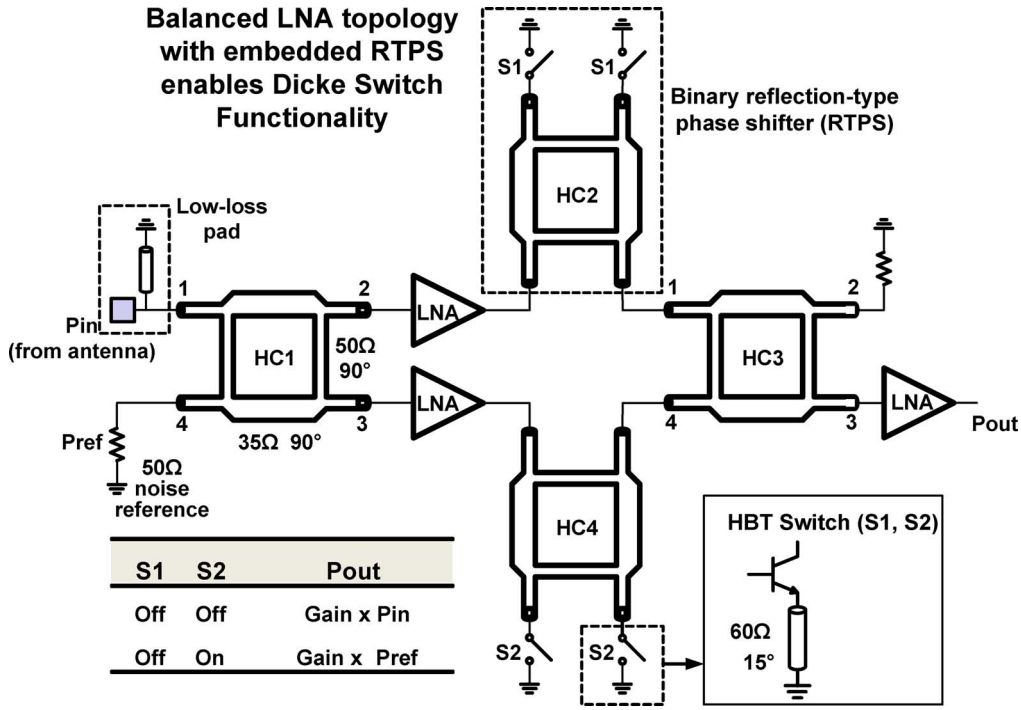

Fig. 5. Balanced LNA with embedded Dicke switch.

dyne detection scheme. This naturally results in a more compact and lower power RX. SiGe HBTs with $f_T/f_{\rm MAX} = 200$ GHz are used to design the on-chip Dicke switch, LNA, and square-law power detector. The baseband circuits, including the Dicke switch clock generator, are implemented using the 0.18-μm CMOS transistors available in the BiCMOS process without the use of any off-chip components.

The analysis and design carried out in this paper is an extension of the research published in [10]–[12].

II. Circuit Design and Analysis

A. Design and Analysis of Balanced LNA With Embedded Dicke Switch

Fig. 5 shows the schematic of the balanced LNA (BLNA) incorporating the embedded Dicke switch. Inspired by the GaAs topology first presented in [13], the circuit is primarily comprised of a balanced LNA with the addition of a reflection-type binary phase shifter in each branch. The operation of this BLNA can be understood using power-waves analysis [14]. Given the well-known s-parameter matrix of a branch-line coupler,

$$[S] = L_C \begin{bmatrix} 0 & \frac{-j}{\sqrt{2}} & \frac{-1}{\sqrt{2}} & 0 \\ \frac{-j}{\sqrt{2}} & 0 & 0 & \frac{-1}{\sqrt{2}} \\ \frac{-1}{\sqrt{2}} & 0 & 0 & \frac{-j}{\sqrt{2}} \\ 0 & \frac{-1}{\sqrt{2}} & \frac{-j}{\sqrt{2}} & 0 \end{bmatrix}$$

(L_C is the insertion loss of the branch-line coupler) and using the superposition principle, and assuming input power-waves on ports 1 (antenna port) and 4 (reference port) are expressed as

$$a_{\rm pin1} = a_{\rm IN1} \cdot e^{-j\theta_1}$$
$$a_{\rm pin4} = a_{\rm IN4} \cdot e^{-j\theta_4}$$

(where $a_{\rm IN,k}$ and $\theta_{\rm k}$ denote the amplitude and phase of the power wave at the kth port, respectively), we compute the signal magnitude and phase at each point in the BLNA. Note that for this case, the power wave $a_{\rm IN4}$ represents the noise power of the 50 Ω noise reference. Since the insertion loss L_C appears in both gain paths of the BLNA, the power waves of intermediate and output ports are all normalized to L_C throughout the power-waves analysis.

Port 2 of hybrid coupler HC1 will have the power-wave

$$\begin{aligned} a_{\rm pin2} &= (a_{\rm IN1} \cdot e^{-j\theta_1}) \cdot S_{21} + (a_{\rm IN4} \cdot e^{-j\theta_4}) \cdot S_{24} \\ &= -j\frac{a_{\rm IN1} \cdot e^{-j\theta_1}}{\sqrt{2}} - \frac{a_{\rm IN4} \cdot e^{-j\theta_4}}{\sqrt{2}} \end{aligned} \quad (3)$$

and port 3 of HC1 will have the power-wave

$$\begin{aligned} a_{\rm pin3} &= (a_{\rm IN1} \cdot e^{-j\theta_1}) \cdot S_{31} + (a_{\rm IN4} \cdot e^{-j\theta_4}) \cdot S_{34} \\ &= -\frac{a_{\rm IN1} \cdot e^{-j\theta_1}}{\sqrt{2}} - j\frac{a_{\rm IN4} \cdot e^{-j\theta_4}}{\sqrt{2}}. \end{aligned} \quad (4)$$

For the case when both phase shifters are in the same state, both power-waves go through identical paths consisting of LNA gain and phase shift as well as identical attenuation and phase shift due to the reflection type phase shifters (RTPS) in Fig. 5. Therefore, the power-wave at port 1 of HC3 will be

$$a_{\rm pout1} = -j\frac{G_{\rm LNA} \cdot L_{\rm RTPS} \cdot a_{\rm IN1} \cdot e^{-j(\theta_1 - \Phi)}}{\sqrt{2}} - \frac{G_{\rm LNA} \cdot L_{\rm RTPS} \cdot a_{\rm IN4} \cdot e^{-j(\theta_4 - \Phi)}}{\sqrt{2}}$$

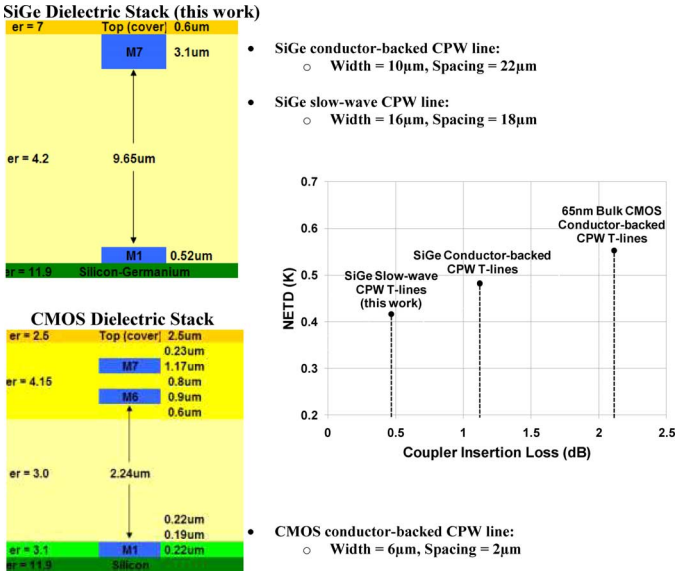

Fig. 6. Simulated NETD as a function of branch-line coupler insertion loss and RTPS insertion loss. Including practical design points for a 65 nm CMOS technology and the SiGe technology used in this work. The dielectric stacks for each technology and specific CPW widths and spacing are also shown.

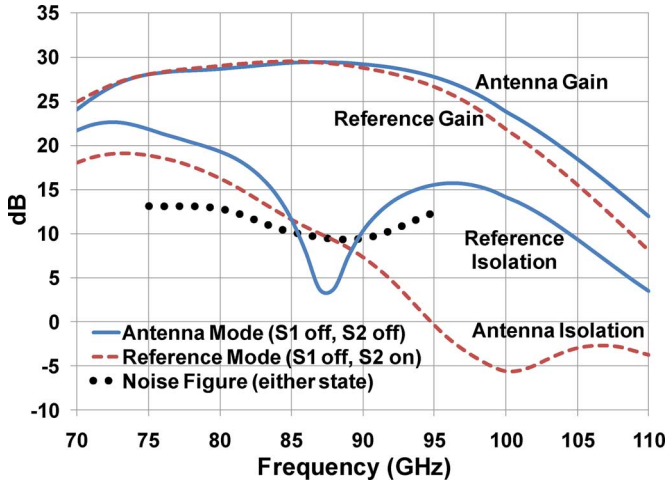

Fig. 7. Measured gain, NF, and isolation for the BLNA.

where G_{LNA} is the LNA's gain, L_{RTPS} denotes the RTPS's loss, and Φ represents the combined phase shift of both the LNA and RTPS. Similarly, the power-wave at port 4 of HC3 will be

$$a_{\mathrm{pout4}} = -\frac{G_{\mathrm{LNA}} \cdot L_{\mathrm{RTPS}} \cdot a_{\mathrm{IN1}} \cdot e^{-j(\theta_1-\Phi)}}{\sqrt{2}} - j\frac{G_{\mathrm{LNA}} \cdot L_{\mathrm{RTPS}} \cdot a_{\mathrm{IN4}} \cdot e^{-j(\theta_4-\Phi)}}{\sqrt{2}}.$$

We then use superposition to compute the power delivered to port 3 of HC3 (i.e., the output port),

$$\begin{aligned} a_{\mathrm{pout3}} &= G_{\mathrm{LNA}} L_{\mathrm{RTPS}} \left(\frac{a_{\mathrm{IN4}} \cdot e^{-j(\theta_4-\Phi)}}{2} + j\frac{a_{\mathrm{IN1}} \cdot e^{-j(\theta_1-\Phi)}}{2} \right) \\ &\quad + G_{\mathrm{LNA}} L_{\mathrm{RTPS}} \left(-\frac{a_{\mathrm{IN4}} \cdot e^{-j(\theta_4-\Phi)}}{2} + j\frac{a_{\mathrm{IN1}} \cdot e^{-j(\theta_1-\Phi)}}{2} \right) \\ &= G_{\mathrm{TOTAL}} \cdot a_{\mathrm{IN1}} \cdot e^{-j(\theta_1-\Phi-(\pi/2))} \end{aligned} \quad (5)$$

where G_{TOTAL} is the product of the LNA's gain and the RTPS's loss. As seen in (5), when the phase shifters are in the same state, only power incident at port 1 of HC1 (a_{IN1})is present at the BLNA's output port. However, when the phase shifters are in opposite states, one power-wave will experience an additional 180° phase shift. In this case, the power delivered to the output port is expressed as

$$\begin{aligned} a_{\mathrm{pout3}} &= G_{\mathrm{LNA}} L_{\mathrm{RTPS}} \left(-\frac{a_{\mathrm{IN4}} \cdot e^{-j(\theta_4-\Phi)}}{2} - j\frac{a_{\mathrm{IN1}} \cdot e^{-j(\theta_1-\Phi)}}{2} \right) \\ &\quad + G_{\mathrm{LNA}} L_{\mathrm{RTPS}} \left(-\frac{a_{\mathrm{IN4}} \cdot e^{-j(\theta_4-\Phi)}}{2} + j\frac{a_{\mathrm{IN1}} \cdot e^{-j(\theta_1-\Phi)}}{2} \right) \\ &= G_{\mathrm{TOTAL}} \cdot a_{\mathrm{IN4}} \cdot e^{-j(\theta_4-\Phi-\pi)} \end{aligned} \quad (6)$$

which shows that when phase shifters are in opposite states, only power from the 50 Ω reference resistor ($a_{\mathrm{IN_4}}$) is delivered to the output port. By toggling between these two states, the desired chopping operation of the Dicke switch is achieved. It can also be shown that when the phase shifters are in opposite states, power from port 1 of HC1 is dissipated in the 50 Ω resistor connected to port 2 of HC3.

To analytically compare NF performance of the BLNA in Fig. 5 with that of the traditional LNA+switch in Fig. 2, suppose that each LNA stage in Fig. 5 exhibits a gain of G_{LNA}. The noise factor of the LNA+switch $F_{\mathrm{SW\text{-}LNA}}$ in Fig. 2 is readily expressed as

$$F_{\mathrm{SW\text{-}LNA}} = L_{\mathrm{SW}} F_{\mathrm{LNA}} \quad (7)$$

where L_{SW} represents the linear loss of the Dicke switch, and F_{LNA} represents the noise factor of the LNA in Fig. 2. The noise factor of the BLNA with embedded Dicke switch is found to be

$$F_{\mathrm{BLNA}} = L_C F_{\mathrm{LNA}} \left(1 + \frac{L_C L_{\mathrm{RTPS}} - 1}{G_{\mathrm{LNA}} + 1} \right). \quad (8)$$

The loss of the hybrid couplers are 2–3 times (∼ 4 dB) lower than that of SPDT switches. The improvement in noise factor is

$$IM_F = \frac{F_{\mathrm{SW\text{-}LNA}}}{F_{BLNA}} = \frac{L_{\mathrm{SW}}}{L_C \left(1 + \frac{L_C L_{\mathrm{RTPS}} - 1}{G_{\mathrm{LNA}} + 1} \right)}. \quad (9)$$

Assuming 20 dB gain for each LNA; and 6.5- and 6-dB losses for RTPS and Dicke switches, respectively, and 0.5 dB loss for hybrid coupler, approximately 2.5 dB improvement in NF will be achieved. ■

Fig. 7 shows the measured gain and isolation from the antenna and reference ports for the two different phase-shifter states. As expected, when both phase shifters are in the same state, the signal from the antenna is amplified while the reference signal is suppressed. Conversely, when the phase shifters are in opposite states, the reference input is amplified, while the antenna signal is suppressed. Note that the balanced structure ensures equal gains in both the antenna and reference modes. An additional LNA is used after the balanced structure in order to achieve a

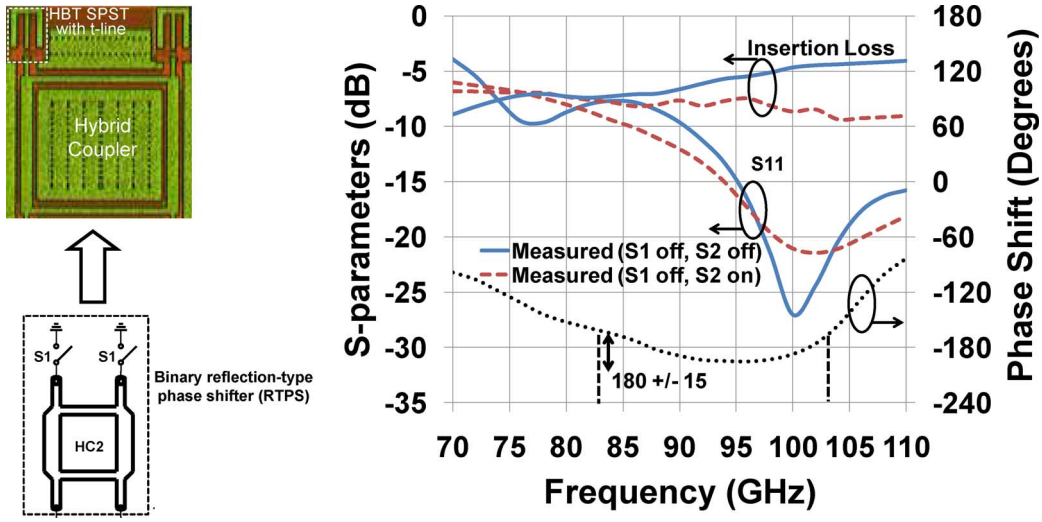

Fig. 8. Measured RTPS S-parameters and phase-shift.

total pre-detection gain of 30 dB, as can be seen in Fig. 7. Note that within the bandwidth of interest, the antenna and reference gains closely follow each other. Fig. 7 also indicates the measured NF of the BLNA. The proposed BLNA with embedded Dicke switch achieves a minimum NF of around 9.7 dB.

The BLNA with embedded Dicke switch uses four couplers and three 5-stage LNAs. The LNA in a conventional SPDT structure would use two 5-stage LNAs to achieve almost the same pre-detection gain, and therefore, will consume smaller chip area. Nevertheless, the BLNA, by virtue of its design, is able to achieve the required NETD for indoor imaging applications. On the other hand, the SPDT architecture (in currently available SiGe technology) essentially cannot. The use of a switch in front of the LNA in the conventional SPDT approach degrades the system noise temperature, and therefore NETD [see (2)]. It should also be noted that the layout in this work was done conservatively in order to avoid high-frequency EM coupling and to ensure first-pass success. A more aggressive layout approach (e.g., avoiding the use of quarter-wavelength bias-chokes) can be used to reduce the chip area.

B. Reflection-Type Phase-Shifter Design

The RTPS structure of Fig. 8 was chosen because it provides broadband input and output matching. Additionally, the RTPS phase shift stays within $\pm 10\%$ of 180° for the majority of the W-band. Fig. 8 shows the measured s-parameters as well as measured phase shift for the RTPS structure. The input and output return losses as well as insertion loss of this structure for both possible switch-state operations have been measured. The output return loss was measured to be identical as the input return loss (due to the symmetric nature of the RTPS), and therefore, was not included in Fig. 8. The insertion loss for both operation states is better than -8 dB from 73–100 GHz, which is approximately 2 dB higher than a traditional HBT-based SPDT switch for the technology used in this work. It should be noted, however, that this loss comes after 20 dB of LNA amplification, and therefore, does not contribute to front-end NF as a conventional Dicke-switch architecture would.

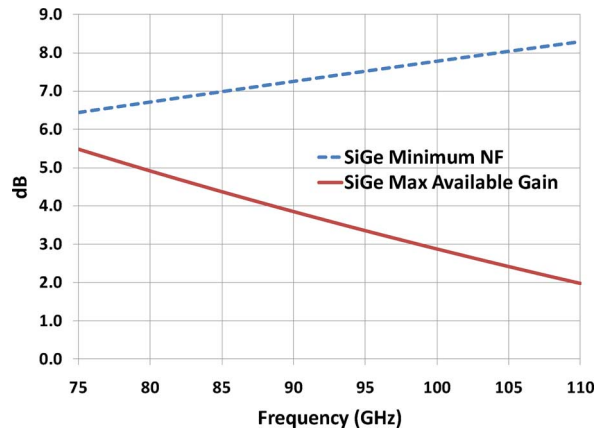

Fig. 9. MAG and NFMIN for the device used in this work across the W band.

C. Five-Stage LNA Design and Analysis

Fig. 9 shows the maximum available gain (MAG) and minimum achievable NF ($\mathrm{NF_{min}}$) of a common-emitter HBT in the technology used in this work. The device is optimally sized and biased such that it achieves the lowest $\mathrm{NF_{min}}$ for this technology. Simulations of a single HBT at 90 GHz show a MAG of 3.9 dB and an $\mathrm{NF_{min}}$ of 7.2 dB. A multi-stage amplifier designed in this technology, therefore, incorporates a first amplifier stage whose gain will not be high enough to significantly reduce the NF contribution of the subsequent stages. Using the well-known Friis equation for the cascaded NF of a multi-stage amplifier, along with the transistor's MAG and $\mathrm{NF_{min}}$ values, the effect of the latter gain stages on the overall LNA NF can be estimated. It turns out that the second stage will add at least 1.2 dB to the overall LNA's NF. Adding a third and a fourth stage will contribute 0.4 and 0.1 dB to the overall NF respectively, resulting in theoretical four-stage MAG and $\mathrm{NF_{min}}$ of 15.6 dB and 9.0 dB. The previous analysis assumes that each stage achieves maximum gain and minimum NF. However, by design, the first stage of an LNA will trade off a certain amount of available gain in order to achieve the best possible noise match at the input. This, along with loss in

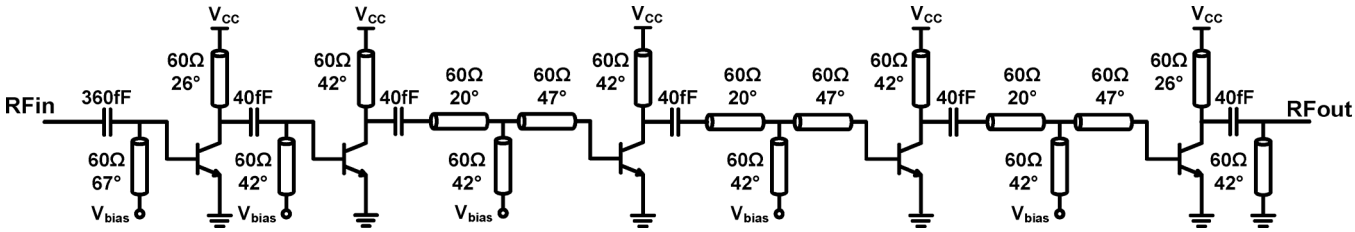

Fig. 10. Five-stage LNA schematic.

the matching networks, necessitates the use of a fifth gain stage in order to achieve the desired 15-dB LNA gain for this work. The fifth stage has a negligible (< 0.1 dB) contribution to the LNA NF.

The five-stage common-emitter LNA schematic is shown in Fig. 10. The input matching networks of the first two stages (i.e., the high-pass L- and the π-match networks at the input ports of the first and the second CE stages) are designed to achieve minimum NF. These high-pass matching networks reduce the power gain at lower frequencies, where the HBT transistors exhibit naturally high gain, which helps the LNA's stability. Furthermore, it is desirable to keep the topologies of these matching networks as compact as possible in order to minimize any pre-gain losses, which will otherwise contribute to higher NF. To achieve the above goals, a different design methodology compared to standard silicon-based techniques for obtaining simultaneous power and noise match (presented in [15]) is used. Specifically, due to the low gain of the HBTs in the W-band, inductive emitter degeneration is not employed, thereby avoiding the associated reduction in gain. First, the current density which minimizes the HBT's $\mathrm{NF}_{\min}$ is obtained. In HBT LNAs, as opposed to CMOS LNA's, maximizing f_T will not necessarily result in minimizing $\mathrm{NF}_{\min}$. This is because, in HBT devices, an increase in bias current will lead to significantly higher shot-noise. The minimum $\mathrm{NF}_{\min}$ is thus achieved at a bias current lower than that for maximum f_T. The location of the optimum source reflection coefficient, Γ_{opt}, for noise match is plotted on the Smith chart, along with the device unmatched input reflection coefficient Γ_{IN}. The device size is then swept such that Γ_{opt} moves sufficiently close to the 50 Ω point on the Smith chart, while at the same time, Γ_{IN} moves to the same resistance (or conductance) contour as Γ_{opt}. This choice of the device size will only require a single stub at the input in order to move the device Γ_{IN} towards Γ_{opt}, thereby achieving excellent noise and impedance match.

Following the methodology described above, an optimum HBT emitter area of 0.75 $\mu\mathrm{m}^2$ is found. Fig. 11 indicates simulated Γ_{IN}, Γ_{opt}, and the 7.3-dB NF circle (which intersects the 50 Ω point on the Smith chart). As shown in Fig. 11, Γ_{opt} is located on the circle with a constant VSWR of 1.4:1, which corresponds to -15-dB input return loss. A short-circuited stub at the input moves Γ_{IN} along a constant conductance contour such that it achieves an input noise match within 0.1 dB of $\mathrm{NF}_{\min}$, and an input return loss of -15 dB at 90 GHz.

Starting with the output of the second gain stage, all subsequent interstage matching networks employ a more complex T-match network topology realized using transmission lines (t-lines). This matching network offers more degrees of freedom than a single-stub matching network, and therefore,

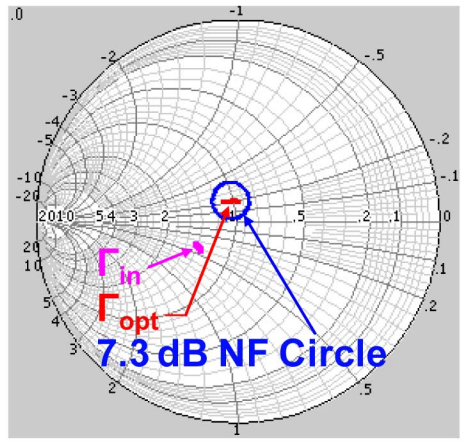

Fig. 11. ΓIN, ΓOPT, and a 7.3 dB NF circle.

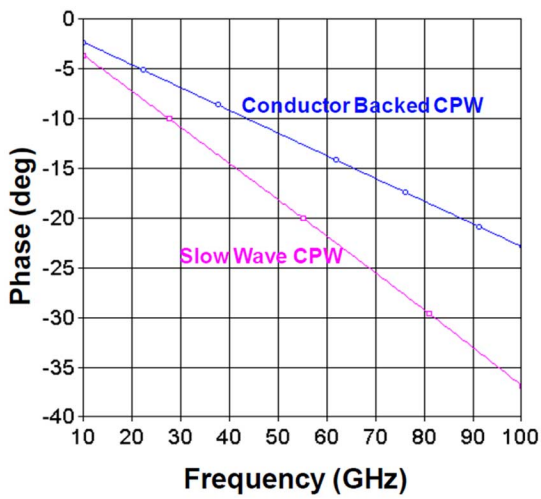

Fig. 12. Phase shift of a conductor backed CPW and SW-CPW (both 100 μm long).

enables conjugate matching between the output of each stage and the input of the subsequent stage over a larger bandwidth than a single-stub matching network. As a result, maximum power transfer, and hence maximum gain, from the last three stages will be achieved. The insertion loss of the t-lines in the T-match should be minimized, since this loss will reduce the amplifier gain. To this end, t-lines were implemented as slow-wave coplanar waveguide (CPW) structures [16]. EM simulations in Fig. 12 show that at 90 GHz, a slow-wave CPW (SW-CPW) t-line achieves roughly 60% higher phase-shift compared to standard conductor-backed CPW t-lines, for a

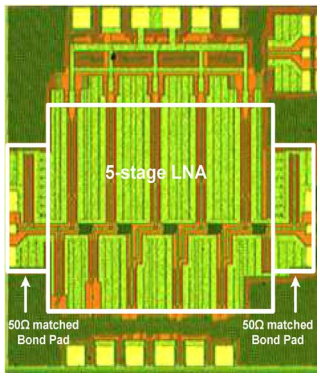

Fig. 13. Die photo of the five-stage LNA.

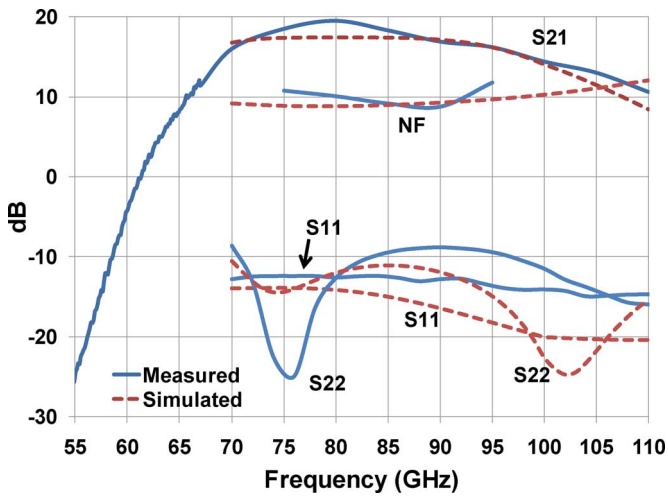

Fig. 14. Measured and simulated five-stage LNA performance.

given length. This translates to reduced loss of the matching networks, as well as reduced chip area.

A standalone test structure of the five-stage LNA was fabricated. Fig. 13 shows the chip microphotograph of the five-stage LNA breakout circuit. The layout has been carefully designed to avoid parasitic feedback across each LNA stage. In particular, every input and output matching stub alternate their orientation in the layout in order to minimize EM coupling between the t-lines, and further stabilize the LNA. The simulated LNA k-factor was consistently greater than 10 across the W-band.

On-wafer LNA s-parameters were measured using a VNA with W-band frequency extenders. The VNA measurement results in Fig. 14 are in good agreement with both theory and simulation, and show a peak gain of 19 dB at 80 GHz, and better than -12 dB input return loss and -9 dB output return loss from 70 to 110 GHz. NF measurements, shown in Fig. 14, were performed using a spectrum analyzer (Agilent E4448A) and an external down-converter. The NF was only measured up to 95 GHz due to limitations of the external down-converter. The input and output ports of the LNA were probed with a spectrum analyzer, and no oscillations were observed in the frequency range from 1- to 110-GHz, verifying the stability of the design. The core five-stage LNA draws 35-mA of current from a 1.8-V supply and consumes 1.0 mm^2 of chip area.

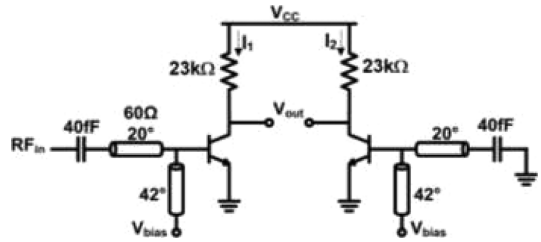

Fig. 15. W-band power detector schematic.

D. Detector Design and Analysis

The operation principle of a power detector in a direct-detection architecture is to convert the MMW input power to a constant output voltage. Therefore, a linear relationship between input power and output voltage needs to be established. This necessitates that the detector should operate in the square-law region. The detector in this work consists of a pair of common-emitter HBTs, as shown in Fig. 15. The HBTs are biased via current mirrors and the MMW signal is applied to the base of one of the HBTs. The DC output voltage is taken differentially at the two collectors. Assuming the input signal is a sinusoidal wave with frequency f and amplitude $V_{\rm im}$, the output voltage is expressed as

$$\begin{aligned} V_{\rm OUT} &= R \cdot (I_1 - I_2) \\ &= R \cdot I_S e^{V_{\rm BE,ON}/V_T} \left(e^{V_{\rm im}\cos(2\pi f t)/V_T} - 1 \right) \end{aligned} \quad (10)$$

where $V_{\rm BE,ON}$ is the bias voltage at the base, $V_T = kT/q$ is the thermal voltage, and R is the load resistor. Expanding (10) using Taylor series, while truncating higher order terms and leaving the DC output, $V_{\rm OUT}$ becomes approximately equal to

$$V_{\rm OUT} \approx I_{\rm DC} R \frac{V_{\rm im}^2}{4V_T^2} = I_{\rm DC} R \frac{2 \cdot |Z_{\rm IN}| \cdot {\rm Re}\left(\frac{Z_{\rm IN}}{Z_{\rm IN}+R_S}\right) \cdot P_{\rm IN}}{4V_T^2} \quad (11)$$

where $I_{\rm DC}$ is the DC current in each branch, $P_{\rm IN}$ is the input power, R_S is the source resistance, and $Z_{\rm IN}$ is the input impedance of the HBT.

An important detector figure-of-merit for imaging applications is the responsivity, which measures the change in detector output voltage per unit input power. From (11), the responsivity β can be calculated as

$$\beta = \frac{V_{\rm OUT}}{P_{\rm IN}} = \frac{I_{\rm DC} R \cdot |Z_{\rm IN}| \cdot {\rm Re}\left(\frac{Z_{\rm IN}}{Z_{\rm IN}+R_S}\right)}{2V_T^2} = \alpha I_{\rm DC} R \quad (12)$$

where α (in W^{-1} units) accounts for MMW power transfer due to the input matching network. As can be inferred from (12), the responsivity is proportional to the DC current and the load resistor, and inversely proportional to the square of the temperature.

The load resistor and HBT device generate three major types of noise at the detector output: shot noise, thermal noise and flicker noise. Since the Dicke switch is necessarily designed to modulate the PMMW signal above the technology's 1/f corner

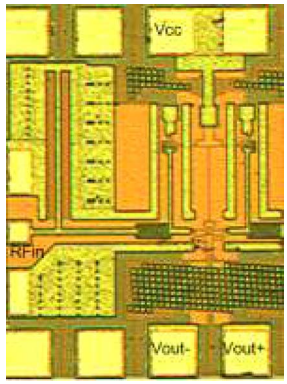

Fig. 16. Die photo of the detector test structure.

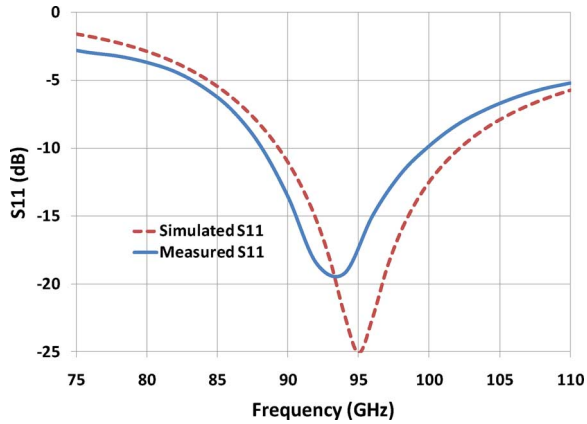

Fig. 17. Simulated and measured detector input return loss.

frequency, flicker noise can be ignored. The output noise power density is then readily expressed as

$$\frac{\overline{V_n^2}}{\Delta f} = 2qI_{\rm DC}R^2 + 4kTR. \tag{13}$$

The detector NEP is defined as the minimum input power required for a signal-to-noise ratio of unity at the detector output. From (12) and (13), the NEP (in $\mathrm{W/Hz^{1/2}}$) is obtained as

$$\mathrm{NEP} = \frac{\sqrt{\frac{\overline{V_n^2}}{\Delta f}}}{\beta} = \frac{\sqrt{2qI_{\rm DC}R^2 + 4kTR}}{\alpha I_{\rm DC}R} = \frac{1}{\alpha}\sqrt{\frac{2q}{I_{\rm DC}} + \frac{4kT}{I_{\rm DC}^2 R}}. \tag{14}$$

The foregoing analysis provides design insights for a differential HBT-based detector. Most notably, increasing the voltage drop across the load resistor will enhance both the responsivity and the NEP so long as the HBT stays in the forward-active region. Taking this design trend into account, the detector in Fig. 15 is biased to have a collector current of 42 μA and a load resistance of 23 kΩ. As seen in Fig. 15, an input matching network is also used in order to deliver maximum power to the detector input and provide a 50 Ω matched termination at the LNA output.

A detector test structure was fabricated as shown in Fig. 16. The detector $\mathrm{S_{11}}$ was measured using a VNA with W-band frequency extenders. Fig. 17 shows measured and simulated $\mathrm{S_{11}}$. The detector's responsivity has been measured using a coherent test setup, consisting of a signal generator as a variable input power source and an oscilloscope to measure the output voltage changes. The output spot noise power of the detector was measured using a spectrum analyzer at 1 MHz frequency (the frequency of our Dicke switch). A low frequency, low noise pre-amplifier (SRS 552) manufactured by Stanford Research Labs was used to boost the detector output noise power. Fig. 18 shows the detector test setup for both responsivity and noise performance. The input signal to the DUT was AM modulated at a rate of 100 kHz (which is roughly the same as the $1/\mathrm{f}$ corner frequency in this technology) to effectively emulate the functionality of a Dicke switch. Additionally, the input power was kept below -40 dBm to ensure the detector output is not compressed. The measured peak coherent responsivity, depicted in Fig. 19, is 11 kV/W. From the measured responsivity and output rms noise voltage (assuming a 1 Hz bandwidth centered at the Dicke switch frequency), a minimum NEP of 5 $\mathrm{pW/Hz^{1/2}}$ is reported (*cf.* Fig. 19). The detector occupies 0.6×0.75 mm^2 of chip area (including bond pads), and dissipates 76 μW of power.

III. Radiometer Measurement

A. Five-Stage LNA With Power Detector

A standalone test structure consisting of the core five-stage LNA cascaded with the W-band power detector has also been fabricated and tested. Similar to the testing of the power detector, the test setup utilizes a signal generator with pulse amplitude modulation (100% depth at a 100 kHz rate) in order to mimic the functionality of a Dicke switch. Fig. 20 shows the die photo of the core LNA plus power detector. Fig. 21 demonstrates the measured and simulated responsivity and NEP versus frequency, respectively, where measurements track simulations across the LNA's bandwidth.

The LNA+detector has a measured peak responsivity of 600 kV/W and a minimum NEP of 0.1 $\mathrm{pW/Hz^{1/2}}$. The average NEP across the bandwidth is 0.21 $\mathrm{pW/Hz^{1/2}}$, resulting in a calculated NETD of 5.5 K (assuming an external Dicke switch and 30 ms integration time). To achieve the desired NETD of less than 0.5 K, additional pre-detection gain is required in order to reduce the noise contribution of the detector. Therefore, the fully integrated system-on-chip passive imager exhibits 30 dB of BLNA gain, reducing the NETD to less than 0.5 K. Fig. 22 demonstrates how the LNA performance affects the NETD for several different semiconductor technologies, given a fixed detector's NEP performance.

B. Integrated SiGe Passive Imager

Fig. 23 shows the SiGe imaging RX chip micrograph. The power detector is followed by an active bandpass filter (Fig. 24) with an in-band gain of 20 dB and bandwidth of 0.1–10 MHz, which captures the first 9 harmonics of the detector's output square-wave. The active BPF is comprised of a fully differential op-amp with common mode feedback, and is placed in a bandpass feedback configuration. The op-amp has an open loop gain of 60 dB and 70° phase margin while dissipating 10-mW of DC power. As mentioned before, all feedback capacitors are implemented using standard on-chip MIM capacitors in the SiGe process, which provides a capacitance density of 2.0 $\mathrm{fF/\mu m^2}$.

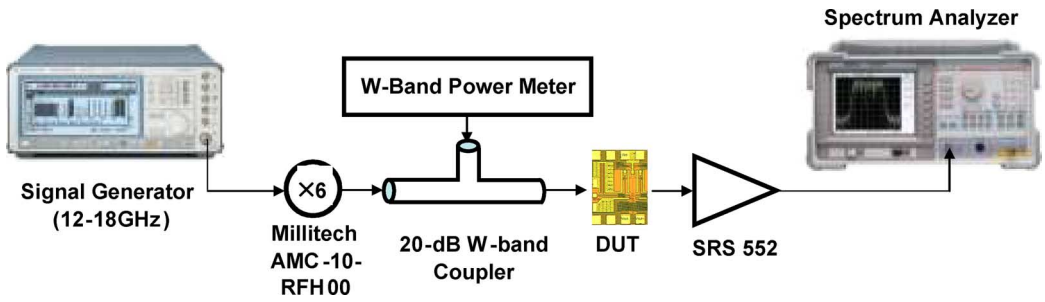

Fig. 18. Test setup for detector's NEP and responsivity measurements.

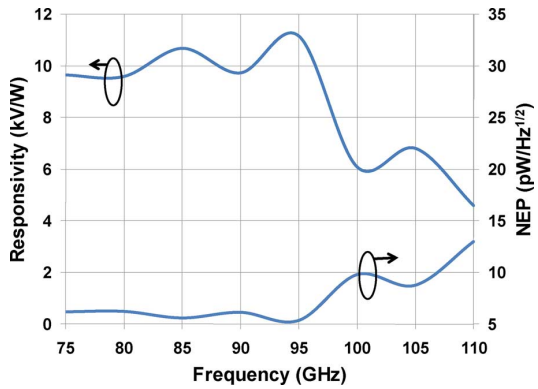

Fig. 19. Measured detector's responsivity and NEP.

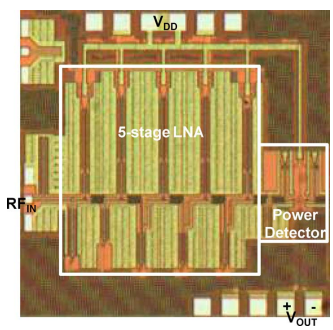

Fig. 20. LNA+detector test structure.

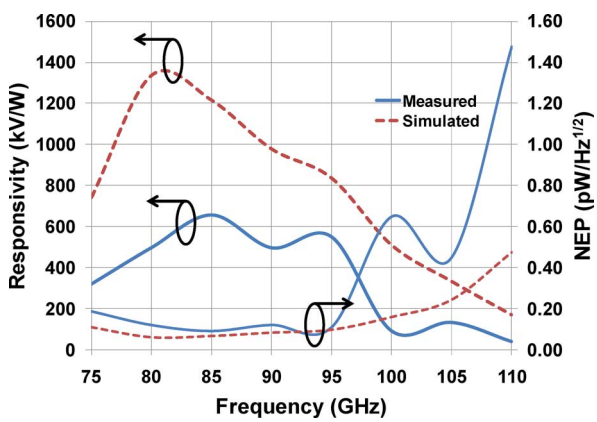

Fig. 21. Measured and simulated LNA+detector responsivity and NEP.

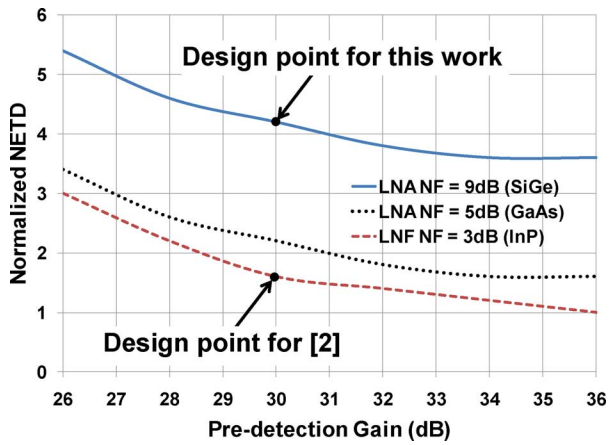

Fig. 22. Simulated NETD versus LNA performance.

The Dicke switch clock generator is realized as a four-stage differential ring oscillator, which generates a 1-MHz square wave with peak-to-peak amplitude of 0.5 V. Local switch drivers are used to buffer the clock, providing a full rail-to-rail swing for the RTPS and synchronized demodulator clock inputs. The clock generator consumes 0.9 mW of DC power.

Following the active BPF, a synchronized demodulator is used to convert the square wave voltage signal into a true DC voltage level. Since both the clock and the baseband have been designed in a fully-differential manner, the synchronized detector is readily implemented as a complementary combination of CMOS pass transistor switches in a passive-mixer configuration (Fig. 24), which dissipates no DC power.

The integrator in the baseband circuit is realized with the same op-amp core previously used in the active BPF. The integrator has a maximum differential output voltage swing of 0.6 V. Reset switches are driven by an off-chip pulse generator, such that the integration time can be varied.

In order to evaluate the passive imaging RX performance, relevant imaging parameters have been measured on wafer, with a system integration time of 30 ms. The responsivity of the RX chip is estimated by measuring the integrator's output voltage with the Dicke switch activated. A baseline calibration is performed before the responsivity measurement in order to estimate the input noise temperature when no signal is applied. Fig. 25 shows measured responsivity and NEP versus frequency of the passive imaging RX. The RX achieves a responsivity of 20–43 MV/W across the W-band. The minimum NEP of the imaging system is 10 $\mathrm{fW}/\mathrm{Hz}^{1/2}$, which is almost 10 times lower than that of the five-stage-LNA+detector. The reason is because the entire integrated imager employs the BLNA of Fig. 5 whose gain is 11 dB higher than that of the five-stage LNA. Although

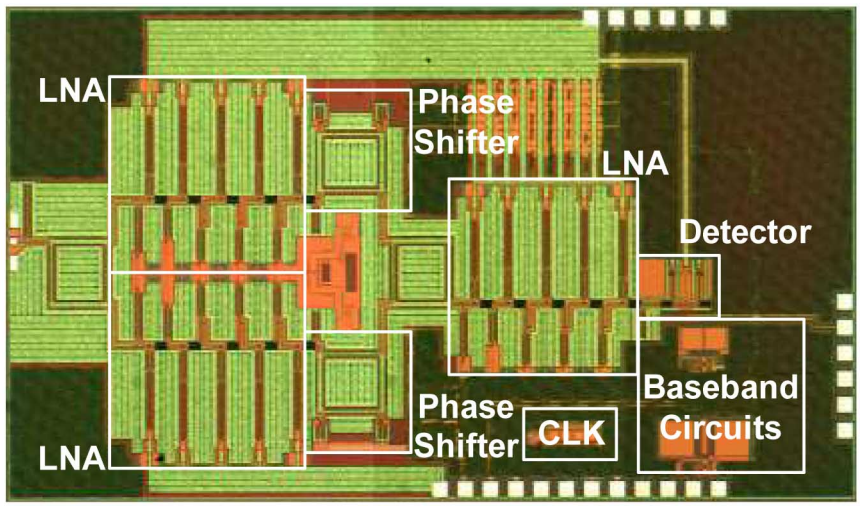

Fig. 23. SiGe imaging RX chip micrograph.

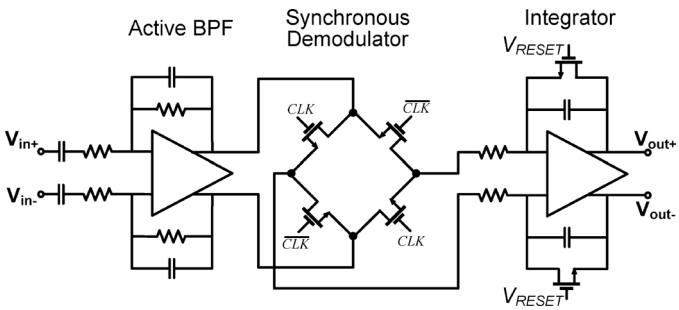

Fig. 24. Schematic of the baseband chain.

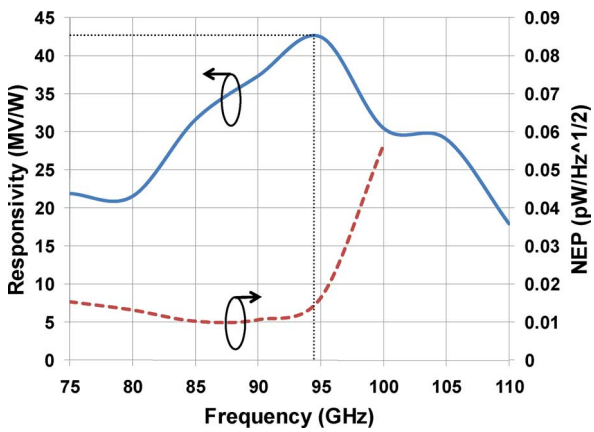

Fig. 25. Measured system responsivity and NEP.

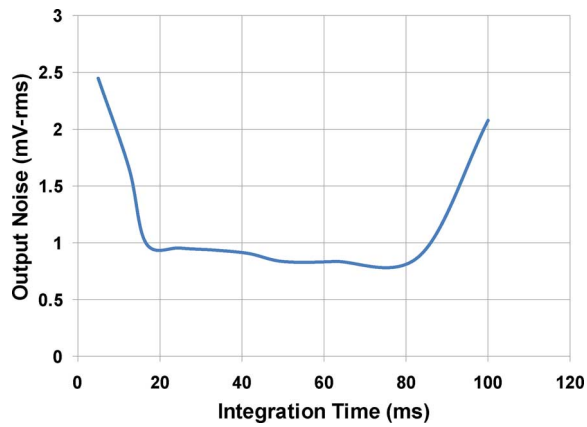

Fig. 26. Allan time measurement.

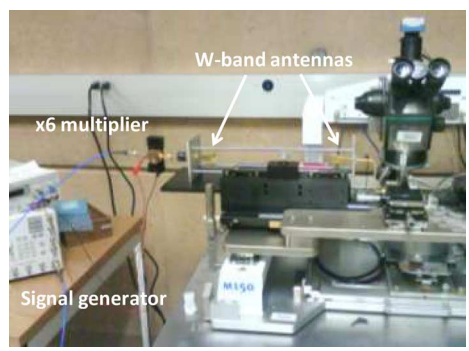

Fig. 27. Imaging test setup.

the base-band op-amp increases the signal level as well as the output noise, the improvement in NEP is primarily due to higher front-end gain.

Assuming the increased front-end gain due to the BLNA allows the BLNA's NF to dominate the system noise temperature, (2) can be used to calculate NETD. With this method, we calculate an NETD of 0.4 K. Using the average measured system NEP of 20 $\mathrm{fW/Hz^{1/2}}$ (*cf.* Fig. 25) and (1), the calculated NETD is reported to be 0.46 K. This slight increase shows the effect of the detector and baseband circuits on the input system noise temperature. Both calculations result in numbers that meet practical imaging requirements. Since the BLNA's gain is 11 dB higher than that of the five-stage LNA, the NETD of the entire imager is improved by roughly 13 times compared to 5.5 K NETD for the five-stage-LNA+detector.

Although the NETD can be improved by increasing the integration time according to (1) and (2), this improvement is upper-limited by the $1/f$ noise corner of the passive imaging

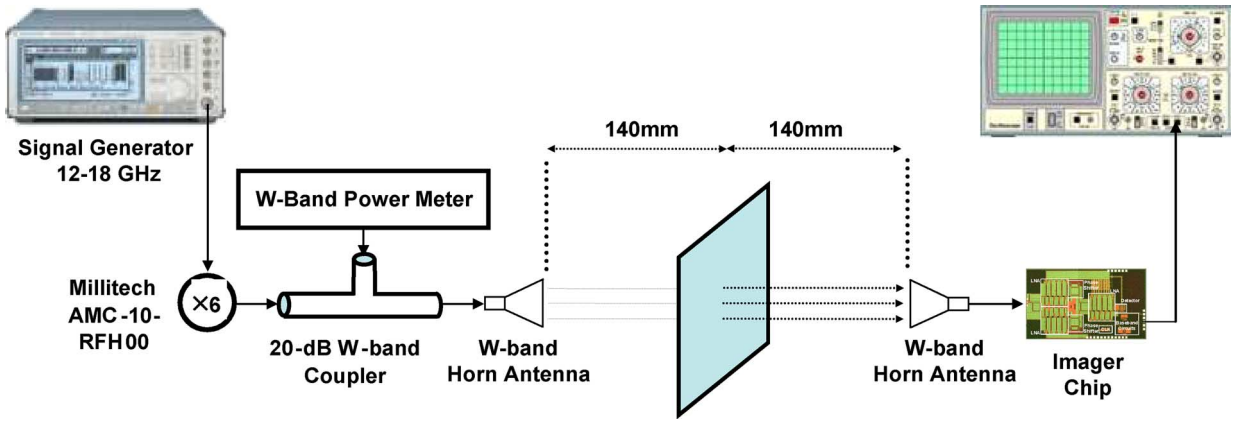

Fig. 28. Imaging test setup diagram.

receiver. Increasing the integration time continues to improve the NETD until the $1/f$ noise falls within the time-constant of the integrator, after which there will be degradation in NETD. It is thus important to characterize the RX with respect to integration time, in order to ensure it is operating at a point where the output noise voltage is at a minimum. An Allan time measurement [17] has been performed to characterize the RX's output noise with respect to integration time (Fig. 26). This measurement is performed by placing the imaging RX in a non-Dicke-switch mode of operation so that the $1/f$ noise's contribution to output noise voltage becomes relevant. The output noise voltage is measured with various integration times. This measurement determines the bounds of integration times allowed to attain the minimum NETD. As seen in Fig. 26, the RX output noise voltage decreases, as integration time is increased. This is expected due to the fact that the integrator's bandwidth will decrease, thereby attenuating more out-of-band noise at the integrator's input (which comes from all preceding circuits in the RX chain). While at the same time, the periodic integration/reset time is fast enough that the low frequency (i.e., slowly varying) $1/f$ noise contribution to the integrator's output noise voltage is largely reduced. As the integration time is increased beyond 80 ms, the large $1/f$ noise present at the integrator's input will fall within the integrator's bandwidth and begin to dominate the smoothing effect of the integrator, causing an increase in output noise voltage, as observed. It should be noted that for the Allan time measurement the RX system was not operating in a Dicke switched mode, as proper Dicke switch operation is not affected significantly by the $1/f$ noise corner of the technology. The chip design and SiGe process used in this work result in a minimum and approximately flat output noise voltage between 20 and 80 ms of integration time, covering the typical PMMW integration times of 30 to 40 ms.

Based on circuit measurements and (2) for NETD of a Dicke switch imager, the proposed SiGe PMMW receiver is capable of achieving sufficient temperature resolution for indoor applications in a passive mode. Due to limited sensitivity of available laboratory instrumentation, a source was required to illuminate the object being imaged (i.e., improve the SNR). More specifically, a black-body radiator at room temperature (297 K) yields approximately 261 mV at the output of the imaging RX. Assuming the black body temperature is increased by 0.5 K, the overall temperature will become 297.5 K, resulting in a system output voltage of 261.46 mV. However, the lab oscilloscope has a voltage resolution of 5 mV. As a result, the oscilloscope could not detect the temperature difference between an object at 297 K and an object at 297.5 K.

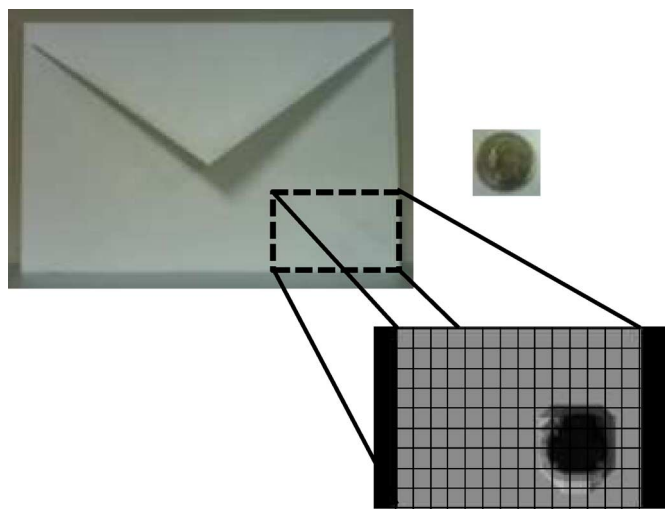

Fig. 29. Image of an envelope containing a coin in visible light and the MMW image.

Fig. 27 shows the lab setup for the line-of-sight active measurement of the passive imaging RX. A 12–18-GHz signal generator drives a x6 multiplier, providing a transmit power of -30 dBm at 90 GHz to a WR-10 horn antenna. The radiated power from the antenna is used to illuminate the object of interest, which, in turn, increases the SNR at the RX input. The RX employs an off-chip narrow-beam horn antenna manufactured by Quinstar Technology. The pyramidal standard gain horn antenna has an aperture size of 26.2×20.3 mm^2, a mid-band gain of 24 dB, and a beam width of 11°. The horn antenna is connected through a WR-10 waveguide to the wafer probe. A mechanical drawing of the imaging test setup is shown in Fig. 28. A simple MMW image of an envelope containing a coin (a US quarter) was created and demonstrated in Fig. 29. The image was generated one pixel at a time, by stepping the envelope position over a 60×40 mm^2 area in 5-mm increments. This coarse step was chosen due to the limited accuracy

TABLE I
SUMMARY OF RECEIVER PERFORMANCE

Pre-detection Gain	30 dB
3-dB Bandwidth	26 GHz
Minimum NEP	10 fW/Hz$^{1/2}$
Responsivity	20−43 MV/W
NETD	0.3/0.4 K (τ = 40/30 ms)
Supply Voltage	1.8 V
Power Dissipation	200 mW
Technology	0.18-µm SiGe BiCMOS (fT/fmax = 200 GHz) MAG = 3.9 dB, NFmin = 7.2 dB @ 90GHz
Die Area	5×2.5 mm^2

TABLE II
PERFORMANCE COMPARISON OF 94-GHZ IMAGERS

Ref.	Technology	Integration	NETD	Responsivity
[2]	InP HEMT	LNA+Detector chipset	0.45 K[1]	0.5 MV/W
[13]	GaAs HEMT	LNA + Detector + Dicke Switch	1.6 K[2]	-
[4]	0.13-µm SiGe	LNA+Detector	0.6-0.8 K[3]	4 MV/W
[5]	65nm CMOS	LNA + Detector + Dicke Switch	10 K[4]	0.09 MV/W
This work	**0.18-µm SiGe**	**LNA+Detector+Dicke Switch+Baseband**	**0.4 K**	**43 MV/W**

[1]τ = 3.125 ms. [2]τ = 10 ms. (τ = 30 ms for others)
[3]Accounting for external Dicke switching. [4]Calculated from data.

of manual movement of the envelope. The chip output voltage was read on an oscilloscope for each pixel.

Table I summarizes the RX performance, and Table II compares this work to other published imaging receivers. As indicated in Table II, the proposed imaging RX achieves the best NETD compared to any silicon-based radiometer to date.

IV. CONCLUSIONS

A highly integrated passive imaging RX was designed and fabricated in a silicon-germanium process. The RX utilizes high-speed HBTs, slow-wave CPW transmission lines, and a unique balanced LNA with an embedded Dicke switch in order to achieve 0.4 K NETD. Improvements in imaging performance, power dissipation, and chip area can be achieved by using more advanced silicon processes, such as 45 nm CMOS with f_T/f_{MAX} of 400 GHz. Such processes can also be used to design for other PMMW windows (140 GHz or 220 GHz). Future work could also include focal plane arrays (FPA), which integrate multiple imaging pixels into a single RX chip.

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