Ka-Band SiGe HBT Low Phase Imbalance Differential 3-Bit Variable Gain LNA

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***Abstract*—This letter presents the design and implementation of a differential Ka-band variable gain low noise amplifier (VG-LNA) with low insertion phase imbalance. The VG-LNA is based on a 0.12 μm SiGe heterojunction bipolar transistor process, and the gain variation is achieved using bias current steering. The measured VG–LNA gain at 32–34 GHz is 9–20 dB with eight different linear-in-magnitude gain states, and with a noise figure of 3.4–4.3 dB. The measured rms phase imbalance is $< 2.5^{\circ}$ at 26–40 GHz for all gain states and this is achieved using a novel compensating resistor in the bias network. The VG-LNA consumes 33 mW (13.5 mA, 2.5 V) and the input 1-dB gain compression point is −27 dBm. The chip size is 0.13 mm^2 without pads.**

***Index Terms*—Current steering, low noise amplifier (LNA), noise figure, phase imbalance, SiGe heterojunction bipolar transistor (HBT), variable gain amplifier (VGA).**

I. Introduction

RECENT development of SiGe BiCMOS technology allows system integration of a millimeter-wave phased array on a single chip. The phased array system requires amplitude and phase control of the incoming signal to achieve electronic beam control with low sidelobe levels [1]. A variable gain amplifier (VGA) is often used for the amplitude control and can be combined with a low noise amplifier (LNA) to reduce power consumption and chip size.

A phased array requires an amplitude control range of about 10 dB, and a linear-in-magnitude gain variation is desirable for amplitude weighting. A VGA with digital control is preferred over an analog design since it simplifies the interface with digital circuits and is less sensitive to noise in the control lines. The VGA must have a low insertion phase variation over the different gain states (phase imbalance) to avoid complex phase/amplitude calibration of the array [1].

In this letter, a SiGe HBT differential variable gain LNA (VG-LNA) is demonstrated at Ka-band frequencies. The LNA is designed for simultaneous input power and optimum noise matching [2], [3], and the VGA is based on a digital current steering technique to minimize the phase imbalance [4].

II. Digital Current Steering VGA

There are three basic VGA topologies which are not based on a variable attenuation stage (Fig. 1). A bias-controlled VGA, where the bias current or collector-emitter voltage are controlled

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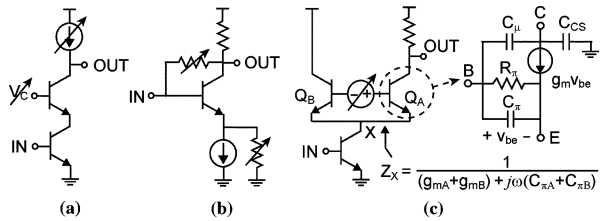


Fig. 1. Basic types of VGA: (a) bias control, (b) feedback control, and (c) current splitting.

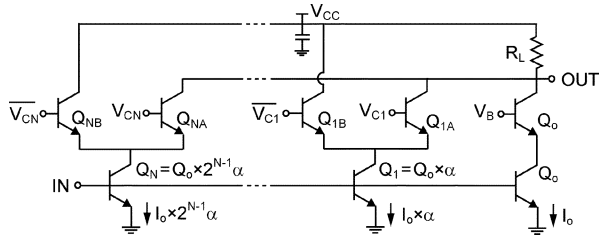
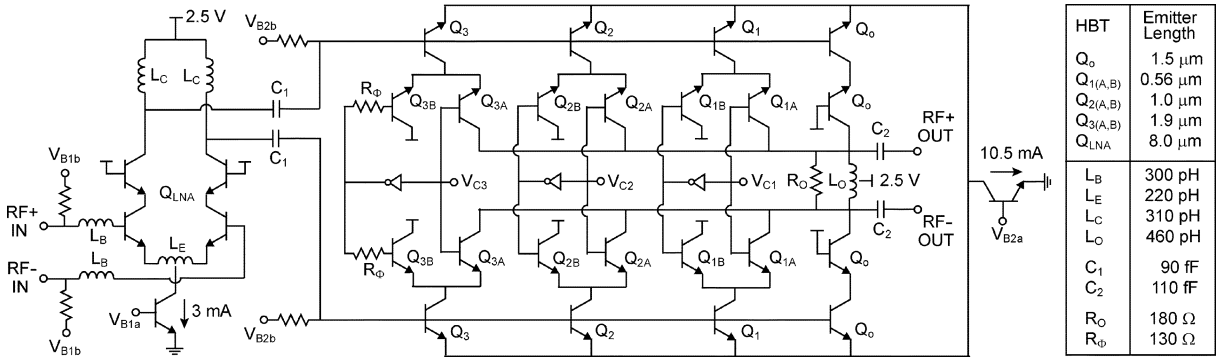


Fig. 2. Current steering linear-in-magnitude VGA with digital controls.

to change the transconductance (g_m), is quite common for RF applications [Fig. 1(a)] [5]. The feedback factor can also control the gain of a amplifier [Fig. 1(b)] [6]. The input impedance for these VGA topologies depends on the gain level, especially at Ka-band frequencies. Therefore, the insertion phase changes significantly depending on the VGA gain, and results in a high phase imbalance.

Fig. 1(c) shows a current splitting VGA topology [7], [8]. The bias current of the input transistor can be split into two transistors depending on the control voltage, and a variable gain can be achieved. This topology has a constant bias current for the input transistor, and results in a constant input impedance. The bias current variation for the current splitting stage changes the impedance looking into node X, $1/(g_m + j\omega C_\pi)$. However, this does not have much affect on the insertion phase since $g_m \gg j\omega C_\pi$. The output capacitance, $C_\mu + C_{CS}$ (C_{CS} = capacitance between collector and substrate), slightly varies due to the bias voltage variation at the base-collector junction. This effect can be compensated using a resistor as discussed in Section III.

Fig. 2 presents the digital version of the current splitting VGA. The gain variation is achieved by completely steering the bias current of the input transistor ($Q_n, n = 1 \cdots N$) to two transistors (Q_{nA} and Q_{nB}). When the control voltage V_{Cn} is high, the Q_n bias current is steered through Q_{nA} and the base signal of Q_n is amplified to the output. When V_{Cn} is low, the Q_n bias current is steered toward Q_{nB} without amplifying the signal. The transistor sizes of N current steering amplifiers are



HBT	Emitter Length
Q_o	1.5 μm
$Q_{1(A,B)}$	0.56 μm
$Q_{2(A,B)}$	1.0 μm
$Q_{3(A,B)}$	1.9 μm
Q_{LNA}	8.0 μm
L_B	300 pH
L_E	220 pH
L_C	310 pH
L_O	460 pH
C_1	90 fF
C_2	110 fF
R_O	180 Ω
R_Φ	130 Ω

Fig. 3. Schematic of the Ka-band differential VG-LNA.

binary scaled for N-bit operation, and therefore the bias current and g_m are also scaled in the same way. The minimum gain of the VGA is defined by the cascode transistor, Q_o, which is α times smaller than Q_1. The VGA voltage gain can be written as

$$A_v = -g_{mo}R_L(1+\alpha\cdot b_1+2\alpha\cdot b_2+\cdots+2^{N-1}\alpha\cdot b_N) \quad (1)$$

where g_{mo} is g_m of Q_o, and $\{b_1\, b_2 \cdots b_N\}$ is the binary word for the control voltage (V_{Cn}). Therefore, the maximum gain variation is $20\log\{1+\alpha(2^N-1)\}$ (dB).

III. Differential VG-LNA Design

A differential Ka-band 3-b VG-LNA is designed using the IBM 0.12 μm SiGe BiCMOS process with a peak f_T of 200 GHz (Fig. 3). A LNA stage precedes the VGA stage to achieve a low noise figure for all the gain states. The LNA is an inductively degenerated cascode amplifier, and its input impedance is matched with L_B and L_E for simultaneous input optimum noise and power matching [2]. The transistors have an emitter size of 0.12×8 μm^2 and are biased at 1.5 mA each, which is close to the optimal current density for the minimum noise figure.

The VGA stage is implemented to achieve a maximum gain variation of $\sim$11 dB, resulting in α =0.35. To minimize the current consumption, the smallest transistor Q_1 is selected first to have a small emitter length (ℓ_E) of 0.56 μm. The ℓ_E of Q_o, Q_2, and Q_3 are then scaled, while the emitter width (0.12 μm) is fixed. Since the g_m of the input transistor does not exactly scale with ℓ_E, the ℓ_E ratio between the transistors is slightly modified for accurate linear-in-magnitude gain control. The VGA is biased at a current density for maximum f_T, resulting in a total bias current of 10.5 mA.

The VGA phase imbalance is low by virtue of the constant bias current of the input transistor. However, the insertion phase still varies slightly for each bit since the output capacitance ($C_\mu + C_{CS}$) changes depending on the gain state. The capacitance change is more severe for the larger transistor (the higher order bit). When V_{C3} is switched to low, C_μ decreases due to the increased reverse-bias voltage of the base-collector junction and the VGA insertion phase increases. This phase imbalance can be compensated by using a resistor R_Φ (130 Ω) in the Q_{3B} control line. R_Φ increases the input impedance of Q_{3B} to $(j\omega C_{\pi B}R_\Phi+1)/(g_{mB}+j\omega C_{\pi B})$, and therefore the magnitude of the Q_3 voltage gain increases. This results in an increase of the Q_3 input capacitance due to the Miller effect, and a decrease in the VGA insertion phase. As a result, the decrease of C_μ at the output is compensated by increasing the effective input capacitance of Q_3.

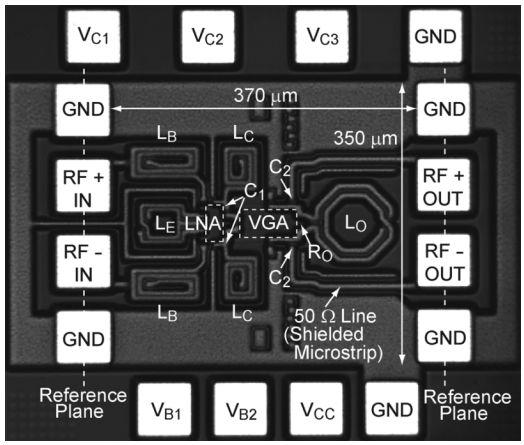


Fig. 4. Micro-photograph of the Ka-band differential VG-LNA.

Fig. 4 shows a photograph of the VG-LNA. The output of the VG-LNA is matched to a differential 100 Ω load using L_O and C_2. L_C and C_1 are used for interstage matching between the LNA and VGA stages. All passive components such as inductors, interconnects, and capacitors are simulated using a commercial electromagnetic software (Sonnet). The total VG-LNA chip area is 350×370 μm^2 (0.13 mm^2) without pads.

IV. Measured Results

The differential VG-LNA was measured on-chip using waveguide magic-T baluns for differential to single-ended conversion. The measurement system is calibrated using a differential calibration substrate (Cascade ISS126–109) and the measured results are referenced to the input and output G-S-S-G pads. The measured VG-LNA has a linear-in-magnitude gain control between 20 and 9 dB at 32–34 GHz (Fig. 5). At 33 GHz, the eight different gains are 9.9, 9.1, 7.9, 7.1, 5.9, 5.1, 3.8, and 3.0 in magnitude, resulting in a gain step of 1.0±0.2 and a slightly lower gain step for the least significant bit. the The measured center frequency shifted by 1–2 GHz compared to simulations due to un-accounted parasitic capacitances and transistor model/process variations. The measured S_{11} and S_{22} are less

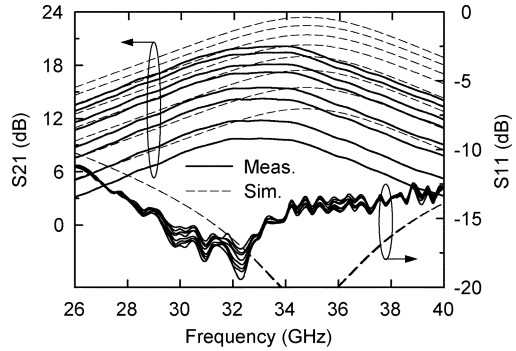


Fig. 5. Measured and simulated gain and input return loss of the eight different gain states.

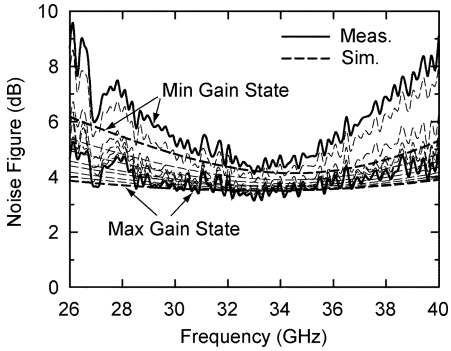


Fig. 6. Measured and simulated noise figures of the eight different gain states.

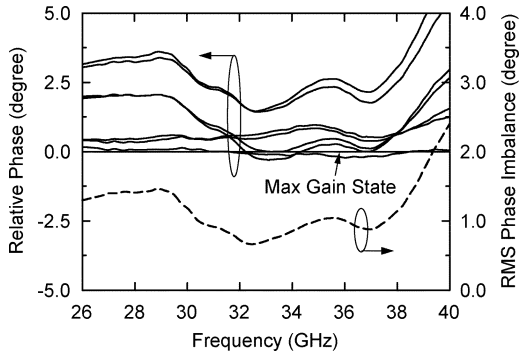


Fig. 7. Measured relative insertion phase and rms phase imbalance for all gain states.

than -11 dB and -15 dB for the eight different gain states, respectively. Even though the output capacitance $(C_\mu + C_{CS})$ depends on the gain states, the S_{22} is always well matched since $R_\circ$ dominates the output impedance.

The noise figure was measured using an Agilent 346CK01 noise source and an E4448A spectrum analyzer. The off-chip balun and G-S-S-G probe loss is subtracted from the measurement. The measured noise figure is 3.4–4.3 dB for the maximum–minimum gain state at 32–34 GHz (Fig. 6). The noise figure is slightly worse for the low gain state because the VG-LNA gain is low but the VGA noise current is constant. Fig. 7 shows the measured insertion phase of the VG-LNA relative to the maximum gain state, and the rms phase imbalance is $< 2.5^\circ$ at 26–40 GHz.

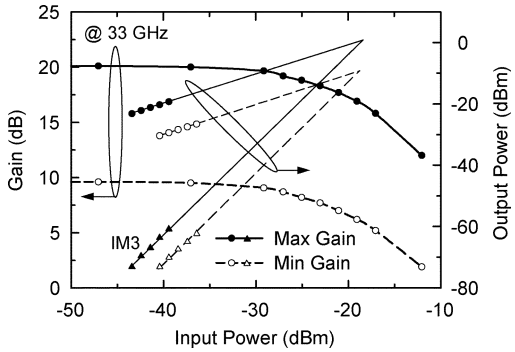


Fig. 8. Measured output power and gain versus the input power.

The input 1-dB gain compression point is measured at 33 GHz, resulting in -27 dBm for all the gain states (Fig. 8). The third-order intermodulation product with an offset frequency of 1 MHz results in an input intermodulation intercept point of -19 dBm. The input power handling capability of the VG-LNA does not depend on the gain state because the linearity of the VGA stage does not change due to the constant bias current.

V. Conclusion

A differential Ka-band VG-LNA (9–20 dB gain) is implemented using a 0.12 μm SiGe BiCMOS process for phased array systems. A rms phase imbalance of $< 2.5^\circ$ is achieved using a digital current steering technique and a compensation resistor. To our knowledge, this represents the first VG-LNA at Ka-band frequencies with excellent phase balance, and is suitable for Ka-band phased array applications.

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