A 1.9 GHz Low-Voltage Silicon Bipolar Receiver Front-End for Wireless Personal Communications Systems

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Abstract— **A 1.9 GHz wireless receiver front-end (low-noise preamplifier and mixer) is described that incorporates monolithic microstrip transformers for significant improvements in performance compared to silicon broadband designs. Reactive feedback and coupling elements are used in place of resistors to lower the front-end noise figure through the reduction of resistor thermal noise, and this also allows both circuits to operate at supply voltages below 2 V. These circuits have been fabricated in a production 0.8 μm BiCMOS process that has a peak npn transistor transit frequency (f_T) of 11 GHz. At a supply voltage of 1.9 V, the measured mixer input third-order intercept point is +2.3 dBm with a 10.9 dB single-sideband noise figure. Power dissipated by the mixer is less than 5 mW. The low-noise amplifier input intercept is −3 dBm with a 2.8 dB noise figure and 9.5 dB gain. Power dissipation of the preamplifier is less than 4 mW, again from a 1.9 V supply.**

I. Introduction

A 1.9 GHz low-noise preamplifier (LNA) and doubly-balanced mixer that have been fabricated in a mature silicon BiCMOS process are described in this paper. A production silicon technology offers the advantages of low fabrication cost as well as the potential for a high level of circuit integration. Monolithic transformers fabricated using coupled microstrip lines have been implemented to lower the operating voltage and the current consumed by both the receiver preamplifier and mixer. In addition to allowing a lower operating voltage, the transformer in the preamplifier is used as a low loss feedback element that has been exploited to achieve a low noise figure in the preamplifier, while maintaining the benefit of negative feedback to linearize the stage. Also, a monolithic transformer balun is used to efficiently couple the single-ended input signal from the LNA to a low power doubly-balanced mixer and thereby realize a low level of harmonic distortion and a good signal-to-noise ratio.

II. System Context

A block diagram of the first stage of a typical radio receiver is illustrated in Fig. 1. The front-end preamplifier and mixer are highlighted in this system level block diagram.

Manuscript received May 22, 1995; revised August 21, 1995. This work was supported by Micronet, the Natural Sciences and Engineering Research Council of Canada (NSERC), the Telecommunications Research Institute of Ontario (TRIO), and P. Schvan and R. Hadaway of Northern Telecom Ltd.

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IEEE Log Number 9415824.

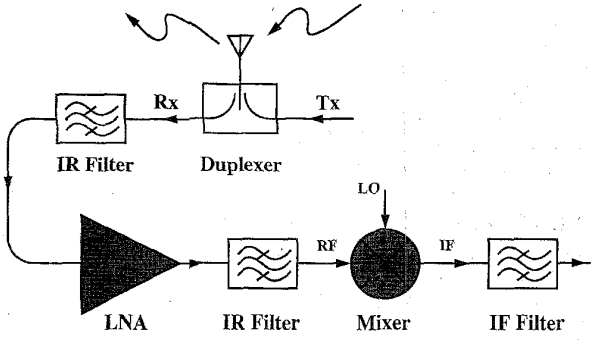


Fig. 1. Block diagram of a generic radio receiver.

The radio frequency signal received at the RF input to t mixer is modulated by the local oscillator (LO) signal and thereby translated to an intermediate frequency (IF) band. Tl facilitates signal processing at a lower frequency where high quality filters and amplifiers can be economically constructe

The spurious free dynamic range of the receiver is the sing most important performance specification for the receiv front-end. It is defined by the difference between the overlo point and the minimum discernible or acceptable signal level the RF input. The minimum signal level or receiver sensitivi is determined by the receiver noise figure (NF), which c be estimated from Friis' formula [1]. The upper limit the receiver dynamic range is usually determined by t mixer's distortion and gain compression characteristics, wh a preamplifier with sufficient gain to adequately suppress t mixer noise is used.

III. Fabrication Process

Northern Telecom's 0.8 μm BiCMOS process [2] was us to fabricate the preamplifier and mixer circuits. Bipolar devic were chosen for the front-end circuit implementation becau of their superior unity power gain frequency (f_{MAX}) wh compared to MOS devices fabricated in the same technolog A summary of the electrical parameters for a minimum si bipolar transistor is given in the right column of Table I. The npn bipolar devices are optimized for digital applications w a 5 V power supply, and a relatively high transistor tran frequency (f_T) is achieved through the use of a polysilic emitter contact. However, the area required to electrica contact the extrinsic base region results in large collector-ba

TABLE I
MICROSTRIP LINE AND BJT DEVICE PARAMETERS

Microstrip Line Parameter	Value	BJT Parameter ($A_E = 0.8X4.0\mu m^2$)	Value
Substrate resistivity	10 Ω-cm	Base-emitter capacitance, C_{JE0}	15 fF
Substrate (Si) thickness	380 μm	Base-collector capacitance, C_{JC0}	21 fF
Sub. dielectric constant	11.7	Collector-sub. capacitance, C_{JS0}	40 fF
Oxide (SiO_2) thickness	5 μm	Extrinsic base resistance, $r_{bb'}$	290 Ω
Oxide dielectric constant	3.9	Transit frequency, f_T	11 GHz
Top metal resistivity	0.03 Ω-μm	Max oscillation frequency, f_{MAX}	13 GHz

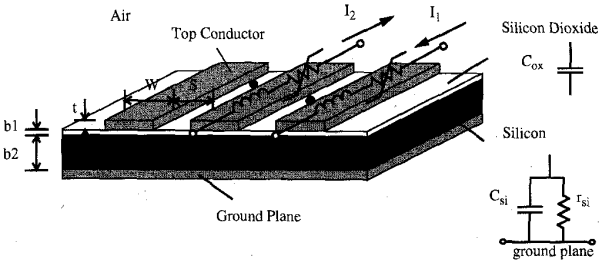


Fig. 2. Cutaway view of coupled microstrip lines on a silicon IC.

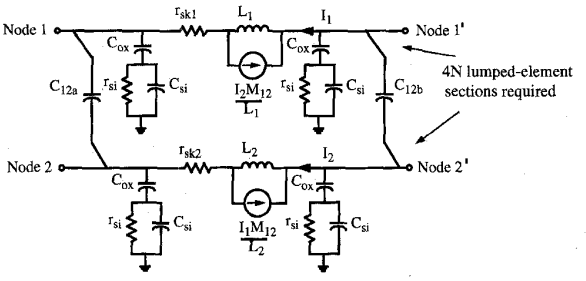


Fig. 3. Lumped element circuit model for coupled microstrip lines on silicon.

capacitance (C_{JC}) and a large extrinsic base resistance ($r_{bb'}$) when compared to bipolar IC processes that are optimized for RF performance. This limits the transistor f_{MAX} and the power gain that can be achieved by a preamplifier connected in the common emitter configuration, as well as limiting the minimum amplifier noise figure (NF_{min}). Resonant tuning using inductance can be used to reduce the effect of transistor parasitics on the circuit performance, but a transistor with a large emitter area is needed to minimize the noise introduced by the extrinsic base resistance.

Substrate and metallization properties, which define the properties of a microstrip line in the BiCMOS process, are shown in the left column of Table I. A cutaway view of two coupled microstrip transmission lines on silicon is also shown in Fig. 2 to illustrate some of the key parameters. The thin top metallization layer limits the quality factor of microstrip inductors or transformers fabricated using this process because energy is dissipated by the finite resistivity of the metallization as well as in the conductive substrate. However, the thick intermetal oxide dielectric reduces parasitic capacitance between the top level metal and the substrate, and this helps to improve the self-resonant frequency of these passive components. The quality of microstrip transmission lines fabricated on silicon substrates is degraded by dielectric losses in the conductive substrate as the signal frequency increases [3]. However, modern silicon VLSI technologies with multiple levels of metal used for circuit interconnections have a relatively low capacitance between the top layer of metal and the substrate. This development combined with a substrate resistivity on the order of between 1 and 100 Ω-cm can result in an acceptable level of dielectric loss in the 1–3 GHz frequency range. Recognition of this fact has revived interest in exploring the possibilities offered by the integration of microstrip elements on silicon for RFIC designs [4]–[6].

IV. MONOLITHIC MICROSTRIP TRANSFORMERS

Successful integration of high performance RF front-ends depends heavily upon the development of on-chip resonant circuits. Monolithic microstrip transformers integrated in Northern Telecom's BiCMOS VLSI technology are used in this paper to perform impedance matching, coupling, and phase-splitting functions in the RF front-end. Optimization and refinement of circuit designs incorporating on-chip inductors and transformers has been identified by others [7], [8] as lacking in the present state of the design art. A computationally efficient, scalable lumped-element model was therefore developed, which can be applied to any configuration of microstrip lines; not just spiral inductors or transformers. A physically-based, lumped-element model is extracted from the circuit layout and substrate parameters, which can then be used in either a time-domain (e.g., SPICE) or frequency domain (e.g., Touchstone) simulation. This approach to component modeling is more efficient than 3-D electromagnetic simulation techniques [9] and is shown in this paper to be sufficiently accurate for RF applications up to a few GHz.

As an example of this technique, a circuit model can be derived for the pair of coupled microstrip lines illustrated in Fig. 2. The physical length of a microstrip line on an RFIC is typically less than 1 μm, which is much less than the guided wavelength for applications below 3 GHz. A lumped-element π-equivalent circuit can therefore be used to accurately model each individual microstrip line. Two such π-equivalents are shown in Fig. 3, for two adjacent microstrip lines, as well as mutual capacitive coupling between the lines (represented by C_{12} in the figure). The parameters of the lumped-element model for each microstrip line are computed from the layout geometry and the substrate and metallization properties listed in Table I. The self and mutual inductances for all parallel line segments are calculated from closed-form expressions [10], where the nonzero metallization thickness is incorporated in the self and mutual inductance calculations using the geometric mean distance of the conductor cross-section [11]. The effect of the current induced in the ground plane is also accounted for [12], while current induced in the substrate can be neglected in the GHz frequency range because the substrate resistivity for the BiCMOS process is sufficiently large [13].

The self and mutual capacitances are computed using a two-dimensional numerical technique developed for coupled microstrip lines [14]. The shunt resistance of the semiconducting layer can then be estimated directly from the quasistatic

capacitance C_{Si} [15]. Dissipation of the mutual capacitances can be neglected when the microstrip lines are closely spaced. The frequency dependent resistance r_{sk} is determined from closed-form expressions [16] to complete the lumped-element equivalent circuit representation. This circuit model can be directly used in a time domain or frequency domain circuit simulation along with other active and passive RF elements. The complete model would normally be reduced to a compact model or S-parameter representation for faster optimization of a complex RF circuit.

This technique can be extended to more than two coupled lines and applied to the analysis of spiral microstrip components, such as an inductor or a transformer. The physical layout of a microstrip spiral is first partitioned into four groups of multiple coupled lines for analysis; one group per side of the rectangular layout. A lumped element π-section is again used to model each individual microstrip line within a group, where it should be noted that the assumption of "electrically short" transmission lines is normally satisfied, for the outside dimensions of the rectangular spiral are usually less than 1 mm. Assuming $N = 8$ microstrip lines per side, for example, there would be $4N$ or 32 lumped element sections, along with the additional interconnecting elements to model the mutual capacitance between strips as in Fig. 3.

For design optimization, a simplified version of this lumped element model (i.e., a compact model) is then developed by simplifying this lumped element model, as is valid within a more restricted range of frequencies. An example of such a compact model for a transformer of turns ratio $1 : n$ is shown in Fig. 4. A compact model for a transformer balun is similar to the model shown in this drawing but with two secondary output ports and a center-tapped secondary winding. A linear transformer with magnetizing inductance L_m forms the core of the model. Parasitic inductances L_p and L_s are placed in series with the primary and secondary windings of the linear transformer to account for nonideal coupling (leakage) between the windings. Lumped resistors r_p and r_s are placed in series with the leakage inductances to represent losses in the metallization, and lumped capacitors are used to represent electrostatic coupling between the windings, as well as from each winding to the underlying substrate. The low frequency parameters of the compact model are easily determined from the corresponding low frequency parameters of the complete lumped-element model described previously. An estimate of the parasitic capacitances can also be obtained from the complete model, but optimization is required to refine the capacitive parasitic values and minimize the error between the electrical characteristics of the compact and complete lumped-element models. It should be noted that in the process of optimizing the compact model parameter values, their physical significance is lost.

From the simplified transformer circuit model shown in Fig. 4, it can be easily seen that the transformer will show a bandpass-type frequency response between the primary and secondary terminals. At frequencies well below the passband, little of the signal that is applied to the primary terminals can be coupled to the secondary winding. Therefore, the magnetizing inductance must be made large enough that the passband will occur within the desired frequency range by proper selection of the transformer dimensions and the number of turns of metal. However, too large a structure introduces unwanted parasitic capacitances that will limit the upper bandwidth. It should be noted that the linear transformer (shown at the center of the diagram in Fig. 4) has a permeability equal to that of free space, which implies high linearity and low frequency dependent losses in the core material. However, low core permeability does not tightly confine the magnetic field, so there is a less than perfect coupling between the primary and secondary windings of a monolithic transformer. This results in significant leakage inductances (L_p and L_s in Fig. 4) that also place an upper limit on the bandwidth of the transformer.

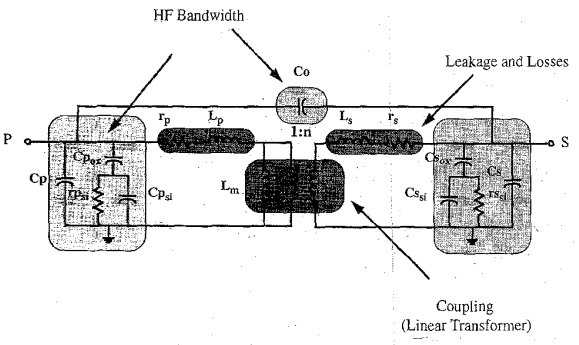


Fig. 4. Compact circuit model of a monolithic transformer.

If the feed-forward capacitance (C_o) is neglected, the parasitic elements at the input and output of the linear transformer in Fig. 4 can be combined with the source and load impedances into a single impedance, for example, Z_s at the source. The linear transformer has a reasonably high coefficient of coupling (k is between 0.7 and 0.8 for the monolithic transformers here) so it can be assumed that the leakage inductances are relatively small. The impedance seen at the secondary terminals for the combined source impedance Z_s (as defined) is then approximated by the following equation:

$$Z_{\text{reflected}} = n^2 \cdot [j\omega(L_m) \| Z_S]. \tag{1}$$

The impedance reflected from the primary to the secondary ($Z_{\text{reflected}}$ in (1)) is simply the parallel combination of the primary inductance and the combined source impedance multiplied by the square of the transformer turns ratio. Appropriate selection of the source reactance can then be used to modify the impedance reflected from the primary to the secondary. For example, a capacitance might be used to force a resonant condition between Z_s and L_m. A real impedance can then be reflected to the secondary. Similar arguments apply for impedances reflected from the secondary back to the primary. This example shows how tuning of the transformer primary and secondary circuits can be used to reduce the effects of the transformer inductances and thus idealize the transformer behavior for frequencies close to resonance. The transformer bandwidth when tuned is still on the order of a few hundred MHz, which is more than adequate for prospective wireless applications.

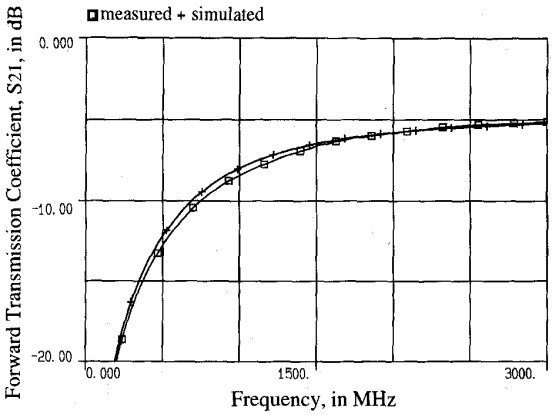


Fig. 5. Frequency response of the monolithic transformer balun (inverting output).

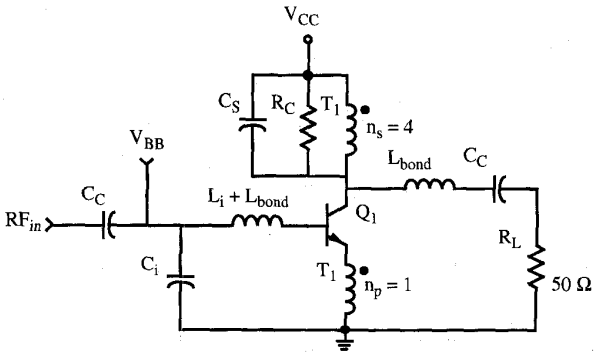


Fig. 6. Transformer-coupled low-noise amplifier schematic diagram.

The measured and simulated performance of the transformer balun designed for the doubly-balanced mixer is shown in Fig. 5. The measured transmission coefficient (S_{21}) from the primary input to the inverting secondary output is plotted for an on-wafer measurement using a separate test structure designed specifically for this purpose. The simulation result shown is for a complete lumped element model derived from the layout and substrate parameters as previously outlined. The performance predicted by the transformer model and the experimental measurements differ by less than 0.2 dB in the transformer passband. Excellent agreement has also been obtained for the primary to noninverting secondary output response of the balun.

The turns ratio of the monolithic transformer is set by the ratio of the secondary to the primary winding length and by the transformer linewidth and line spacing. The metal lines used in the transformer layout have dimensions on the order of microns, however, these dimensions are defined photolithographically to within one-tenth of a micron in a submicron IC process. Therefore, the coupling and the transformer turns ratio (i.e., self and mutual inductances) are insensitive to variations in the fabrication process. Simulations predict that the tolerance on the self and mutual inductances of the transformers designed in this paper will be less than 3% for a ± 0.2 μm change in the linewidth and linespacing. A larger and more subtle tolerance is introduced by variations in the intermetal dielectric oxide thickness and changes in substrate resistivity, both of which affect the parasitic capacitances of the transformer structure. However, simulations also predict that the variation in transformer bandwidth will be less than 5% for a ± 1 μm change in oxide thickness and a $\pm 50\%$ change in substrate resistivity from the nominal BiCMOS process parameters listed in Table I. These tolerances are far less than those encountered for other passive monolithic components, such as capacitors and resistors. A third source of variation is the temperature coefficient of resistance for the metallization used. Aluminum has a strong positive temperature coefficient of resistance (approximately 0.4% per degree Celsius) which can cause a large change in the metal losses with increasing temperature. For monolithic inductors, this is a severe problem because this shift in metal resistance will directly affect the component quality factor or Q. The effect on the performance of the transformer is not as severe, however, because the metal losses are in series with the terminal impedances present at the primary and secondary that are an order of magnitude larger.

V. Preamplifier (LNA) Design

High frequency amplifiers in a silicon integrated circuit technology have traditionally been designed as broadband circuits using resistors (R) and capacitors (C) as the sole passive circuit elements. However, a narrowband circuit topology that exploits the performance advantages offered by resonant tuning of inductive (L) and capacitive (C) elements has been chosen for this design. The schematic diagram of the low-noise RF preamplifier is shown in Fig. 6. Transformer T_1 is connected so that negative feedback is applied by mutual inductive coupling from the amplifier output at the collector of Q_1 back to the emitter to improve the linearity of the amplifier. Also, negative feedback will stabilize the amplifier gain as operating parameters such as temperature and supply voltage are varied. The common emitter connection has been chosen for Q_1 in order to maximize the gain and minimize the noise figure available from a single-stage amplifier [17]. For this paper, a preamplifier power gain of approximately 10 dB was chosen as a compromise between the overall receiver sensitivity and the input signal level that will overload the front-end circuitry.

The collector-emitter voltage across transistor Q_1 is almost equal to the full supply voltage V_{CC} because the resistive losses in the transformer primary and secondary windings are small. This allows the transistor to operate in the forward-active mode for supply voltages as low as 0.9 V. The transistor can also be operated at a low bias current, since the bandlimiting effects of the device parasitic capacitances at the collector can be minimized by tuning the collector load to the desired frequency of operation. Thus, low voltage as well as low power operation of the preamplifier can be realized. In addition, power consumed at the input by active feedback and terminal impedance modification schemes is eliminated by using the passive LC matching network formed by L_i and C_i, which can be implemented with high quality-factor off-chip components.

The relative contribution of the transistor noise sources to the overall signal-to-noise ratio depends upon the source impedance seen at the transistor input terminal, and there is an optimum source impedance that will result in the lowest noise figure. In general, this optimum noise match is not equal to the conjugate of the transistor input impedance that would be required for maximum power transfer. An inductor can be placed in series with the emitter lead of the BJT to modify the noise match [18], and under certain conditions, the minimum noise figure and the maximum power transfer at the input can be achieved simultaneously, making this approach very attractive. However, a large series inductor is required in practice, and therefore, two stages of amplification would be needed to achieve a gain of at least 10 dB. This increases the circuit complexity and the power consumption. A second alternative is to select the matching components at the amplifier input (L_i and C_i) to strike a compromise between the amplifier noise figure and the quality of the input impedance matching. However, without a good impedance match between the antenna and the LNA input, additional components would be required for antenna-amplifier isolation, which increases receiver cost, size, and weight. Therefore, a high quality impedance match is needed in order to transfer as much power from the antenna as possible without reflections. In this design, the LNA input is impedance matched to the source, and there is a slight increase in the noise figure as a result.

Dominant noise sources in this amplifier are thermally generated noise from the extrinsic base resistance of Q_1 and the shot noise generated by the flow of bias current in the collector. The collector load resistor R_C is used to match the impedance at the collector of Q_1 to the load. The resistor value needed to do this is relatively high, hence its thermal noise contribution is negligible because it appears at the amplifier output. Resonant tuning of the circuit adds some flexibility in the choice of the emitter area for Q_1 by resonating out stray capacitances, which is important when attempting to optimize the stage for the best possible noise figure.

The emitter area of the bipolar transistor for this LNA design was selected after evaluating both the gain and noise performance of the devices available in the BiCMOS technology. The maximum power gain that can be obtained from transistor Q_1 must be sufficient to meet the LNA gain specification at the desired operating frequency and bias point. The dominant term in the noise figure for a common emitter amplifier at high frequencies is [19]

$$\text{Noise Figure} \propto g_m \cdot r_{bb'} \left(\frac{f}{f_T}\right)^2. \tag{2}$$

This is consistent with the dominant noise sources being collector current shot noise (since collector current density determines f_T) and the thermal noise generated by $r_{bb'}$. At a given frequency, temperature, and bias current, only $r_{bb'}$ and f_T in (2) will vary with emitter area. Thus, the device emitter area can be increased in order to reduce $r_{bb'}$ until the collector current shot noise causes an unacceptable degradation of the noise figure because of a reduction in the transistor f_T.

The number of emitter stripes used in the device design was also investigated. The extrinsic base resistance for a given emitter area can be reduced by using a large number of transistors with short emitter stripes connected in parallel. This is commonly done in low frequency designs, where a much larger base area will be used in order to minimize $r_{bb'}$ at the expense of increased collector-base capacitance [20]. However, it was found in this case that multiples of the longest possible emitter stripe produced the best noise performance at a 2 mA bias current. This optimum is rather broad and is not critically dependent on the number of emitter stripes used or the total emitter area. The emitter area selected for Q_1 was $0.8 \times 120\ \mu\text{m}^2$.

Stability is an important issue in feedback amplifier design, especially at radio frequencies. The preamplifier must be stable for input and output terminations that are drastically different from the intended 50 Ω source and load impedances (such as an open circuit), and it must be stable in all frequency bands. The bipolar transistor is potentially unstable at low frequencies when the power gain is large, and hence, resistive damping is often added to the matching networks to dampen oscillations, even in single-stage amplifiers. This is undesirable because resistive losses increase the thermal noise level. The transformer feedback network used in this design bandlimits the low and high frequency ranges of the response, ensuring that the amplifier will be absolutely stable even when lossless matching networks are used. Computer simulations predict absolute stability for this design in all frequency bands (i.e., Rollett's stability factor > 1), and no oscillatory tendencies have been noted in practice.

The maximum power gain is realized when the LNA input and output are impedance matched to the source and load. The power gain of the low-noise amplifier (when properly matched) can be approximated by (3), shown at the bottom of this page, assuming the simplified BJT model of Fig. 7 and ideal voltage and current relationships for the transformer (i.e., perfect coupling) where

$$A_{\text{BJT}} = 1 + j\omega r_{bb'}(C_\pi + C_\mu) - \omega^2 L_{\text{in}}(C_\pi + C_\mu) \tag{4}$$

and L_{in} is the total inductance at the amplifier input (i.e., L_i in series with L_{bond} in Fig. 6).

At low frequencies, the effects of the transistor capacitances can be ignored, and (3) can be approximated by

$$|S_{21}|^2 \sim \left|\frac{-g_m Z_L}{1 + g_m Z_L\left(\frac{1}{n}\right)}\right|^2. \tag{5}$$

$$\text{Power Gain} = |S_{21}|^2 = \left|\frac{-g_m Z_L}{A_{\text{BJT}} + g_m Z_L\left[\frac{1}{n} + j\omega r_{bb'} C_\mu\left(\frac{1}{n} + 1\right) - \omega^2 L_{\text{in}} C_\mu\left(\frac{1}{n} + 1\right)\right]}\right|^2 \tag{3}$$

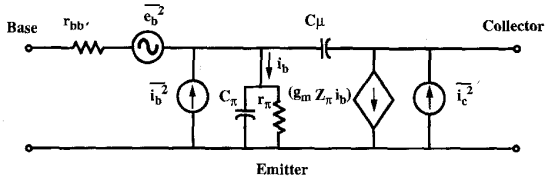


Fig. 7. Simplified small-signal model of the BJT at high frequency.

If the product of the transconductance and the load impedance $(g_m Z_L)$ is large, then (5) predicts that the low frequency power gain of the amplifier is equal to the square of the turns ratio (n). Tuning of the amplifier input can be used to achieve the same effect at RF because of two resonances present in (3). The first is the series resonance at the input, which is described by (4), and the second is the effect of the feedforward path due to the collector-base capacitance (C_μ) combined with the transformer feedback path. If the total inductance at the input (L_{in}) is resonated with capacitances C_π and C_μ, then the magnitude of A_{BJT} (as given by (4) becomes negligible compared to the other terms in the denominator of the power gain relationship. For small values of the base resistance and collector-base feedback capacitance, the C_μ dependent components in the second term in the denominator can be neglected, and the power gain of the LNA again reduces to the square of the transformer turns ratio. Thus, a transformer turns ratio of 4 should produce a power gain of 12 dB.

Under the previous assumptions, the 1:4 step-up transformer (T_1 in Fig. 6) will set the power gain of the amplifier if the transconductance and/or the load impedance are large. However, the BJT transconductance is small when the amplifier is operated at a low bias current, and the load impedance is also small (on the order of 50 Ω), hence the power gain of the LNA is not simply n^2. Nonidealities present in monolithic transformers, such as nonideal coupling between primary and secondary and feedforward parasitics (e.g., C_o in Fig. 4) will modify the power gain. In addition, the simplified high frequency equivalent circuit in Fig. 7 does not completely account for the BJT gain roll-off with frequency. Therefore, it is useful to compare the power gain of the BJT alone to the power gain that can be obtained from the complete LNA, in order to evaluate the true effect of the transformer feedback.

The frequency dependence of the maximum stable power gain for a BJT connected in common emitter configuration without transformer feedback is illustrated in Fig. 8. The BJT bias conditions used to derive these results are identical to those used for the LNA ($V_{\text{CE}} = 1.9$ V, $I_C = 2$ mA). Below 3 GHz, the BJT is potentially unstable, and so the highest power gain that can be achieved without an oscillation occurring is plotted in this frequency range. Above 3 GHz, the device is absolutely stable, and there is a discontinuity in the slope of the BJT gain curve at the transition point between the conditionally and unconditionally stable regions. The power gain of the LNA is also plotted in Fig. 8 for comparison, using an identical BJT biased under the same conditions, but connected to a 1:4 turns ratio transformer as in Fig. 6. The circuit is absolutely stable for all operating frequencies,

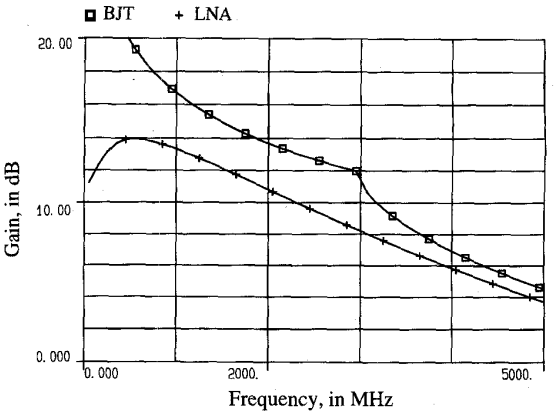


Fig. 8. Maximum available gain for the low-noise amplifier and the BJT.

consequently, the power gain curve shown for the LNA is the maximum gain available from the amplifier. As shown in the figure, transformer feedback achieves the desired effect; it stabilizes the amplifier and levels the power gain available from the BJT, at the expense of some gain reduction as would be expected with negative feedback.

Considering the input impedance of the amplifier, an analysis similar to (3) shows that the feedback from the output through the transformer has a relatively small effect. The output impedance is, however, strongly affected by the transformer feedback. The output impedance of a BJT without feedback has a large real component due to the small output conductance of the device. Application of negative feedback lowers the output impedance so that an additional matching network is not necessary at the output, which simplifies the overall LNA design.

The amplifier bias supply shown in Fig. 6 (V_{BB}) was not included on the prototype front-end testchip, and off-chip biasing was used. However, circuits that could be used to implement this bias source on-chip can be found in the existing literature [21], [22]. The collector current of the bipolar transistor must be controlled for variations in both the supply voltage and ambient temperature because many of the small-signal characteristics of the device are sensitive to changes in the collector bias current. One method of achieving this was presented by Heaney *et al.* in [23].

VI. Mixer Design

In general, optimum mixer performance can be expected from a balanced as opposed to a single-ended circuit topology [24]. The schematic diagram of the doubly-balanced mixer designed in this paper is shown in Fig. 9. The radio frequency (RF) input signal is split into in-phase and anti-phase components by balun T_1, which are then fed to the cross-coupled switching quad of transistors Q_1 to Q_4. Bias current is fed from current source Q_5 to the switching quad through the center-tap in the balun secondary. The signal current is chopped by the transistor quad at the LO rate in order to down-convert the input signal from RF to the desired IF. The down-converted RF input signal is buffered to a 50 Ω

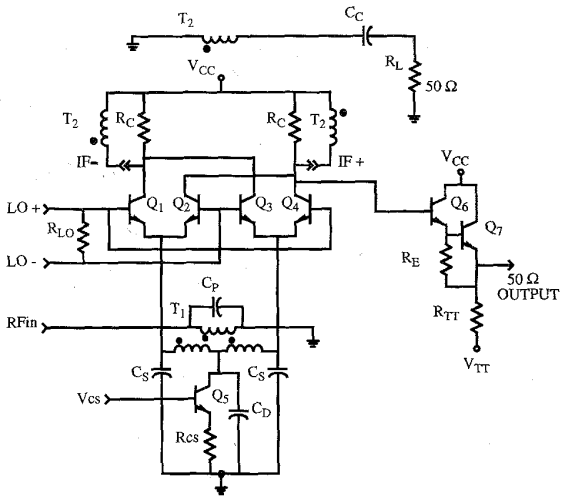


Fig. 9. Doubly-balanced mixer schematic diagram.

load using the on-chip Darlington buffer (Q_6 and Q_7), or alternately, the IF output can be impedance matched using an external matching network (e.g., balun T_2 shown in Fig. 9). The balun turns ratio for the external matching network is chosen to match the impedance at the collectors of the mixer switching quad and the load at the IF output. Package and bondwire parasitics have a relatively small influence on the IF port matching, and a good impedance match can be achieved through the proper selection of the turns ratio for T_2 and the collector load resistance R_C.

The input from the LO is terminated on-chip by resistor R_{LO}. Most external microwave sources are single-ended, and therefore, a single-ended to differential signal conversion would be required to couple the generator to the LO input. An external passive balun could be used or another on-chip balun could be designed for this purpose, however, this would require greater chip area. The eventual design goal for a PCS product application is an integrated RF front-end where the LO source (i.e., a voltage-controlled oscillator or VCO) would be integrated on-chip with the receiver front-end, and in that case, the differential signal could be derived directly on-chip from the oscillator output without adding another balun at the LO inputs.

The doubly-balanced connection of this mixer will cancel even-order spurious components at the IF output. This is important in a monolithic mixer implementation, where spurious signals can interfere with other circuits integrated on the same IC through parasitic coupling paths. The LO signal is normally much larger than either the RF or the IF signals, and thus high isolation is necessary between the LO inputs and the other ports to prevent the LO signal from leaking back to the antenna or overloading the IF circuitry. The LO and IF ports are isolated by the symmetric connection of transistors Q_1 to Q_4, and matching of these devices in a monolithic context allows a LO-IF isolation of greater than 40 dB to be achieved in practice. The LO and RF ports are isolated by the balun, and thus symmetry in the balun response between the inverting and non-inverting ports is necessary to achieve good LO-RF isolation.

The balun T_1 is tuned by capacitors placed in parallel with the primary and secondary terminals, as per (1). When properly tuned, the source at RF and its associated impedance will reflect as a resistor and a voltage source in series at the secondary terminals. The load impedances seen by the two sides of the transformer secondary are the emitters of the switching quad. They can be modeled as an inductor in series with a resistor. The inductive reactance can be absorbed into the tuning network at the balun secondary, and consequently, only the real portion of this impedance must be matched to the transformed signal source. When this is done, the large-signal emitter resistance defines the transformer load. The emitter resistance depends upon the bias current (via Q_5) and the signal amplitude at the LO input to the mixer.

At a bias current of 2.5 mA, the load at the balun secondary is almost 50 Ω (resistive) when the LO port of the mixer is driven by a large amplitude sinusoid (−3 dBm input power). This impedance cannot be matched with a 1:1 turns ratio balun because the resistive losses of the transformer windings must be added to the primary and secondary impedances. Modifying the transformer turns ratio to a 4:5 step-up achieved the desired match without altering the bias current.

The source impedance as seen by each pair of transistors in the switching quad r_{SRC} can be approximated by the following equation:

$$r_{\mathrm{SRC}} = \frac{n^2 \cdot 50 + r_{T1}}{2} \tag{6}$$

where $1 : n$ is the balun turns ratio, and r_{T1} represents the resistive losses of the transformer windings. Ideal behavior of the transformer can be assumed here because the balun primary and secondary are resonant tuned. The LO inputs of the switching quad are driven with a large amplitude signal, and therefore two of the transistors in the quad are biased in the active region, and the other transistors in the quad are cut off for a large portion of each cycle (e.g., Q_1 and Q_4 "on" and Q_2 and Q_3 are cut off as in Fig. 9, when LO+ is much larger than LO−). The transistors biased in the active mode operate in the common base configuration and amplify each phase of the received signal to the IF output. The transformed source resistance (r_{SRC}) degenerates the common base amplifier and extends its linear range of operation. The transformer has been used to advantage here to match the source impedance to the mixer and improve the mixer linearity without causing a significant increase in the overall noise figure. This is because no additional dissipation has been added to the circuit other than the losses in the transformer windings, which are relatively small. Linearization of conventional IC mixers, such as the Gilbert-type balanced demodulator, requires the addition of degeneration resistance, which causes a large degradation in the mixer noise figure when high linearity is desired.

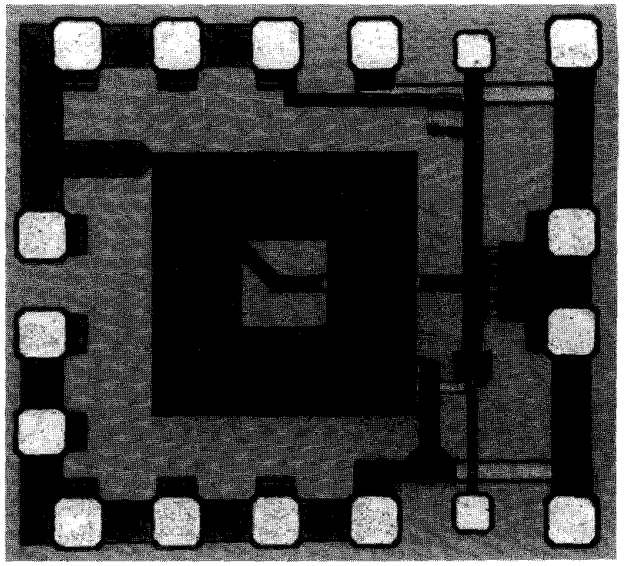
The noise introduced by the mixing process is difficult to determine analytically [25]. The balun introduces some loss at the mixer input because of dissipation in the windings, but this decrease in the signal-to-noise ratio can be easily computed from linear network theory. However, the nonlinearity caused by large-signal operation of the switching quad cannot be

treated in a simple way. When the quad is switched hard in either direction, only two of the transistors are active and the circuit is operating in a common base amplifier configuration. The RF signal coupled to the quad by the balun is amplified to the collector load at the IF outputs. There is some degradation caused by the dominant transistor noise sources of the common base amplifier, which are collector current shot noise and thermally generated noise from the extrinsic base resistance. Operating the mixer at a low bias current reduces the shot noise contributed by each active device, however, the switching speed of the transistors in the quad is also important to lowering the noise figure. When the LO inputs are close to the same potential, very little of the signal at the mixer RF input appears at the IF output because of the balanced circuit connection. All four transistors in the quad are forward biased in this condition and contribute noise to the IF output. Thus, the signal-to-noise ratio at the IF output is very low during the switching interval, and fast switching of the transistor quad is needed to reduce this portion of each LO cycle. Switching speed is not the only consideration because of the trade-off between emitter area and the extrinsic base resistance of the bipolar transistor. Careful selection of the emitter area for the transistors in the switching quad is therefore required in order to achieve a good mixer noise figure. A compromise is needed between a small transistor that can switch quickly between states and a larger transistor with less thermally generated noise from the transistor $r_{bb'}$.

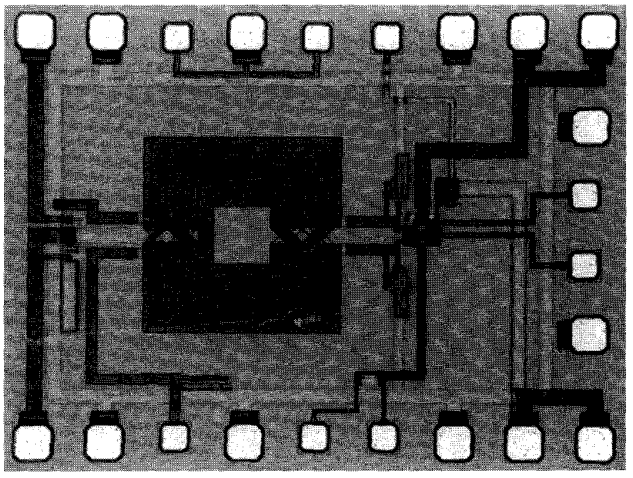
The nonlinear noise analysis capability of a harmonic balance simulator (Hewlett-Packard's MDS simulator) was used to compute the mixer noise figure. From these simulations, it was confirmed that collector current shot noise and thermally generated noise from the transistor extrinsic base resistance were the dominant sources of noise. The relationship between the local-oscillator input signal level and the noise figure was also investigated, and a transistor emitter area for transistors Q_1–Q_4 in Fig. 9 was selected that resulted in a simulated noise figure of 10.5 dB (single-sideband). Simulations also predict that the on-chip termination resistor R_{LO} increases the noise figure of the mixer by approximately 1 dB, and hence the noise figure could be improved by either integrating the LO source on the same chip as the mixer or by using a reactive matching network at the LO input.

VII. Circuit Layout Considerations

Photomicrographs of the low-noise preamplifier and doubly-balanced mixer test circuits are shown in Fig. 10(a) and (b), respectively. The transformers for both the mixer and the preamplifier are fabricated using aluminum metal 1 μm thick with a linewidth of 15 μm and a line-spacing of 1.8 μm. The inverting step-up transformer designed for the LNA consists of a total of eight turns and measures 400 μm on each side. The secondary winding is a continuous four turn spiral, and the primary winding consists of four single-turns connected in parallel, resulting in the desired 1:4 transformer turns ratio. The active area required by the amplifier is 0.65 $\times$ 0.55 mm^2.



(a)



(b)

Fig. 10. Front-end test chip photomicrographs. (a) Low-noise preamplifer. (b) Doubly-balanced mixer.

The design of the balun can be clearly seen in the photomicrograph of the complete mixer shown in Fig. 10(b). The balun consists of nine turns of top level metal and measures 425 μm on each side. The balun is symmetrically wound so that the center-tap can be precisely located and the losses in both halves of the secondary winding equalized. Primary and secondary microstrip lines are interleaved to maximize mutual coupling between the windings, and each half-turn is interconnected along the horizontal line of symmetry that runs across the center of the test chip. The mixer has an active area circuit area of 0.85 $\times$ 0.65 mm^2. The pad configuration used for both the LNA and mixer test chips was chosen to facilitate both on-wafer characterization using coaxial microwave probes and wirebonding of the IC's into a package [26].

TABLE II
LOW-NOISE PREAMPLIFIER PERFORMANCE SUMMARY

Low-Noise Amplifier	0.3μm GaAs E/D MESFET	0.5μm GaAs-JFET	Measured 0.8μm Si-Bipolar	Simulated 0.8μm Si-Bipolar
Supply Voltage	2.0 V	3.0 V	1.9 V	1.9 V
Supply Current	1.0 mA	4.0 mA	2.0 mA	2.0 mA
Frequency	1.9 GHz	1.9 GHz	1.9 GHz	1.9 GHz
Noise Fig. (50Ω)	-	2.8 dB	2.8 dB	2.9 dB
Min. Noise Figure	2.0 dB	-	2.1 dB	1.9 dB
Gain	12.2 dB	18.1 dB	9.5 dB	10.5 dB
IP3 (input)	-7.1 dBm	-11.1 dBm	-3 dBm	-3.5 dBm
Input VSWR	1.36	1.5	1.2	1.15
Output VSWR	1.77	3.1	1.4	1.03
Isolation	-	21 dB	21 dB	30 dB

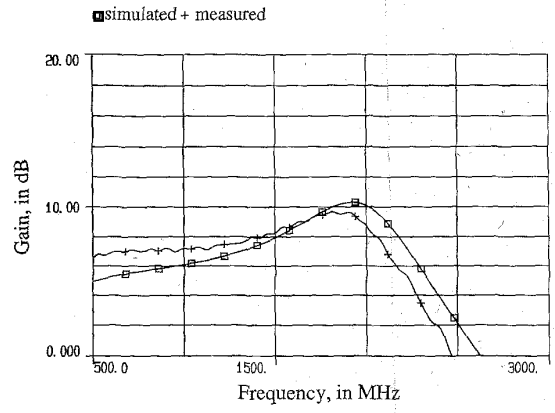


Fig. 11. Frequency response of the low-noise amplifier.

VIII. EXPERIMENTAL RESULTS

The measured and simulated performance of the low-noise amplifier is summarized in the column at the right side of Table II. These experimental measurements were obtained from a packaged device biased at a supply voltage of 1.9 V and a bias current of 2 mA. Both the LNA and mixer were packaged using a commercially available ceramic surface mount package for testing and characterization purposes. Ground path inductance of the preamplifier was minimized through the use of multiple wire bonds between the LNA common connection and the package ground. Simulations show that this emitter-to-ground inductance reduces the amplifier gain but does not affect its stability. Spurious oscillations or other unstable behavior were not observed during testing of the amplifier.

A noise figure of 2.8 dB was measured for the silicon LNA. A 3.5 nH series inductor (L_i) and a 2.5 pF shunt capacitor (C_i) were connected at the amplifier input as shown in Fig. 6 to achieve a good 50 Ω input match (VSWR of 1.2). The minimum noise figure of 2.1 dB was determined from on-wafer measurements of the amplifier using the ATN NP-5 noise measurement system. This data indicates that the noise figure of the amplifier could be further reduced at the expense of the quality of the input impedance match (i.e., higher VSWR) if desired. No attempt was made to impedance match the output of the LNA, however, an acceptable VSWR of 1.4 was achieved with the packaged device.

The third-order intercept point (IP3) characterizes the level of third harmonic distortion generated by the LNA. This transformer-coupled amplifier achieves a high input intercept for the chosen bias current. Harmonic distortion is generated by the nonlinear capacitances of the BJT and by the nonlinear (exponential) relationship between the collector current and the base-emitter voltage (i.e., the diode nonlinearity). Distortion produced by the diode nonlinearity will be higher here because a low dc collector current is used. In addition, the BJT when operated at a low bias current has large parasitic capacitances and can therefore generate significant amounts of harmonic distortion, even at low input power levels. A common-emitter amplifier with the same emitter area as that used in the LNA here and operated under identical bias conditions was found to have an input third-order-intercept point of −13 dBm. Thus, an 10 dB improvement in the input intercept point of the device is achieved through the use of transformer-coupled feedback in this amplifier configuration. A plot of the measured and simulated amplifier gain is shown in Fig. 11. The bandpass shape of the LNA frequency response is the result of resonant tuning the input matching network. The peak gain of 9.5 dB was obtained from the packaged device at a frequency of 1900 MHz. There are slight differences between the experimental measurement and the simulated curves, which can be attributed to modeling errors, tolerances in the input matching network components, and losses introduced by the package and test fixture. The power supply decoupling network causes the measured gain to increase at lower frequencies, where the quality of the ac ground at the transformer secondary is poor.

The amplifier isolation measured for the packaged device is 10 dB lower than predicted by the computer simulation, which was expected. This is because parasitic coupling within the package and the test fixture was not included, and there is a significant amount of mutual coupling (both capacitive and inductive) between package leads and bondwires. However, the measured isolation is adequate for wireless receiver applications.

The specifications for two recently reported 1.9 GHz GaAs LNA's are shown in the left column of Table II for comparison. The silicon bipolar LNA outperforms the 0.5 μm GaAs JFET preamplifier [26] in all reported specifications except power gain. The LNA fabricated in the fine-line E/D MESFET process demonstrated the best combined noise figure, gain, and power consumption specifications as of its publication date [27]. This GaAs IC has approximately 2.5 dB more gain at one-half the supply current of the silicon LNA developed in this paper. The GaAs amplifier input intercept point (IP3) is 4 dB lower than the silicon LNA, in part because a small bias current was chosen for the design. However, the quality of the input and output matching of the GaAs amplifier is poorer (i.e., a higher VSWR), and it should be noted that the process used to fabricate the E/D MESFET amplifier [28] is considerable more sophisticated and costly than a near-micron silicon BiCMOS technology.

The measured performance of the doubly-balanced mixer is summarized in Table III. The mixer was packaged and tested

TABLE III
DOUBLY-BALANCED MIXER PERFORMANCE SUMMARY

Mixer	0.5 μm GaAs-JFET	Measured 0.8μm Si-Bipolar	Simulated 0.8μm Si-Bipolar
Supply Voltage	3.0 V	1.9 V	1.9 V
Supply Current	4.0 mA	2.5 mA	2.5 mA
RF Frequency	1.9 GHz	1.9 GHz	1.9 GHz
LO Frequency	1.66 GHz	1.8 GHz	1.8 GHz
SSB NF (50Ω)	10.8 dB	10.9 dB	10.5 dB
Conversion Gain	5.7 dB	6.1 dB	6.3 dB
IP3 (input)	2.3 dBm	2.3 dBm	1.1 dBm
RF Port VSWR	1.2	1.17	1.15
LO-RF Isolation	13 dB	32 dB	80 dB
LO-IF Isolation	5 dB	47 dB	52 dB

at a supply voltage of 1.9 V and bias current of 2.5 mA. An input power of −5 dBm was used to drive the LO input, giving a single sideband noise figure of 10.9 dB in a 50 Ω system (i.e., with no additional noise matching network). The LO drive signal was coupled from the single-ended generator output to the differential inputs of the mixer using an external passive balun. A very low RF input VSWR of 1.17 was achieved without additional matching components. The on-chip Darlington buffer was used for initial testing of the mixer at wafer probe. This buffer circuit consumes additional power in order to interface the mixer IF output to a low impedance (50 Ω) environment, and therefore, it is more efficient to use a passive differential-to-single ended matching circuit at the IF port. Thus, an external transformer balun (transformer T_2 in Fig. 9) was used to match the mixer output to a 50 Ω load for testing and characterization of the packaged devices.

Recently reported results for a low-power 1.9 GHz monolithic mixer fabricated in a 0.5 μm GaAs technology are also listed in Table III for comparison [26]. A 3 V power supply is required by the cascoded transistors of the GaAs mixer, and hence that circuit dissipates more power. The noise figure and linearity of the silicon bipolar mixer (indicated by the high third-order intercept point, or IP3 at the input) are comparable to the results demonstrated for the GaAs design. The doubly-balanced configuration used for the silicon mixer, when compared to the singly-balanced GaAs design, resulted in a clearly superior LO-RF and LO-IF port isolation of 32 and 47 dB, respectively. High LO-IF isolation is desired in order to suppress spurious frequency components at the mixer IF output in a monolithic receiver implementation, and LO-RF isolation is necessary to prevent the LO signal from leaking back to the antenna. The LO-RF isolation of the silicon mixer, while more than adequate, is degraded by parasitic signal paths that exist on-chip, within the IC package, and on the test fixture. These signal paths were not accounted for in the simulation. Good agreement between measurement and simulation for all other specifications was obtained from both harmonic balance (Libra) and time-domain (SPICE) circuit simulators.

IX. CONCLUSION

Monolithic transformers fabricated using coupled microstrip lines have been used in this paper to further the design art of wireless receiver circuits in silicon IC technology. Performance specifications comparable to some recently reported results in GaAs technology were realized through the use of transformers implemented in a production BiCMOS process with standard process metallization. In addition to allowing an operating voltage below 2 V at 1.9 GHz, the monolithic transformer has been exploited as a low-loss feedback element to achieve a receiver preamplifier noise figure of 2.8 dB. The benefit of negative feedback was used to raise the amplifier input intercept to −3 dBm. A monolithic transformer balun has been used to efficiently couple the single-ended input signal from the preamplifier to a doubly-balanced mixer, thereby realizing a +3 dBm input intercept point and a 10.9 dB single-sideband noise figure at a low bias current. The power dissipation for the entire receiver front-end is less than 9 mW, which is a direct consequence of the efficiency offered by narrowband design methods.

ACKNOWLEDGMENT

Fabrication support and services were provided by the Telecom Microelectronics Center, Northern Telecom Ltd., Ottawa.

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