An Integrated 50-GHz SiGe Sub-Harmonic Mixer/Downconverter with a Quadrature Ring VCO

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***Abstract* — A 50 GHz sub-harmonic mixer based on multiple LO phases integrated with a 24 GHz quadrature ring VCO is fabricated in a 0.12µm SiGe BiCMOS process. The mixer core consumes 7 mA from a 3.3V supply. The mixer has a conversion gain of 9 dB and an SSB Noise Figure of 11.8 dB.**

***Index Terms* — Sub-harmonic mixer, quadrature ring oscillator, Millimeter wave integrated circuits, SiGe, Voltage Controlled Oscillator, Bipolar.**

I. Introduction

Wireless transmission at multiple gigabit-per-sec data rates is possible in high-frequency millimeterwave bands, and the use of silicon technology provides an opportunity for deployment of these systems at low cost [1,2]. Current silicon germanium and CMOS technologies offer high f_T and f_{MAX} and can be used for applications in the millimeterwave bands such as 24 GHz and 77 GHz automotive radars and 57- 64 GHz high data rate wireless communications. The goal of this research is to realize a high performance, low dc power, low area, millimeterwave receiver front-end for such applications in SiGe BiCMOS technology.

The design of high performance silicon-based oscillators at these millimeterwave frequencies is extremely challenging. One solution is to generate the local oscillator (LO) at a fraction of the RF frequency and then use a multiplier prior to frequency translation [1]. Another approach is to use a sub-harmonic mixer, which uses a sub-harmonic of the RF frequency as the LO [3]. This technique avoids a separate multiplier and associated circuitry, resulting in lower dc power consumption and active area. In direct-conversion applications, this approach reduces the DC offset issues due to LO-RF feedthrough. We present a double-balanced millimeterwave sub-harmonic mixer based on the frequency doubling obtained at the common emitter node of a differential pair [5]. This topology uses just two levels of transistors and hence operates at a low supply voltage and is completely double-balanced. To generate the required phases necessary for double-balanced operation, a two-stage differential ring oscillator is employed.

The integrated downconverter block diagram is shown in Fig 1. It includes a sub-harmonic mixer, a quadrature ring oscillator and associated LO and IF buffers.

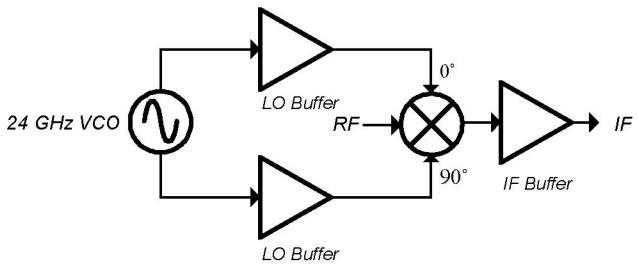

Fig.1. Architecture of down-converter with a sub-harmonic mixer.

II. Circuit Design

A. Sub-harmonic Mixer Design

One of the popular methods to obtain a sub-harmonic mixer is the use of anti-parallel diode pairs [4]. Unfortunately, this technique does not provide any conversion gain. At millimeterwave frequencies, high gain is difficult to obtain and hence a passive mixer can reduce the sensitivity of the receiver.

One technique to obtain sub-harmonic mixing with conversion gain is to multiply RF by quadrature LO signals at half the RF frequency [3]. However this topology needs three levels of transistors in its core and hence, is not suitable for low-voltage, low-power applications. Another technique involves using frequency doubling obtained at the common emitter node of a differential pair. This topology uses two transistor levels in its core and hence saves some head room. The schematic diagram of this mixer is shown in Fig 2.

This topology is a slightly modified version of the classic Gilbert Cell mixer. Each of the four LO switches are replaced by a pair of transistors, Q3-Q4, Q5-Q6, Q7-Q8 and Q9-Q10.

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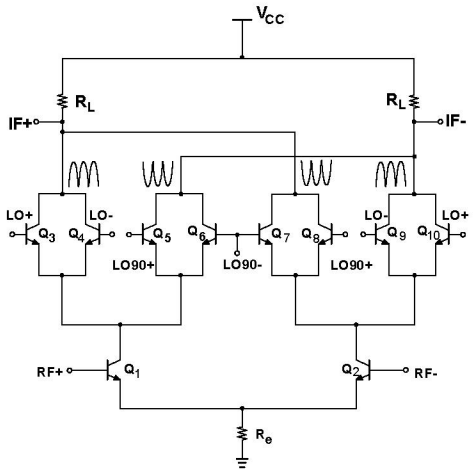

Fig. 2. Schematic of the sub-harmonic mixer.

Due to the inherent frequency doubling obtained at the common-emitter and collector nodes of these transistors, sub-harmonic mixing with one-half the frequency is obtained. Differential quadrature phases of the LO are needed to make the 2LO currents balanced. This topology is balanced for RF, LO, 2LO and IF making it a completely double-balanced mixer. This eases the grounding requirement, which is extremely beneficial at millimeterwave frequencies. The mixer tail current source is replaced by resistor R_e because of the difficulty in obtaining a high output impedance current source at high frequencies due to the parasitic capacitance at the collector of the current source transistor.

The sum of the collector currents of transistor pairs Q3-Q4, Q5-Q6 etc., have the form of a full-wave rectified sine wave, and they are composed of even harmonics only. This current has a $2w_{lo}$ term indicating frequency doubling. When the LO amplitude is high enough, the RF current can be thought of as being multiplied by +/- 1 at twice the LO frequency. So the ideal conversion gain, ignoring parasitic capacitances and assuming complete switching, is the same as that of a Gilbert cell mixer i.e.

$$G_c \approx \frac{2}{\pi} g_m R_L \qquad (1)$$

In comparison with the Gilbert Cell mixer, this topology shows a higher sensitivity to LO amplitude due to the extra capacitance that has to be charged and discharged due to the doubler pairs.

The transcondutor pair Q1-Q2 are sized 0.12 μm x 6 μm and biased at 3.5 mA current where collector and base shot noise contributions are equal for optimum noise performance [6]. An LO swing of 900 mV peak-to-peak was chosen for noise and gain considerations.

Input impedance matching is performed on-chip. The complex source impedance at the input of the mixer g_m transistors includes the 100 ohm differential source, bond pad capacitances of approximately 40 fF each and the metal lines. This is matched to the mixer core using 50 ohm microstrip shunt stubs and series transmission lines formed with top metal over bottom metal as shown in Fig. 3.

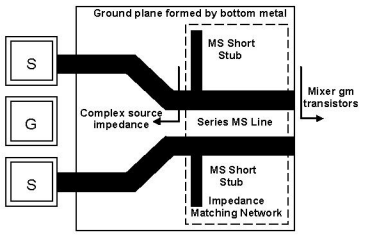

Fig. 3. Input impedance matching network.

B . Ring Oscillator

The differential quadrature phases needed for the sub-harmonic mixer are generated using a two stage differential ring-oscillator. This approach requires far lesser area than alternative techniques using quadrature hybrids [1].

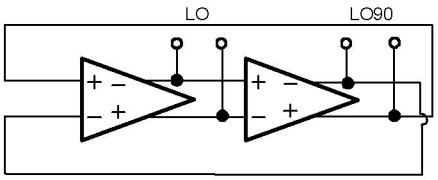

Fig. 4. Two-stage differential ring oscillator.

The block diagram of the 24 GHz quadrature ring oscillator is shown in Fig. 4. The delay cell constitutes an emitter-coupled differential pair followed by an emitter follower. The collector voltage was kept higher than BV_{CEO} but below BV_{CBO} , improving the phase noise due to the higher swing [7]. The measured VCO tuning rage was 18.5-25 GHz and had a phase noise of -85 dBC/Hz at 1 MHz offset. The detailed design and measurement results have been published in [7].

C. LO & IF Buffers

The LO buffers constitute a differential pair with resistor loads. To avoid LO pulling, they are driven by emitter followers as shown in Fig. 5. The mixer gain and Noise Figure depend on the degree of switching and hence on the LO swing. Provision for controlling the swing is provided through changing the tail current bias. IF emitter followers

with controllable bias current were used to allow impedance matching to the output load.

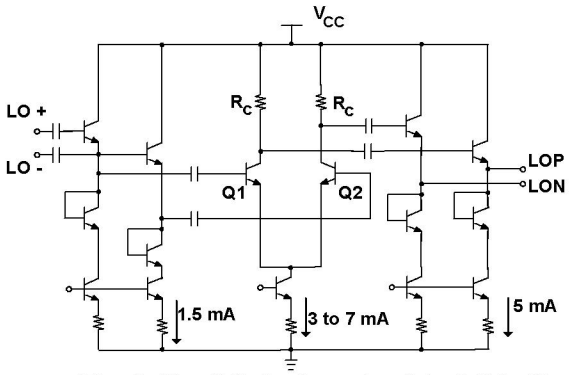

Fig. 5. Simplified schematic of the LO buffer.

II. Measurement Results

The circuit is fabricated in a seven metal layer IBM 8HP 0.12 μm SiGe BiCMOS process with an f_T of 200 GHz [1].

A. Measurement Setup

On-wafer probe testing was carried out using 125 um pitch dual probes in GSGSG configuration. Differential signals were generated using a WR-15 magic-T based on the scheme described in [8]. The measurement setup is shown in Fig. 6.

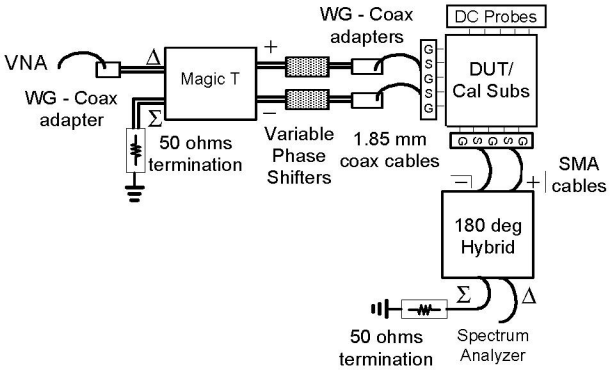

Fig. 6. Measurement setup.

A differential SOLT calibration substrate provided by the probe manufacturer is used to calibrate the RF port up to the probe tips. Waveguide phase shifters were used to correct any phase error due to the 1.85 mm coaxial cables between the waveguide to coaxial adapter and the probes.

B. Measurement Results

The peak measured conversion gain is 9 dB and the single sideband Noise Figure is 11.8 dB. The conversion gain and Noise Figure with varying RF frequency and a fixed LO frequency of 23 GHz is shown in Fig. 7 and Fig. 8 respectively.

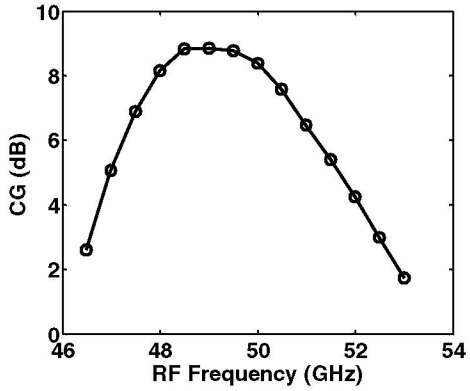

Fig. 7. Measured Conversion Gain vs. RF Frequency.

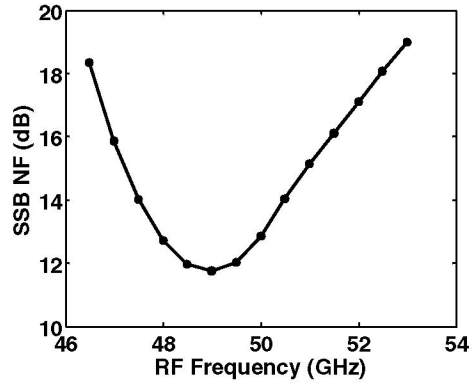

Fig. 8. Measured SSB Noise Figure vs. RF Frequency.

The measured input referred 1dB compression point was -16.5 dBm for an IF of 3 GHz. The measured input return loss was better than -7 dB from 50 – 55 GHz. The mixer core consumes 7mA from a 3.3V supply. Fig. 9 shows the chip microphotograph. The active die area is 880 μm x 360 μm.

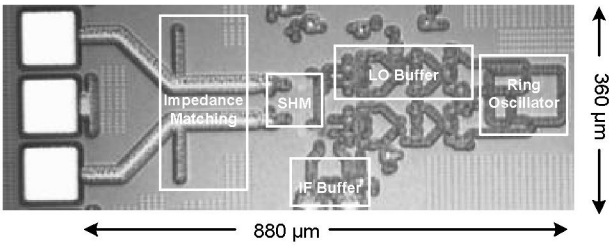

Fig. 9. Chip Microphotograph.

Reference	Frequency (GHz)	CG (dB)	SSB NF (dB)	IP_{1dB} (dBm)	SHM	Core Power (mW)	Technology
[1]	60	4	-	-	No	32.4 *(includes LO EF)*	0.12 µm SiGe HBT
[9]	60	7	13	-7	No	27 *(single balanced)*	0.12 µm SiGe HBT
[10]	60	9	21	-	No	1 *(single balanced)*	0.13 µm CMOS
[11]	77	-10.7	-	2.4	Yes	22	0.5 µm SiGe HBT
[12]	24	13	17.5	-	No	6 *(single balanced)*	0.18 µm CMOS
This Work	**50**	**9**	**11.8**	**-16.5**	**Yes**	**23**	**0.12 µm SiGe HBT**

Table I. Performance comparison with recent work.

A comparison with recent millimeterwave mixers in silicon is shown in Table I.

IV. Conclusioins

An integrated 50 GHz 0.12 µm SiGe sub-harmonic mixer and a 24 GHz ring VCO operating at 3.3V power supply is presented. The conversion gain of the mixer is 9 dB with a Noise Figure of 11.8 dB. These results demonstrate for the first time a completely double-balanced active sub-harmonic mixer integrated with a quadrature ring oscillator at these frequencies with excellent performance for millimeterwave wireless applications using SiGe technology.

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