A W-band CMOS Receiver Chipset for Millimeter-Wave Radiometer Systems

Lei Zhou, *Student Member, IEEE*, Chun-Cheng Wang, *Student Member, IEEE*, Zhiming Chen, *Student Member, IEEE*, and Payam Heydari, *Senior Member, IEEE*

***Abstract*—This paper presents a W-band receiver chipset for passive millimeter-wave imaging in a 65 nm standard CMOS technology. The system comprises a direct-conversion receiver front-end with injection-locked tripler and a companion analog back-end for Dicke radiometer. The receiver design addresses the high 1/f noise issue in the advanced CMOS technology. An LO generation scheme using a frequency tripler is proposed to lower the PLL frequency, making it suitable for use in multi-pixel systems. In addition, the noise performance of the receiver is further improved by optimum biasing of transistors of the detector in moderate inversion region to achieve the highest responsivity and lowest NEP. The front-end chipset exhibits a measured peak gain of 35 dB, −3 dB BW of 12 GHz, NF of 8.9 dB, while consuming 94 mW. The baseband chipset has a measured peak responsivity (R_v) of 6 KV/W and a noise equivalent power (NEP) of 8.54 $\mathrm{pW/Hz^{1/2}}$. The two chipsets integrated on-board achieve a total responsivity of 16 MV/W and a calculated Dicke NETD of 1K with a 30 ms integration time.**

***Index Terms*—CMOS, detector, frequency conversion, millimeter-wave, 94 GHz, passive imaging, radiometer.**

I. Introduction

MILLIMETER-WAVE (MMW) radiometers have been around since the 1960s. Nevertheless, only recently real-time MMW imaging techniques have become increasingly more attractive to the military and the public as a result of rapid progress in monolithic MMW integrated circuit technologies [1]. Applications of MMW imaging include remote sensing [2], security surveillance [3], and nondestructive inspection for medical and environment field [4], [5]. Passive MMW (PMMW) imaging is specifically attractive because its detection of emitted thermal radiation from a scene reduces public health concerns for medical applications and security concerns for military applications [6]. Current imaging systems using mechanical scanning employ high-performance low-noise receivers (RXs) implemented in III-V compound semiconductor technologies with low-level of integration. Benefiting from silicon technology scaling, the continuing increase in f_t enables the integration of highly complex MMW systems, such as 60 GHz high data rate wireless communication [7], [8] and 77 GHz automotive radar system [9]–[11], in a single die. Moreover, high packing density of silicon (and in particular, CMOS) technologies enables the possibility of building low-cost multi-pixel focal plane array (FPA) for PMMW imaging at W- and D-band frequencies. Several MMW front-ends have been developed for imaging systems [12]–[16], while a 94 GHz SiGe PMMW imaging IC with integrated detector is reported in [17].

CMOS, with its superior integration capability and lower cost in high volumes, is poised to be the ultimate solution for a fully integrated PMMW imaging system. Nevertheless, high 1/f noise of MOS power detectors (used in an all CMOS implementation) necessitates the use of a switched-based Dicke system. In [18], a 94 GHz CMOS PMMW imaging is demonstrated. However, due to the inherent lower available gain and higher 1/f noise, the circuit performance in [18] may not meet a practical PMMW imaging's sensitivity requirement. To address these challenges, a high-gain, low-power W-band direct-conversion front-end RX is presented. The proposed chipset incorporates an injection-locked tripler for LO generation and an analog back-end detector realizing a Dicke radiometer in a 65 nm standard CMOS process. This prototype mitigates the aforementioned issues at both architecture- and circuit-level design, demonstrating the feasibility of using CMOS for future generations of low-cost multi-pixel portable passive imaging cameras.

The remainder of this paper is organized as follows. Section II discusses the background and design requirement for PMMW imaging system. In Section III, we describe the RX architecture and system-level considerations for CMOS implementation. The design and analysis of the RX front-end and detector baseband chipsets are described in Sections IV and V, respectively. Measurement results of the RX are presented in Section VI. Finally, Section VII provides concluding remarks.

II. System Consideration

A. Radiometer Background

The radiometer employs a very sensitive RX to detect the power (P_E) emitted from the radiating object which can be expressed as $P_E = kT_EB$, where P_E is the noise-like input signal (called *signal-noise* throughout the paper) power the RX collects, B is the bandwidth of the front-end RX and T_E is the effective radiometric temperature [6]. For imaging application, the input temperature range of the radiometer is 0–313K [19]. The main parameter in the radiometer design is the sensitivity of the constituent RX. Noise equivalent temperature difference (NETD), which is a measure of the sensitivity, is defined as the

Manuscript received March 05, 2010; revised November 06, 2010; accepted November 06, 2010. Date of publication January 06, 2011; date of current version January 28, 2011. This paper was approved by Associate Editor Jacques Christophe Rudell. This work was supported in part by an SRC contract 2009-VJ-1962 and by an NSF grant ECCS 1002294.

The authors are with the University of California at Irvine, Irvine, CA 92697-2625 USA (e-mail: leiz@uci.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2010.2092995

effective radiometric temperature difference ΔT_E, producing a DC voltage at the RX's output, which is equal to the rms value of the output fluctuations due to the RX noise [20]. Given the RX's noise temperature T_N, the relationship between NETD and T_N is expressed as [20]

$$\text{NETD} = \frac{T_N}{\sqrt{B_{HF}\tau_{BB}}} \tag{1}$$

where B_{HF} is the bandwidth of the RX front-end and τ_{BB} is the integration time at the baseband. In order to generate real-time images, the integration time of the imager should not be greater than about 10–25 ms [21]. For instance, if $B_{HF} = 10$ GHz and $\tau_{BB} = 20$ ms, the RX with a T_N of 3000K will have an NETD of 0.21K. For a radiometer used in imaging application, the NETD must be less than 1K for acceptable image quality [22].

B. Dicke Radiometer

The RX's NETD is lowered by increasing either B_{HF} or τ_{BB}. Ideally, the output fluctuation can be reduced by increasing the integration time. However, when integration time reaches milliseconds to seconds range, gain variation in the high-gain amplifier can no longer be neglected. This is because the RX cannot differentiate the output voltage change caused by gain variation from the change in the input signal-noise power. Therefore, the NETD of the RX is expressed as [20]

$$\text{NETD} = T_N\sqrt{\left(\frac{1}{B_{HF}\tau_{BB}}\right)^2 + \left(\frac{\Delta G}{G_0}\right)^2} \tag{2}$$

where ΔG is the effective gain variation and G_0 is the average power gain. For example, the RX with a 3000K system noise temperature T_N indicates an NETD of 3K if the average 30 dB (G_0) front-end gain increases by 0.004 dB. To improve accuracy of the radiometer, the Dicke RX is chosen to solve the gain fluctuation [23]. A Dicke switch is inserted at the front-end input right after the antenna to switch between the input antenna and a reference load. As the modulation frequency is higher than the gain fluctuation frequency, it is possible to detect the signal-noise in the presence of gain variation. Since the RX only receives the input signal-noise one half of the time, the RX sensitivity is degraded as a trade-off of using Dicke RX architecture, i.e., $\text{NETD} = 2T_N/\sqrt{B_{HF}\tau_{BB}}$. Although the Dicke RX's NETD is twice that of an ideal radiometer (obtained above to be 0.21K), the 0.42K Dicke NETD is still much lower than the 3K NETD caused by the 0.004 dB gain variation. Note that, in an imaging system, the noise temperature from thermal background, antenna loss, SPDT Dicke switch loss, and interconnect loss should also be accounted for in the NETD budget. Since the significance of some of these sources of loss depends on the implementation and T_N is usually the main contributor to the total noise temperature of the system, only T_N is used in NETD calculation. The Dicke switch loss also degrades the system NETD and its effect will be explained in more detail in Section III-D.

III. PMMW Imaging Receiver Architecture

A. Direct-Conversion Receiver

Traditionally, PMMW imaging RX employs two types of architectures: direct detection [17], [24] and frequency conversion (e.g., direct conversion, heterodyne, and etc) [25]. The SiGe BiCMOS technology is the best platform to implement a practical PMMW system using direct-detection structure, as shown by a number of recently published works (including a paper recently presented in [26]). However, in the current 65 nm CMOS process, the insufficient front-end gain, poor isolation, and poor detector noise performance at 94 GHz prevent the use of direct-conversion architecture to design a practically viable PMMW system. Instead, a direct-conversion architecture meets the stringent noise and gain requirements of a PMMW system. Although SiGe BiCMOS provides better performance, the CMOS MMW front-end can be seamlessly integrated alongside digital baseband circuit, thereby leading to a low-power and high performance system.

Since there is no phase information in the received signal-noise, the direct conversion (with an LO frequency exactly in the middle of the wide RF band) does not necessarily need I/Q path. Moreover, the baseband bandwidth is reduced to one half of the RF bandwidth because of the frequency folding. Therefore, the proposed RF front-end chipset uses direct-conversion architecture to reduce chip area, as the wide bandwidth (e.g., 10 GHz) and high gain (e.g., 20 dB) requirements for an IF amplifier in a heterodyne architecture require maximizing the gain-bandwidth products, thereby mandating the use of bulky inductors (as part of series and/or shunt peaking passive networks) for bandwidth enhancement. Phase-locked loop (PLL)-based frequency synthesizers are commonly used [27] to generate the LO signal in a frequency conversion RX for wireless communication applications. An injection-locked frequency tripler has been chosen to generate the LO signal from the low frequency external source. The proposed LO generation scheme reduces the LO frequency to 30 GHz, making it markedly easier for routing/distribution and enabling LO sharing in a multi-pixel imager.

The high gain requirement in the PMMW RX is due, in part, to a large noise floor of the detector. It is, therefore, necessary to minimize the detector's noise equivalent power (NEP) (which is a measure of the detector's sensitivity) so as to reduce the required pre-detector's amplifier gain. Responsivity measures the detector's gain, defined as the output DC voltage divided by the incident power to the detector, while the NEP is calculated as the RMS output noise voltage divided by the detector's responsivity (see Sections V-A and V-B). In this design, a baseband detector, comprised of transistors biased in moderate inversion, is proposed to achieve better responsivity and lower NEP. In addition, a baseband detector achieves lower NEP compared to an RF detector, which is another reason why direct-conversion architecture is chosen.

Fig. 1(a) shows the block diagram of the direct conversion PMMW imaging RX. A two-chip solution is chosen to ensure testability at both system- and circuit-level. The chopped input signal with frequency band from 80 to 92 GHz is amplified by a five-stage common-source (CS) LNA. The amplified signal is mixed down to 0.1–6 GHz frequency band by an 86 GHz LO

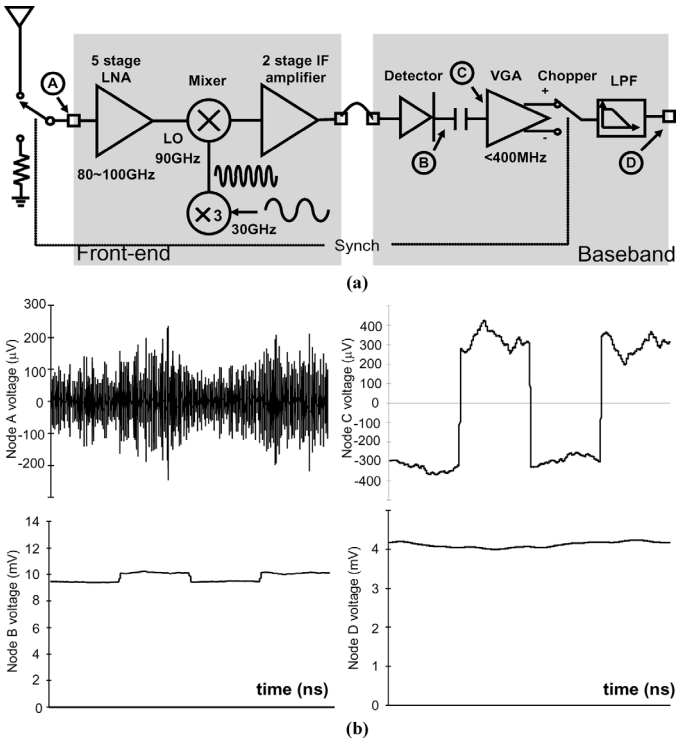


Fig. 1. PMMW imaging chipset. (a) Block diagram. (b) Waveforms at different nodes.

signal provided by the frequency tripler. After frequency conversion, the chopped signal is amplified by a two-stage wideband amplifier. The signal is then fed to the baseband chip, which performs energy detection, synchronization and integration to generate the output voltage proportional to the scene temperature. The wideband detector converts the chopped and amplified signal from the front-end chip into a 100 MHz modulated baseband signal, which is then amplified by a variable-gain amplifier (VGA). A baseband chopper, which is synchronized to the front-end chopper, converts the modulated signal into a constant DC level using a 500 kHz low-pass filter.

B. 1/f Noise

One important issue regarding advanced CMOS process is the higher 1/f noise corner frequency compared to III-V and SiGe compound semiconductor technology. 1/f noise causes DC drift at the RX's output, which affects the RX's NETD in a similar way as the RX's gain fluctuation, and thus will be alleviated using Dicke architecture. By increasing the switching frequency higher than the 1/f noise corner frequency, the 1/f noise contribution on the RX's NETD will become negligible. The 1/f noise corner in a 65 nm CMOS process is between 100 MHz and 1 GHz. Conventional mechanical chopper with electronic-wave absorber has a maximum speed limit of around 200 Hz [28]. Because of its faster switching speed, an electronic switch is thus preferred to reduce the RX's NETD. Fig. 2 shows measured output noise spectrum of the detector along with 1/f noise fitting line. The detector noise floor, measured using the spectrum analyzer, is captured from 100 kHz to 100 MHz with resolution bandwidth (RBW) of 1 Hz. As shown in this figure, at 30 MHz, the noise PSD is approximately 5 dB higher than

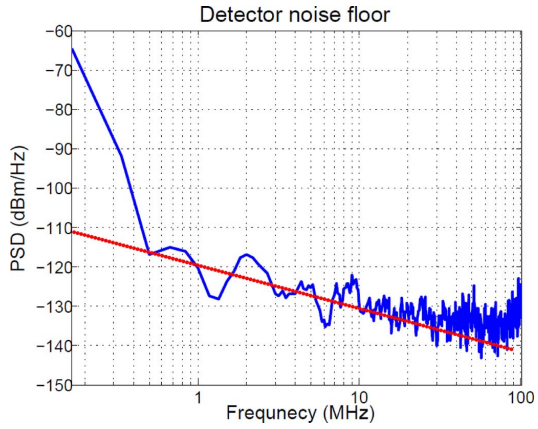


Fig. 2. Measured output noise of the detector with curve fitting.

that at 100 MHz corner frequency. This means that switching at 30 MHz still greatly reduces the 1/f noise.

C. Phase Noise

Since the received signal is downconverted to a zero-IF frequency by an LO signal, inevitably the oscillator noise is also downconverted, which affects the noise floor of downconverted signal, and thus, the RX's noise figure (NF). In contrast to conventional wireless communication systems, there is no specific high power RF interference in the RX band of 80–92 GHz. Assuming the highest neighboring blocking signal is no larger than the expected received RF signal of $kTB = -62.5$ dBm (where $B = 10$ GHz), the noise power P_n at an offset frequency of 100 MHz introduced by the LO phase noise is calculated as $P_n = P_{bl} + L\{\Delta f = 100\ \text{MHz}\}$. In order to ensure that the LO phase noise contributes negligible noise to the RX at the frequency offset of 100 MHz, based on assumed blocking signal level of -62.5 dBm, the LO phase noise needs to be $-174 - (-62.5) = -111.5$ dBc/Hz.

D. Dicke Switch Insertion Loss

The insertion loss of the Dicke switch at the RX's input directly degrades the RX responsivity and NEP. In order to meet the 1K NETD requirement, the insertion loss should be kept lower than 3 dB for our designed RX. However, on-chip SPDT switch in 65 nm CMOS exhibits an insertion loss of 4–5 dB [18]. Therefore, in this prototype, to maximize the power detection performance of the RX in 65 nm CMOS, Dicke switch modulation is emulated off-chip to compensate for the gain variation and improve the RX sensitivity.

IV. PMMW Imaging Receiver Front-End

A. Passive Components

Passives are considered to be the key components in the MMW IC design. Transmission lines (T-lines) provide better model accuracy than inductors due to the well-defined ground planes. However, the use of T-lines results in a noticeable increase in chip area. Slow-wave coplanar waveguides (SW-CPWs) are thus used as part of the on-chip matching

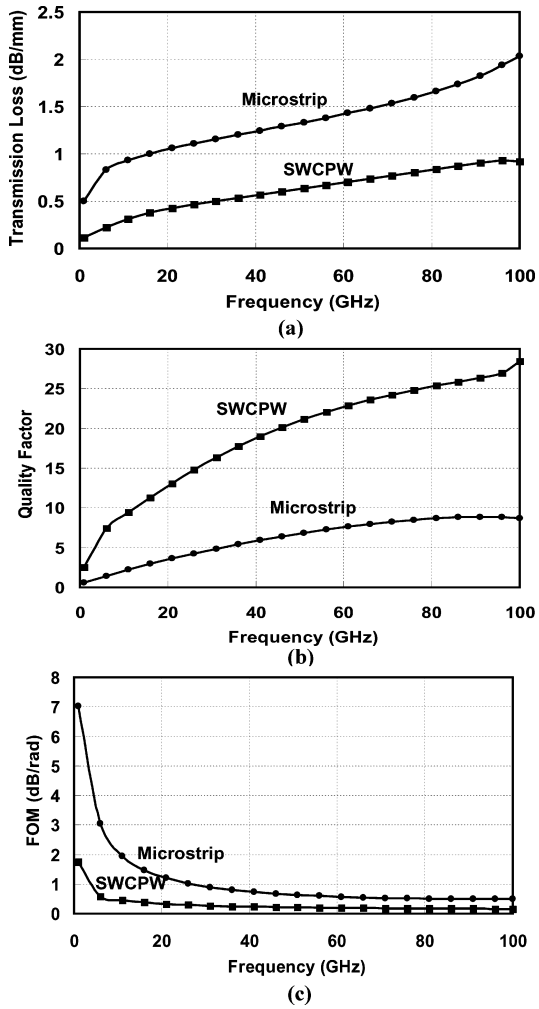


Fig. 3. SW-CPW and microstrip comparison. (a) Transmission loss. (b) Q factor. (c) FOM.

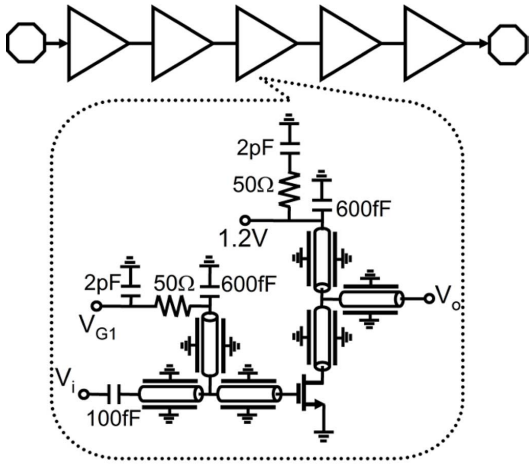
networks in our design [29], [30]. The top two metals are shunted together and used for the signal line. The coplanar grounds are shunted with all metal layers M3–M7, since the lowest two are used for floating shield. To ensure that the two coplanar ground planes are at the same potential, underpasses using metal layers M3–M5 are used. These underpasses use minimum width allowed by the technology in order to suppress the induced current flow in the direction of signal propagation. Metal density requirement is met by efficient use of all metal layers in the ground plane, as for middle conductor, the requirement is met by the periodic underpasses.

Since the characteristic impedance is close to 50Ω, in order for a grounded CPW to achieve such high characteristic impedance, the ratio $\mathrm{W}/(\mathrm{W}+2\mathrm{S})$ must decrease (W: width, S: spacing). A grounded CPW (GCPW) with $\mathrm{W}=3\ \mu$m and $\mathrm{S}=20\ \mu$m can achieve this characteristic impedance. A GCPW with such a wide spacing is roughly equivalent to a microstrip with M1 ground shield. The width and spacing of SW-CPW are 10 μm and 20 μm, respectively. A microstrip with $\mathrm{W}=3\ \mu$m with M1 ground shield is used for comparison. The EM simulated result includes skin effect as well as substrate loss. In the EM simulation environment, substrate loss is set to $10\ \Omega\cdot$ cm. In addition, the SiO_2 dielectric loss is also taken into account in the EM simulation with loss tangent of 0.01. Microstrip lines achieve losses of 1.2 dB/mm at 30 GHz and around 1.8 dB/mm at 90 GHz, as shown in Fig. 3(a), which is mainly attributed to the shorter line width. The SW-CPW achieves 0.9 dB/mm attenuation at 90 GHz. Moreover, the high relative dielectric permittivity of 10 achieved by the SW-CPW compared to just 4.5 for the microstrip line means that an effectively long electrical length can be realized using a shorter physical length. Fig. 3(b) also compares the quality factors (Q), as defined in [31], of the microstrip line and the SW-CPW. At 90 GHz, an SW-CPW achieves a Q of 26.3 compared to only 8.9 achieved by a microstrip line. Note that the improvement in overall Q of the SW-CPW compared to a microstrip line is a result of a given line-to-ground distance and shorter line width. Finally, an appropriate figure-of-merit (FOM) for the T-line's loss is (α/β) or (dB/rad), which takes into account the wavelength due to increased permittivity. The major benefit of slow-wave structure is evidenced in Fig. 3(c). It shows that for the same phase delay, the SW-CPW has lower loss than a microstrip line.

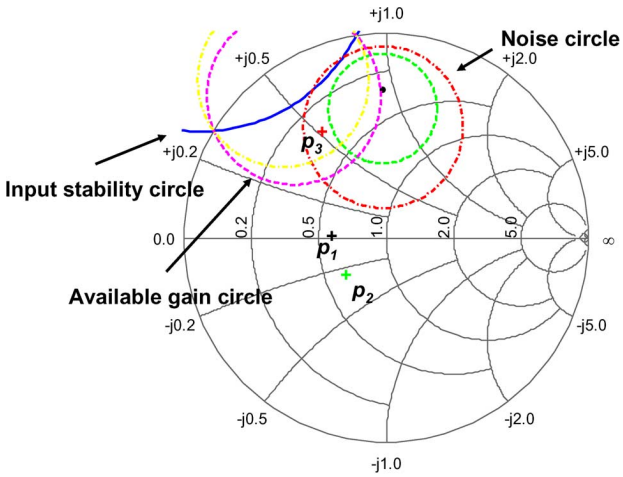
B. LNA

The LNA schematic is shown in Fig. 4(a), which consists of a five-stage SW-CPW-based CS amplifier (similar to [32]). Cascode topology is known to provide high gain and good input-output isolation for stability. However, it begins to lose its high gain advantage for operation frequencies close to the transistor's f_T, due to relatively large parasitic capacitance at the drain node of the CS transistor (intermediate node), and the substrate resistance of the common gate (CG) transistor. In addition, insufficient voltage headroom limits the dynamic range of cascode topology compared to CS structure. Although adding an inductor between the CS and CG stages [33], [34] can boost high-frequency gain by resonating out the parasitic capacitors, the low supply voltage in 65 nm CMOS still limits the cascode topology to achieve high gain and good linearity in W-band [35]. In addition, this inter-stage inductor leads to complex layout and larger chip area. This is because the drain of CS and source of CG stage in a cascode topology are normally shared to achieve a compact layout. In spite of the poor isolation between input and output of CS topology, it is possible to achieve good gain and noise figure using a CS LNA by proper design and careful layout of active and passive elements.

The matching is performed using SW-CPWs, where they are used as series and shunt stubs. The width and spacing of the SW-CPW are 10 μm and 20 μm, respectively, to achieve a characteristic impedance of 50 Ω. The alternate floating shields are implemented using the two lowest metal layers each with 1 μm width. In [31], it is shown that in matching networks, T-lines store mostly magnetic energy. Hence, the T-line's loss is mostly attributed to Q_L. At 90 GHz, a CS stage is conditionally stable. This means that the input and output matching networks of each stage have to be carefully designed to avoid stability issue [36]. Hence, the CS-based LNA design involves a trade-off between gain, stability and noise figure. Fig. 4(b) shows how the input matching is performed on the Smith chart. Input stability circle, available gain and noise figure circles are all overlaid on the same Smith chart. Starting from 50 Ω input, the pad and MIM



(a)



(b)

Fig. 4. (a) Five-stage LNA schematic. (b) LNA matching curve.

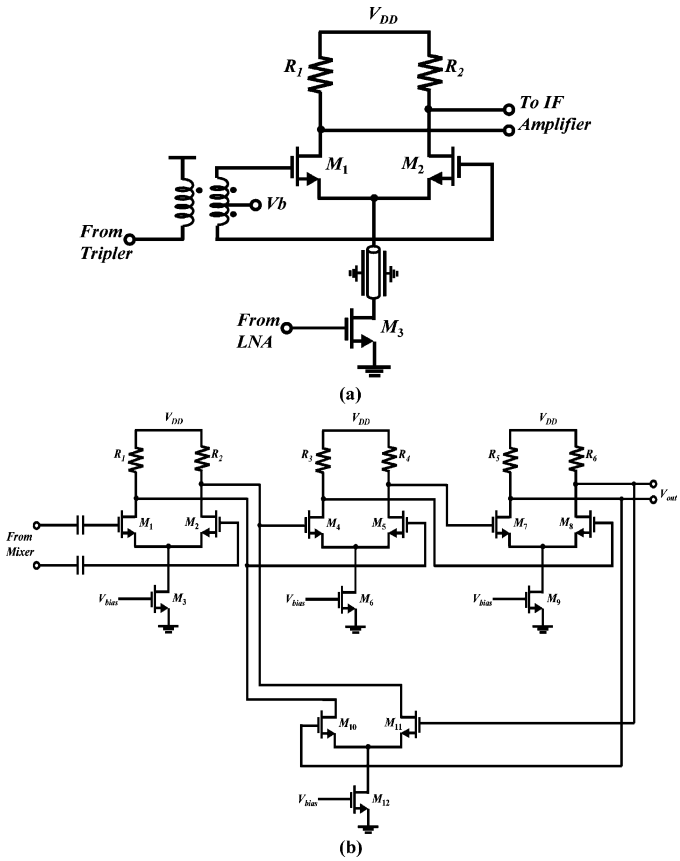


Fig. 5. Schematic of (a) mixer and (b) zero-IF amplifier.

capacitor move the impedance to point $p1$ and $p2$. The matching is finalized with series and shunt T-line (point $p3$). The design does not intend for optimum noise figure, as it would degrade gain and input matching. The output matching circuit is designed in a similar fashion, in which power gain circles together with the output stability circle are used to determine the optimum matching point.

The five-stage LNA takes advantage of accurate modeling of passive components and uses equally sized transistors to reduce the modeling inaccuracy in W-band. Both the input and output ports are matched to 50 Ω with pad's parasitic absorbed as part of the design for both direct and *in situ* probing. Each transistor is biased separately to balance between noise figure and gain. Small source degeneration inductors around 20 pH are introduced to model the non-ideal connection to the mesh-type ground plane. *RC* networks at the supply line and gate terminal of the transistor [shown in Fig. 4(a)] are included to ensure low-frequency stability of the amplifier. They prevent resonances between RF shunt capacitance and the inductance of the dc probes.

C. Mixer and Zero-IF Amplifier

The mixer's schematic is shown in Fig. 5(a). Since the IF frequency band (0.1–6 GHz) is far from the LO frequency (90 GHz), the LO feedthrough can be suppressed at the mixer's output, therefore, a single-balanced mixer is chosen for better noise performance. A SW-CPW T-line is inserted between the drain of M_3 and the common source node of $\mathrm{M}_{1,2}$ to increase the conversion gain of the mixer over the wide 6 GHz frequency range. A balun converts single-ended LO from the tripler to a differential signal. The simulated in-band (80–92 GHz) insertion loss of the on-chip balun is less than 2 dB. In order to minimize the gain and phase mismatch, the balun is placed close to the mixer in the layout. The mixer's output is connected to the input of the first-stage zero-IF amplifier. Fig. 5(b) shows the schematic of the amplifier. The input of the amplifier is AC-coupled with a low cut-off frequency at 100 MHz to remove the DC offset voltage from the mixer. In order to achieve the required 6 GHz bandwidth without using area inefficient inductors, an active feedback amplifier is utilized. Two active feedback amplifiers are cascaded to achieve 20 dB gain over the 6 GHz bandwidth [37]. To reduce the input-referred noise of the amplifier, a third-order gain stage with higher gain bandwidth product is chosen to reduce the number of stages to two [Fig. 5(b)].

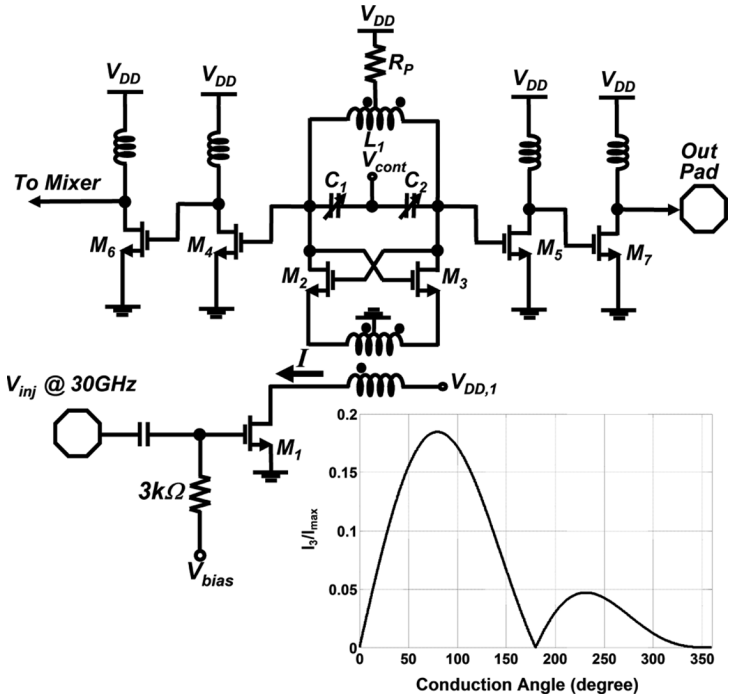


Fig. 6. Tripler schematic and normalized third harmonic amplitude under different conduction angles in the drain current of M1.

D. Tripler

The tripler is designed to cover a wide frequency range from 80 to 92 GHz to compensate for the frequency shift due to inaccurate passive modeling and parasitic of active devices, in addition to process variation. The tripler's schematic is shown in Fig. 6 [38], which consists of two parts: harmonic generation circuitry and injection-locked oscillator (ILO). The 30 GHz input signal is ac coupled to harmonic generator M1 which is biased to maximize third harmonic strength. The drain voltage of M1, $\mathrm{V_{DD,1}}$ in Fig. 6, is fed through the primary coil of the transformer. The stacked transformer is realized in the top two metal layers with 26 μm outer diameter and 4 μm metal width. The secondary coil is center-tapped to ground using lower metal layers for better port-to-port isolation. The simulated coupling coefficient is 0.71 at 90 GHz. The ILO tank consists of a center-tapped inductor with 35 pH half-inductance, two accumulation-mode varactors C1 and C2, and parasitic capacitance at the drain nodes of cross-couple pair (M2, M3). The one-turn octagonal center-tapped inductor L1 is built by shunting the top two metal layers to reduce resistive loss. Varactors (C1 and C2) are employed to tune the natural oscillation frequency of the ILO so as to further increase the locking range of the tripler. The common-mode resistor R_p is a 20 Ω poly-resistor which lowers the gate voltage of C1 and C2, therefore makes full use of the tuning capacity of the varactors to increase the tuning range of the ILO.

In order to have a wide locking range, it is highly desired to maximize the magnitude of the generated third-harmonic signal which is mainly determined by bias condition and the size of the transistor. The strength of the third harmonic component [39] can be expressed as

$$\frac{I_3}{I_{\max}} = \frac{\sin\left(\frac{3\phi}{2}\right)\cos\left(\frac{\phi}{2}\right) - 3\cos\left(\frac{3\phi}{2}\right)\sin\left(\frac{\phi}{2}\right)}{12\pi\left(1-\cos\frac{\phi}{2}\right)} \tag{3}$$

by normalizing the amplitude of third harmonic I_3 to that of overall drain current $I_{\max}$, shown in Fig. 6. Therefore, the optimal gate bias voltage can be achieved due to the relationship of the gate bias voltage with the conduction angle $\phi = 2\cos^{-1}((V_{th}-V_{bias})/V_i)$, where V_{th} is threshold voltage, V_{bias} is gate bias voltage and V_i is the input amplitude. In order to guarantee stable oscillation start-up accounting for PVT variation, the loop gain should be larger than two across the entire bandwidth. The transformer is EM simulated using Sonnet with all the losses taken into account, and the simulation result shows that the loop gain is above 2.5 for the whole frequency range.

V. PMMW Imaging Receiver Detector Baseband

A. Transistor Optimization for Maximum Second Order Nonlinearity of the CMOS Detector

In order to minimize the RX's NETD, not only the MMW front-end is designed to maximize gain with minimum noise added to the RX, the detector – which acts as a key block for signal-noise detection – is also designed for higher responsivity and lower NEP. This section describes the analysis of square-law characteristic of a short-channel transistor under different bias conditions. Unlike a long-channel transistor with square-law characteristic, a short-channel transistor has a super-linear I-V relationship, which limits the transistor's capability to generate even harmonics to increase the detector's

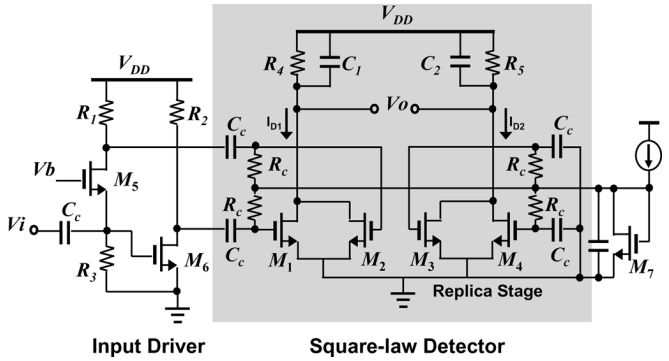


Fig. 7. Detector schematic.

responsivity. As will be explained in the following, by proper biasing, the short-channel transistor can generate relatively large second order harmonics to improve the detector responsivity and NEP.

The I-V equation of a MOS transistor using short-channel model is expressed as [40]

$$I_D = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{GS}-V_{TH})^2}{1+\left(\frac{\mu_0}{2\nu_{sat}L}+\theta\right)(V_{GS}-V_{TH})} \quad (4)$$

where μ_0 is the "low-field" carrier mobility, C_{ox} is the oxide capacitance per unit gate area, W and L are the channel width and length, V_{TH} is the threshold voltage, ν_{sat} is the carrier saturation velocity (about 10^7 cm/s), θ is a fitting parameter roughly equal to $(10^{-7}/t_{ox})\ \mathrm{V}^{-1}$, and t_{ox} is the oxide thickness. Equation (4) is rewritten as

$$I_D = I_{D0} + \sum_{n=1}^{\infty}\frac{f^{(n)}(V_{GS0}-V_{TH})}{n!}v_{gs}^n \quad (5)$$

where

$$I_{D0} = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{GS0}-V_{TH})^2}{1+\left(\frac{\mu_0}{2\nu_{sat}L}+\theta\right)(V_{GS0}-V_{TH})},$$

V_{GS0} is the gate bias voltage of the transistor, and ν_{gs} is the small-signal gate-source voltage. For small-signal detection, I_D is approximated as

$$I_D = I_{D0} + f'(V_{GS0}-V_{TH})v_{gs} + \frac{f''(V_{GS0}-V_{TH})}{2!}v_{gs}^2. \quad (6)$$

For an input signal below 100 mV, the truncation error for the second-order approximation in (6) will be within 0.002%. This approximation is sufficiently accurate, because in a PMMW system, the detector's input power normally varies from -40 to -20 dBm [19].

The combined output current of the differential pair M1–M2 in Fig. 7 can be expressed as

$$I_{D1} = 2I_{D0} + f''(V_{GS0}-V_{TH})v_{gs}^2. \quad (7)$$

The first-order harmonic of I_{D1} is canceled, while the second-order harmonic are added up. Moreover, the differential configuration of Fig. 7 (with drain terminals connected together) removes the first-order harmonic at the output. This is necessary for a broadband detector, because the presence of input signal at the output without sufficient filtering may overwhelm the weak second-order harmonic at the detector's output, leading to a reduction in responsivity. Considering that the replica stage shown in Fig. 7 provides a reference current of $I_{D2} = 2I_{D0}$, the output current of the detector is

$$I_o = I_{D1} - I_{D2} = f''(V_{GS0}-V_{TH})v_{gs}^2 \quad (8)$$

where

$$f''(V_{GS0}-V_{TH}) = \mu_0 C_{ox}\frac{W}{L}\left[1-3\left(\frac{\mu_0}{2\nu_{sat}L}+\theta\right)(V_{GS0}-V_{TH})\right].$$

Equation (8) shows that the output current is linearly proportional to the input power.

The relationship between $f''(V_{GS0}-V_{TH})$ and gate bias voltage with different transistor length is plotted in Fig. 8(a). The W/L ratio is kept constant for different channel length L to evaluate the dependence of $f''(V_{GS0}-V_{TH})$ on L. From Fig. 8(a), the maximum value of $f''(V_{GS0}-V_{TH})$ occurs in the moderate inversion region where the gate voltage is just above the threshold voltage. In addition, for smaller channel length, the $f''(V_{GS0}-V_{TH})$ will reduce. Such dependence matches well with what is predicted from (8).

The detector responsivity R_v is derived as follows:

$$R_v = \frac{V_o}{P_{\mathrm{in}}} = \frac{\frac{1}{2}\frac{\partial^2 i_d}{\partial v_{gs}^2}V_M^2 R_L}{\frac{V_M^2}{2R_0}} = \frac{f''(V_{GS0}-V_{TH})}{2}R_L R_0 \quad (9)$$

where R_0 is the real part of the detector's input impedance, and R_L is the load resistor at the output of the detector. Equation (9) states that maximizing $f''(V_{GS0}-V_{TH})$ will readily result in maximum responsivity.

The detector's NEP is determined by the detector output noise and detector responsivity. The detector's output noise is caused by channel's thermal noise, load resistor's thermal noise and transistor's 1/f noise. Therefore, the NEP becomes

$$NEP = \frac{\sqrt{N_o}}{R_v} = \frac{\sqrt{4kT\gamma g_m}R_L + \sqrt{4kTR_L} + \sqrt{\frac{K}{(C_{ox}WLf)}}g_m R_L}{R_v} \quad (10)$$

where

$$g_m = \mu_0 C_{ox}\frac{W}{L}\left[(V_{GS0}-V_{TH}) - \frac{3}{2}\left(\frac{\mu_0}{2\nu_{sat}L}+\theta\right)(V_{GS0}-V_{TH})^2\right].$$

It is observed that the minimum NEP happens when the detector responsivity R_v is maximized. In addition, transistors biased at the maximum detector's responsivity have lower g_m, which further reduces the detector NEP. Simulation result of the R_v and NEP with respect to gate bias voltage, shown in Fig. 8(b), proves

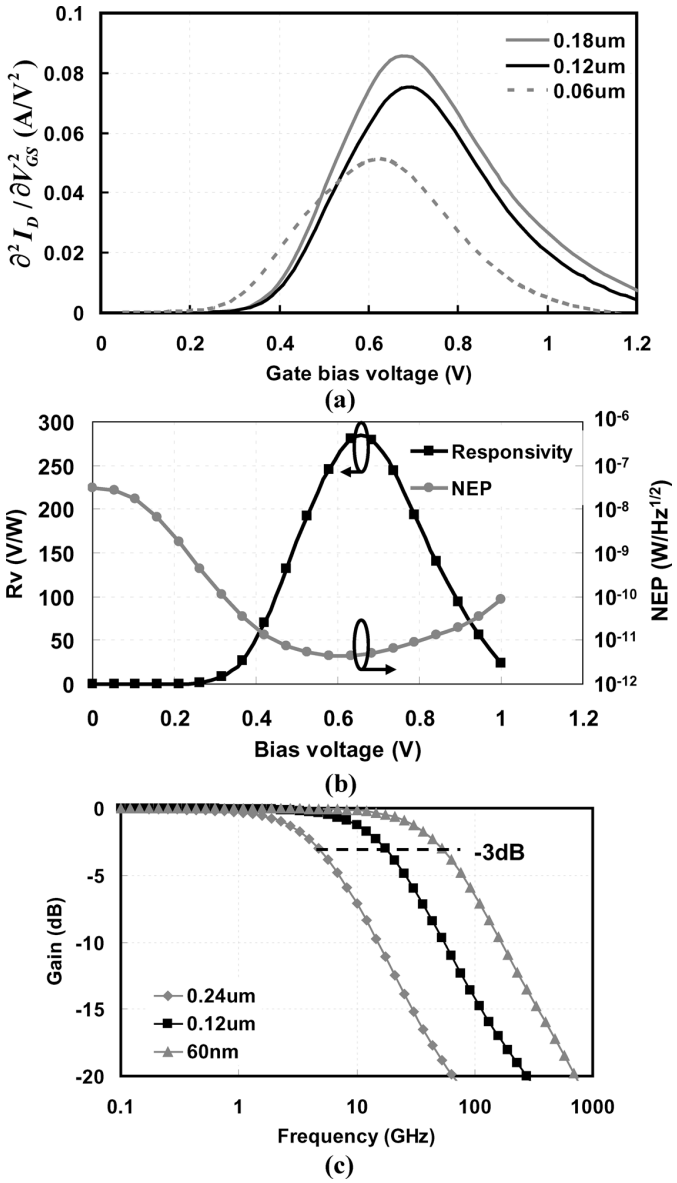


Fig. 8. (a) Transistor 2nd derivative of gate bias voltage with different length. (b) Simulation result of R_v and NEP versus gate bias voltage. (c) Detector bandwidth relationship with transistor length.

that by biasing the transistor in moderate inversion region, the detector can achieve the maximum responsivity and minimum NEP, simultaneously. In this simulation, the nMOS transistor's channel length and width are 0.12 μm and 32 μm, respectively, with a threshold voltage of 0.58 V. Additionally, the 1/f noise is minimized by using non-minimum length transistors. Although the above analytical study is based on simplified short-channel model for transistor in saturation region, it accurately predicts that the optimum detector's responsivity and NEP are achieved for the bias voltage around the threshold voltage.

Taking transistor's length as a parameter, we found that the detector achieves higher R_v and lower NEP by using longer length transistors, justifying the reason for using detectors at lower frequency rather than at RF frequency. Since the detector works as a non-linear circuit, small signal model does not suit to determine the detector's bandwidth. However, the signal bandwidth is only limited by the detector's input, because its output is DC voltage. Therefore, the 3-dB corner frequency of the detector is $f_{-3\mathrm{dB}} = 1/(2\pi R_S(C_{GS} + C_{GD}))$, where R_S is the source impedance, and C_{GS}, C_{GD} are the gate-source and gate-drain capacitors, respectively [41]. Although the power detector with a long channel device exhibits larger second-order harmonics and lower 1/f noise, its bandwidth will decrease. Simulation result in Fig. 8(c) shows the trade-off between transistor length and the detector bandwidth, which indicates that the length of 0.12 μm is optimum for 10 GHz bandwidth with maximum available responsivity.

B. Detector

Fig. 7 shows the core circuit of the square-law power detector. Transistors M1–M4 have the identical size and are biased at the same voltage V_{GS0}. M1 and M2 are configured as a pseudo differential pair to remove the first-order harmonics at the output. The bandwidth of the detector is also increased because of differential topology. A replica stage (M3 and M4) provides the DC component as a reference for detector to generate zero voltage output when input signal is zero. R4 and R5 convert the detector output from current to voltage domain. C1 and C2 at the output of the detector, combined with the resistors R4 and R5, build a first-order 400 MHz lowpass filter to filter out harmonic generated by the detector.

The pre-amp driving the detector is shown in Fig. 7. The pre-amp driver acts as an active balun to provide the differential signal to the input of the detector. Also, the pre-amp driver transfers the gate capacitance to match input 50 Ω to characterize input power during the test. The pre-amp driver is designed to achieve a 6 dB voltage gain with minimum NF for responsivity calibration, because in the fully integrated imager, the input impedance of the core detector is tuned to the preceding stage instead of 50 Ω. Since one output of the active balun needs relatively high resistor (200 Ω), the detector bandwidth is limited to 6 GHz due to the loading from the core detector.

C. Baseband Amplifier and Chopper

Following the detector is a two-stage Gilbert-cell-based amplifier to amplify in-band signal from the detector and filter out the out-of-band noise. The bandwidth of the VGA is designed to be 400 MHz, which covers up to fourth-order harmonics of a maximum 100 MHz chopper speed to avoid SNR degradation. In order to reduce the DC offset and 1/f noise at the detector's output, the input of VGA is AC-coupled with low cutoff frequency of 1 MHz. The gain of VGA can be tuned from -20 dB to 20 dB to adjust for different input power level to increase the RX's dynamic range.

The chopper is used to demodulate the modulated input signal back to the baseband by multiplying it with ± 1 in opposite phase of the control signal fed to the antenna switch. This chopping technique removes the RX noise from the modulated signal at the output of detector. Based on the structure of a passive mixer, transistors are biased at zero voltage to avoid introducing additional 1/f noise at the chopper's output. In order to increase switching speed, the chopper's input is also AC-coupled to the preceding VGA's output and biased at 0 V. A 50 Ω resistor is

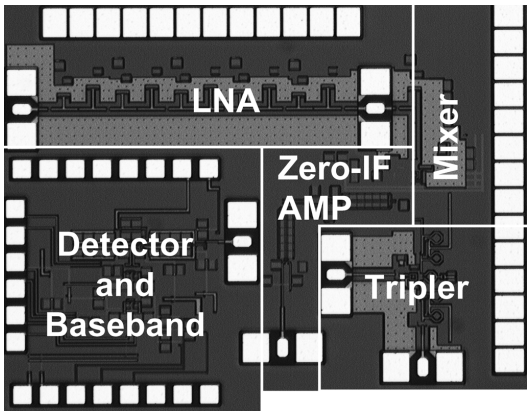


Fig. 9. Die photo of the receiver chipsets. Die size is 1.5×2 mm^2.

connected to the gate of the transistor to match the impedance of the pulse generator to avoid reflection. A non-silicided resistor is used at the output of the chopper, combined with an off-chip capacitor from testing equipment, to form a lowpass filter to average out the noise from the output signal. Since the delay time of the front-end and baseband detector is comparable to the switching period (ns), the front- and back-end choppers need to be synchronized for maximum DC voltage output.

VI. Experimental Results

The PMMW imager was fabricated in a 65 nm CMOS process with seven metal layers. In order to report the measured results of both MMW front-end and baseband building blocks and the entire system, a hybrid method using on-wafer testing and chip-on-board measurements was carried out. Stand-alone front-end and baseband are tested on-wafer, while two chipsets are bonded on a RO4003 board to test the system performance of the imager. The die photo of the 1.5×2 mm^2 passive imaging chipset is shown in Fig. 9.

A. Front-End

The LNA exhibits a wideband input matching, a measured peak gain of 15 dB, minimum NF of 7 dB and a -3 dB BW of 12 GHz, as shown in Fig. 10(a). At room temperature, the front-end RX has 35 dB of measured gain and 9 dB of measured NF, shown in Fig. 10(b). The LNA, mixer/buffer, and the zero-IF amplifier consume 42 mW, 16 mW, and 30 mW, respectively, from a 1.2 V supply.

B. Tripler

The phase noise of the locking state is shown in Fig. 11(a). The 9.8 dB at 2 kHz frequency offset phase noise degradation compared to the input signal shows that the tripler contribute less to the LO's phase noise. The measured maximum locking range of the tripler is shown in Fig. 11(b), which shows 11% locking range to cover the 86 GHz LO frequency for process variation. The supply voltage of the tripler is 0.8 V.

C. Detector

The on-chip buffer enables to bring out the detector signals separately. The detector itself achieves a maximum responsivity of 4500 V/W at 0.5 V gate bias voltage, which matches well with

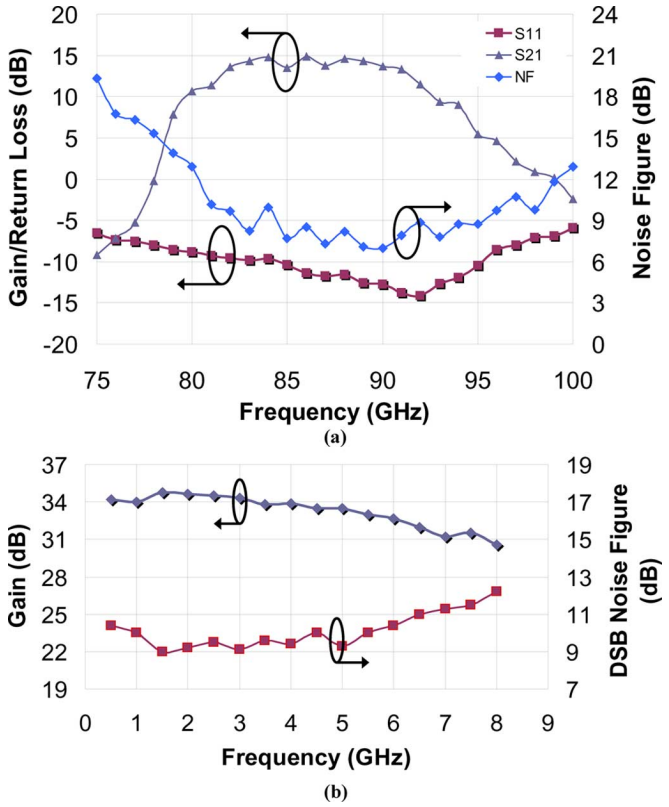


Fig. 10. Front-end measurement results. (a) LNA S-parameters and NF. (b) Front-end receiver gain and NF.

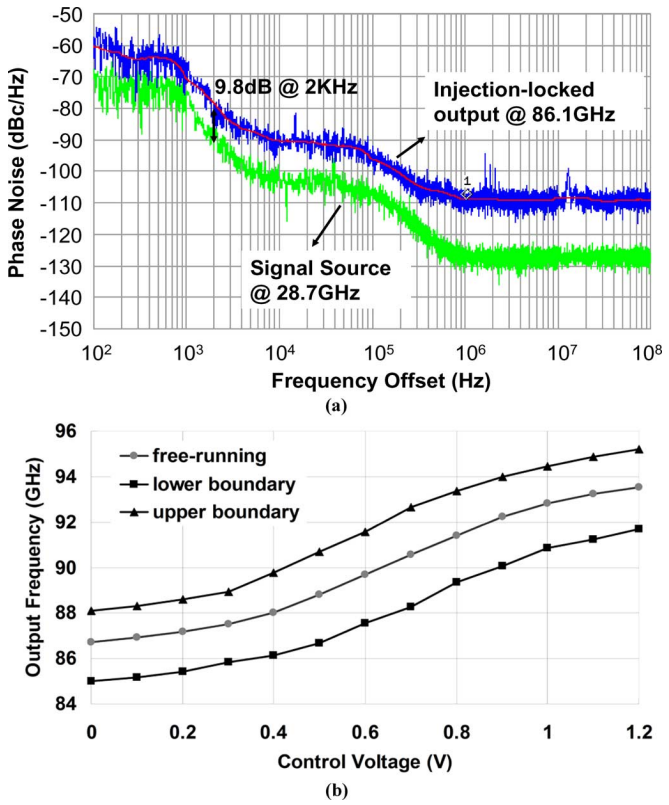


Fig. 11. Frequency tripler measurement results. (a) Phase noise comparison of frequency tripler and inject source signal. (b) Tuning range of the frequency tripler.

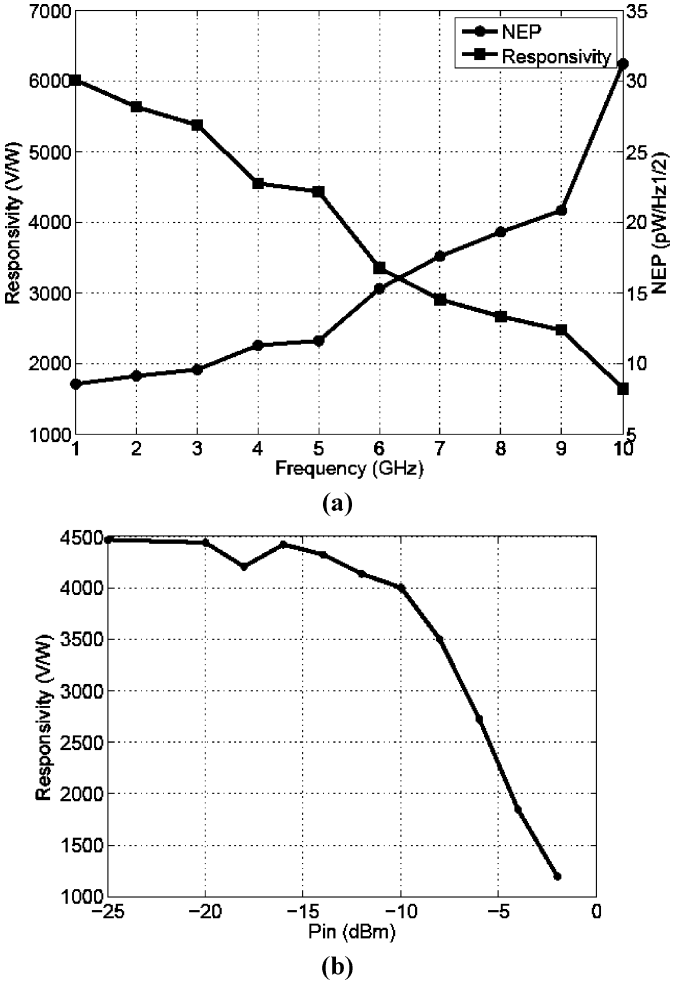


Fig. 12. (a) Detector responsivity and NEP versus frequency. (b) Detector responsivity versus input power.

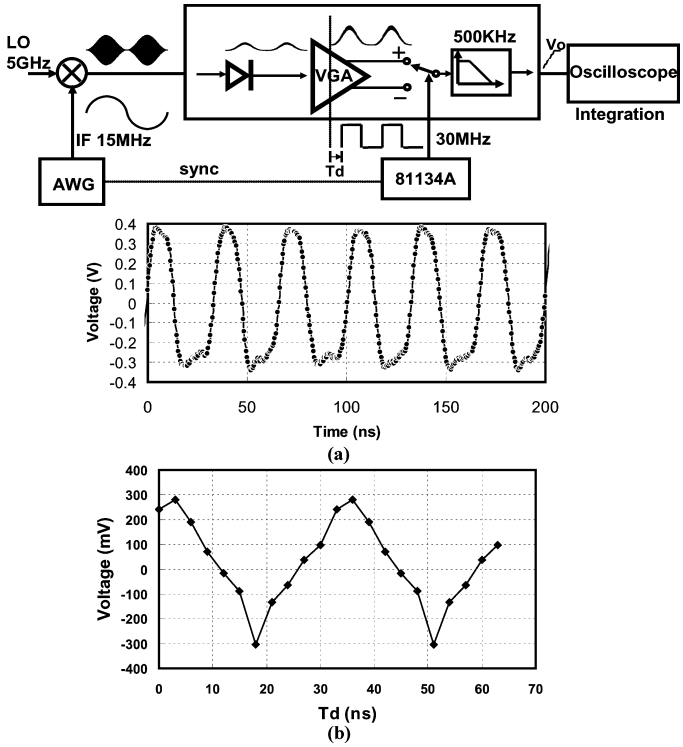


Fig. 13. Baseband chipset measurement setup and measurement results. (a) VGA output voltage waveform. (b) Baseband output voltage versus delay between the front-end and baseband clocks.

the optimum bias voltage in the simulation using BSIM4 model. In order to verify the wideband performance of the detector, the input signal source is swept from 1 GHz to 10 GHz with power of -25 dBm, together with detector responsivity, is shown in Fig. 12(a). As mentioned before, due to the high impedance node at the pre-amp's output, the detector's responsivity drops to 3200 V/W at 6 GHz, which is nearly half of the responsivity at 1 GHz. The measured NEP is also plotted on the right with minimum NEP of 8.54 $\mathrm{pw}/\mathrm{Hz}^{1/2}$ achieved at 1 GHz with higher detector responsivity. Fig. 12(b) shows the detector responsivity relative to the input power at 5 GHz. The measured $\mathrm{P}_{1\mathrm{dB}}$ of the detector, which is defined as the input power when detector responsivity drops 1 dB, is -9 dBm. The supply voltage of the detector is 1.5 V.

D. Baseband Chipset

An AM-modulation input is used for testing purpose and to emulate Dicke switch functionality. This approach makes it easier to measure the detector's responsivity. Before connecting to the front-end chipset, the AM modulated signal, resembling the output of front-end chipset, is fed to the baseband chipset to test the functionality of the detector, VGA and the chopper with low-pass filter. Fig. 13 shows the setup of baseband chipset measurement. Although the signal generator provides AM modulated signal directly, the internal modulated frequency cannot go higher than 1 MHz. Since the 1/f noise corner is around 100 MHz, an alternative approach similar to two-tone test is used here to achieve a higher modulation frequency. The input pseudo AM modulated signal is generated by an up-conversion mixer with 5 GHz LO and 15 MHz IF frequency. Since the pseudo AM modulated signal only contains two tone symmetric around 5 GHz, the detector converts the signal into DC and $2 * \mathrm{IF}$ frequency by square law function. The DC component is filtered out by the VGA's high pass filter at the input. By enabling on-chip buffer to the output, the measured modulated square wave at the output of the VGA is shown in Fig. 13(a). By changing the controlled voltage, the output of the VGA is also changing accordingly to different gain setting. Therefore, the dynamic range of the passive imaging can be increased. As the switching speed increases, the front- and back-end switches need to be synchronized to avoid SNR degradation. The chopper's control signal is set to twice the IF frequency, because the VGA's output signal is at twice IF frequency due to the pseudo AM modulated input signal. Fig. 13(b) shows different delay between input and clock control of the chopper leads to different output voltage.

E. Receiver Chipsets

The front-end and baseband chipsets are wire-bonded to the PCB board (shown in Fig. 14) to characterize system measurement. Since the output signal of front-end has a large bandwidth of 6 GHz, the RO4003 substrate was used to reduce the signal loss and noise coupling from the board substrate. The

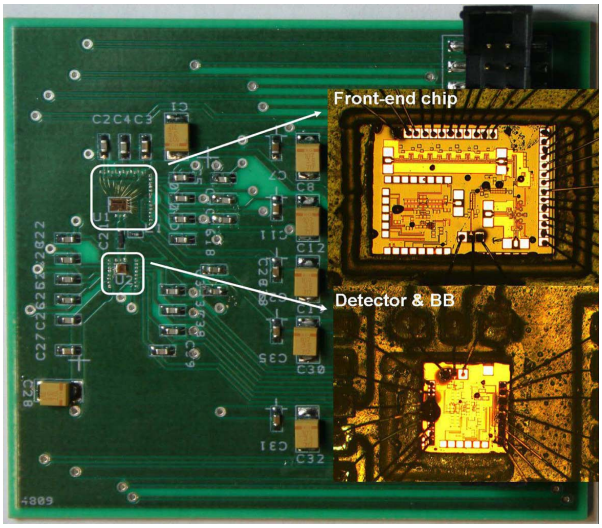


Fig. 14. Board photo.

signal is fed through a MMW waveguide probe to the input of the front-end chipset. After frequency conversion and amplification, the IF signal is brought to the board via wirebond and fed to the input of the baseband chipset. The output of the baseband chipset is probed and measured. All DC supply voltages provided on-board are fed to the chipsets through wirebond. A bias-tee using off-chip high-quality inductor and capacitor is inserted between front-end and baseband chipsets as an open-drain buffer to the front-end. The inductance and capacitance are 6.8 nH and 5.6 pF, respectively. Carefully chosen self-resonate frequency (SRF) minimizes the insertion loss of the bias-tee, which is modeled in the simulation. Two chipsets are put close to the bias-Tee to reduce the bondwire length. The EM and estimated inductance is around 1 nH. Ground pads are also bonded to reference the signal to the same ground so as to reduce the return-current discontinuities of the two chipsets. The distance between two GSG pads is 5 mm.

In order to demonstrate the Dicke switching concept and mitigate 1/f noise, a two-tone signal, similar to the one used in baseband measurement, is generated to emulate the AM-modulated signal. Fig. 15 shows the measured responsivity and NEP of the radiometer with input power at 91 GHz. The 91 GHz frequency was chosen to ensure that worse-case responsivity is accounted for in the measured plot of Fig. 15. The input 1-dB compression point is roughly -44 dBm, which is high enough for passive imaging application. Fig. 15 shows measured and expected responsivity and NEP of the RX chipset with respect to frequency ($P_{\rm in} = -55$ dBm). The peak responsivity and minimum NEP of the radiometer are 16 MV/W and 6.13 fW/Hz$^{1/2}$ respectively, which are measured at 88 GHz. The frequency dependency of responsivity in Fig. 15 is, in fact, caused partially by the input pre-amp to the detector (specifically used to measure input power of the detector) as well as off-chip interconnect. The input pre-amp does not use any BW-enhancing inductors and provides 50 Ω input impedance matching without adding significant noise to overall detector NEP. The frequency response of the detector's responsivity includes the frequency response of the pre-amp. The total system NETD is 1.28K, which is based on

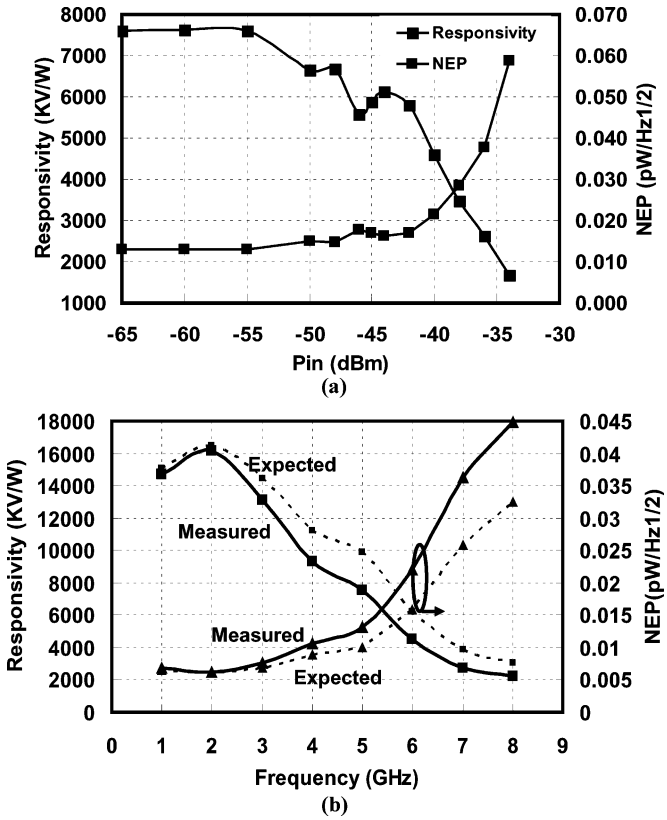


Fig. 15. (a) Responsivity and NEP of the receiver with input power. (b) Responsivity and NEP of the receiver with input frequency.

TABLE I
PERFORMANCE SUMMARY OF THE RECEIVER CHIPSETS

Front-end		Baseband	
LNA + Mixer + Zero-IF		Detector	
Gain (dB)	35	Responsivity (V/W)	6000
Noise Figure (dB)	8.9	NEP (pW/Hz$^{1/2}$)	8.54
Bandwidth (GHz)	12 (80 ~ 92)	VGA + Chopper + LPF	
Tripler		Gain (dB)	20
Locking Range (GHz)	85~95	Bandwidth (MHz)	400
		LPF BW (Hz)	500K
System			
Responsivity (kV/W)	16147	Average NEP (fW/Hz$^{1/2}$)	8.8
3dB Bandwidth (GHz)	81 ~ 91		
Integration Time (ms)	30	NETD (K)	1
Power (mW)			
Front-end	93.2	Baseband	8.4
Technology	65nm CMOS	Size (mm x mm)	1.5 x 2

the average NEP over the 5 GHz IF bandwidth (given a 20 ms integration time) [42]. The reason to use 5 GHz bandwidth instead of the 10 GHz RF bandwidth is because the advantage of DSB NF in the mixer has been used in the NEP. That means it cannot be exploited again in NETD's calculation [19]. If the integration time increases to 30 ms, the total system NETD can be reduced to 1K, which is acceptable for imaging application. Table I summarizes the performance of the Rx chipsets. Considering the

TABLE II
COMPARISON OF STATE-OF-THE-ART W-BAND FRONT-END

	Frequency (GHz)	Technology f_t/f_{max} (GHz)	Front-end Gain (dB)	Front-end NF (dB)	Front-end P1dB (dBm)	Power (mW)	Area (mm^2)
[9]	85 - 96	SiGe HBT f_{max} = 300	31	5.2	-30	700	1.02
[43]	75 - 91	65nm CMOS	13	7.5	-16	89	0.23
[44]	73 - 81	SiGe	46	7.0	-38	195	1.7
[45]	77 - 83	SiGe	37	8	-27.5	161	2.25
[47]	94	SiGe	20	12	-31	148.5	0.1
This work	80 - 92	65nm CMOS	35	8.9	-40	93.2	2

TABLE III
COMPARISON OF STATE-OF-THE-ART W-BAND RADIOMETER. (ALL NETD CALCULATIONS ARE BASED ON THE SAME 30 MS INTEGRATION TIME)

	Frequency (GHz)	Technology f_t/f_{max} (GHz)	Responsivity (kV/W)	Average NEP	NEdT (K)	Power (mW)	Area (mm^2)
[48]	94GHz 8x8 array	Microbolometer	0.017	19	450	N/A	N/A
[49]	89.5 - 93.5	Discrete component	N/A	0.003	0.5	N/A	N/A
[50]	94	0.13um InP HEMT	485	0.0001	1	60*	2.75*
[18]#	81 – 93	65nm CMOS	210	0.09	4.4	39.6	0.41
[42]#	85 – 99	0.12um SiGe	5000	0.021	0.83	34.8	0.4
This work	81 - 91	65nm CMOS	16147	0.009	1	101.6	3

* means LNA only
\# means on-chip switch

2.3 dB insertion loss of the Dicke switch [42], the total system NETD increases to 2.2K (given a 20 ms integration time). Although the NETD with Dicke switch exceeds the 1K requirement, it is possible to reduce the NETD if the RX's bandwidth increases. Assuming the same average NEP (8.8 fW/Hz$^{1/2}$) with 11 GHz bandwidth, the RX's NETD with on-chip Dicke switch can be reduced to 1K with a 20 ms integration time. The expected responsivity and NEP of two chipsets, calculated from separate measurement of front-end and baseband, are also shown in Fig. 15. The chipsets are expected to achieve a total responsivity of 16.5 MV/W and an NEP of 6.07 fW/Hz$^{1/2}$. The measured performance is close to the expected one, which verifies that the board implementation introduces negligible performance degradation. In addition, the system bandwidth can be further increased to 5.5 GHz if two chipsets are integrated together, as shown in the expected responsivity curve. Considering the average NEP of 7.6 fW/Hz$^{1/2}$ over 5.5 GHz bandwidth, the two chipsets are expected to achieve a NETD of 1K with a 20 ms integration time. The performance of the W-band receiver front-end and radiometer are summarized and compared with the state-of-the-art in Tables II and III respectively.

VII. CONCLUSION

A W-band CMOS radiometer front-end and detector baseband chipset solution has been presented. System level considerations have been described to address several problems facing in the implementation of a practical PMMW radiometer using advanced CMOS technology. A direct-conversion RX front-end with a frequency tripler and a baseband detector architecture was implemented. The two chipsets exhibits a total responsivity of 16 MV/W, NEP of 6.13 fW/Hz$^{1/2}$ and a Dicke NETD of 1.28K with a 20 ms integration time. Given 30 ms integration time, the total system NETD can be deduced to 1K, which demonstrates the feasibility of using CMOS for future generations of low-cost multi-pixel portable passive imaging cameras.

ACKNOWLEDGMENT

The authors would like to thank Fujitsu Labs of America for chip fabrication and support, in particular, W. Walker and Dr. M. Wiklund. They would like to acknowledge Prof. Rebeiz of UCSD for allowing access to the MMW measurement facility. They would also like to thank Agilent and Lecroy for providing equipment and Dr. V. Jain of Sabertek for technical discussion.

REFERENCES

[1] C. Martin *et al.*, "Advances in millimeter-wave imaging technology for enhanced vision systems," in *Proc. Digital Avionics Systems Conf.*, Dec. 2002, pp. 11D4-1–11D4-8.

[2] M. R. Fetterman *et al.*, "Simulation, acquisition and analysis of passive millimeter-wave images in remote sensing applications," *Opt. Express*, vol. 16, pp. 20503–20515, Dec. 2008.

[3] R. Appleby *et al.*, "Millimeter-wave and submillimeter-wave imaging for security and surveillance," *IEEE Proc.*, vol. 95, no. 8, pp. 1683–1690, Aug. 2007.

[4] "Assessment of Millimeter-Wave and Terahertz Technology for Detection and Identification of Concealed Explosives and Weapons," National Research Council, National Academies Press, 2007.

[5] S. Oka *et al.*, "Latest trends in millimeter-wave imaging technology," *Progress in Electromagnetics Research Lett.*, vol. 1, pp. 197–204, 2008.

[6] L. Yujiri *et al.*, "Passive millimeter wave imaging," *IEEE Microwave Mag.*, vol. 4, no. 3, pp. 39–50, Sep. 2003.

[7] C. Marcu *et al.*, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 314–315.

[8] A. Tomkins *et al.*, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2085–2099, Aug. 2009.

[9] S. T. Nicolson *et al.*, "Single-chip W-band SiGe HBT transceivers and receivers for doppler radar and millimeter-wave imaging," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2206–2217, Oct. 2008.

[10] V. Jain *et al.*, "A single-chip dual-band 22-to-29 GHz/77-to-81 GHz BiCMOS transceiver for automotive radars," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 314–315.

[11] Y. Kawano *et al.*, "A 77 GHz transceiver in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 310–311.

[12] E. Laskin *et al.*, "A 95 GHz receiver with fundamental-frequency VCO and static frequency divider in 65 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 180–605.

[13] E. Ojefors and U. Pfeiffer, "A 94-GHz monolithic front-end for imaging arrays in SiGe:C technology," in *Proc. Microwave Integrated Circuit Conf.*, Oct. 2008, pp. 422–425.

[14] A. Tomkins *et al.*, "A 94 GHz SPST switch in 65 nm bulk CMOS," in *Proc. Compound Semiconductor Integrated Circuits Symp. (CSICS)*, Oct. 2008, pp. 1–4.

[15] W. Winkler *et al.*, "94 GHz amplifier in SiGe technology," in *Proc. Microwave Integrated Circuit Conf.*, Oct. 2008, pp. 167–170.

[16] E. Ojefors *et al.*, "A 0.65 THz focal-plane array in a quarter-micron CMOS process technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1968–1976, Jul. 2009.

[17] J. W. May and G. M. Rebeiz, "High-performance W-band SiGe RFICs for passive millimeter-wave imaging," in *Radio Frequency Integrated Circuits Symp. Dig.*, Jun. 2009, pp. 437–440.

[18] A. Tomkins *et al.*, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981–1991, Oct. 2010.

[19] N. Skou and D. L. Vine*, Microwave Radiometer Systems: Design and Analysis*, 2nd ed. Boston, MA: Artech House, 2006.

[20] M. Tiuri, "Radio astronomy receivers," *IEEE Trans. Antennas Propagat.*, vol. AP-12, no. 7, pp. 930–938, Dec. 1964.

[21] A. H. Lettington *et al.*, "Passive millimetre-wave imaging architectures," *J. Optics A: Pure and Applied Optics*, vol. 5, pp. S103–S110, 2003.

[22] P. J. Rice *et al.*, "Development of a low cost 94 GHz imaging receiver using multi-layer liquid crystal polymer technology," in *Proc. SPIE*, May 2008, vol. 6948, pp. 694809-1–694809-11.

[23] R. H. Dicke, "The measurement of thermal radiation at microwave frequencies," *Rev. Sci. Instrum.*, vol. 17, pp. 268–275, Jul. 1946.

[24] W. Deal, L. Yujiri, M. Siddiqui, and R. Lai, "Advanced MMIC for passive millimeter and submillimeter wave imaging," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 572–573.

[25] H. Kim *et al.*, "SiGe IC-based mm-wave imager," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2007, pp. 1975–1978.

[26] L. Gilreath *et al.*, "A 94-GHz passive imaging receiver using a balanced LNA with embedded Dicke switch," in *IEEE RFIC Symp.*, May 2010.

[27] K.-H. Tsai and S.-I. Liu, "A 43.7 mW 96 GHz PLL in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 276–277.

[28] M. Sato *et al.*, "Advanced MMIC receiver for 94-GHz band passive millimeter-wave imager," *IEICE Trans. Electron.*, vol. E92.C, no. 9, pp. 1124–1129, 2009.

[29] T. S. D. Cheung *et al.*, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2003, pp. 396–501.

[30] M. Repossi *et al.*, "Design of low-loss transmission lines in scaled CMOS by accurate electromagnetic simulations," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2605–2615, Sep. 2009.

[31] C. H. Doan *et al.*, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[32] M. Varonen *et al.*, "Millimeter-wave integrated circuits in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1991–2002, Sep. 2008.

[33] T. Suzuki *et al.*, "A 90 Gb/s 2:1 multiplexer IC in InP-based HEMT technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 192–193.

[34] X. Li *et al.*, "A novel design approach for GHz CMOS low noise amplifiers," in *Proc. IEEE Radio and Wireless Conf.*, Aug. 1999, pp. 285–288.

[35] S. Pellerano *et al.*, "A 64 GHz LNA with 15.5 dB gain and 6.5 dB NF in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1542–1552, Jul. 2008.

[36] K. Kwok and J. R. Long, "Bilateral design of mm-wave LNA and receiver front-end in 90 nm CMOS," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2008, pp. 181–184.

[37] H.-Y. Huang *et al.*, "A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1111–1120, May 2007.

[38] Z. Chen and P. Heydari, "An 85–95.2 GHz transformer-based injection-locked frequency tripler in 65 nm CMOS," in *2010 IEEE MTT-S Int. Microwave Symp. Dig.*, May 2010.

[39] S. A. Maas*, Nonlinear Microwave and RF Circuits*, 2nd ed. Norwood, MA: Artech House, 2003.

[40] B. Razavi*, Design of Analog CMOS Integrated Circuits*. Boston, MA: McGraw-Hill, 2001, pp. 588–589.

[41] Y. Zhou and M. Y.-W. Chia, "A low-power ultra-wideband CMOS true RMS power detector," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1052–1058, May 2008.

[42] J. W. May and G. M. Rebeiz, "Design and characterization of W-band SiGe RFICs for passive millimeter-wave imaging," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1420–1430, May 2010.

[43] M. Khanpour *et al.*, "A wideband W-band receiver front-end in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1717–1730, Aug. 2008.

[44] J. Powell *et al.*, "SiGe receiver front ends for millimeter-wave passive imaging," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 11, pp. 2416–2425, Nov. 2008.

[45] A. Babakhani *et al.*, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[46] A. Natarajan *et al.*, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local LO-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[47] E. Ojefors and U. Pfeiffer, "A 94-GHz monolithic front-end for imaging arrays in SiGe:C Technology," in *Proc. European Microwave Integrated Circuits Conf.*, Oct. 2008, pp. 422–425.

[48] C. Middleton *et al.*, "Passive millimeter-wave focal plane array," in *Conf. Dig. 2004 Joint 29th Int. Conf. Infrared and Millimeter Waves, 12th Int. Conf. Terahertz Electronics*, Oct. 2004, pp. 745–746.

[49] Q. Lin *et al.*, "The W band radiometer for imaging," in *Proc. Int. Conf. Communication, Cirtuits and Systems*, Jul. 2007, pp. 1306–1308.

[50] M. Sato *et al.*, "Compact receiver module for a 94 GHz band passive millimetre-wave imager," *IET Microw., Antennas Propag.*, vol. 2, no. 8, pp. 848–853, Dec. 2008.

Lei Zhou (S'05) received the B.Eng. degree in electrical engineering from Huazhong University of Science and Technology (HUST), Wuhan, China, in 2002, the M.Eng. degree from the Department of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore, in 2005, and the Ph.D. degree in electrical and computer engineering from University of California, Irvine, in 2010.

He was with Institute of Microelectronics, Singapore, in 2003, where he did his Master research on analog correlator design for IR-UWB receivers. He worked at Atheros Communication, Inc. and at Broadcom Corp. as a Design Engineer intern in summers 2006, 2007 and 2009. He is now with Quantenna Communications, Inc. as a Staff RFIC Design Engineer. His research interests include analog/RF/MMW integrated circuit design for wireless communication systems.

Chun-Cheng Wang (S'07) received the B.S. and M.Eng. degrees in electrical and computer engineering from Cornell University, Ithaca, NY, in 2003 and 2004, respectively. From 2004 to 2007 he was with Realtek Semiconductor Corp. as an Analog/RF Design Engineer. He is currently a Ph.D. candidate at the University of California, Irvine.

His research interests are in RF and millimeter-wave (mmW) integrated circuit design for wireless communications, automotive radars, and imaging applications. He held a summer internship position at Fujitsu Laboratories of America, Sunnyvale, CA.

Mr. Wang was the recipient of the 2010 Center of Pervasive Communications and Computing (CPCC) Fellowship, 2009 School of Engineering Research and Travel Grant Award and the 2007 EECS Department Fellowship at University of California, Irvine. He is a member of Eta Kappa Nu.

Zhiming Chen (S'08) received the B.Eng. degree in electronic engineering from Tsinghua University, Beijing, China, in 2007, and the M.S. degree in electrical engineering from the University of California, Irvine, in 2009, where he is currently pursuing the Ph.D. degree in electrical engineering.

He has been with the Nanoscale Communication IC Lab at the University of California, Irvine, since 2007. He was a summer intern at Finisar Corporation, Sunnyvale, CA, in 2008. He has also held a five-month internship with Broadcom Corporation, Irvine, in 2010, where he was engaged in 60 GHz radio development. His research interests include RF/MMW integrated circuits design with a focus on W-band imaging systems.

Payam Heydari (S'98–M'00–SM'07) received the B.S. and M.S. degrees (with honors) in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1992 and 1995, respectively. He received the Ph.D. degree in electrical engineering from the University of Southern California, Los Angeles, in 2001.

During the summer of 1997, he was with Bell Labs, Lucent Technologies, Murray Hill, NJ, where he worked on noise analysis in deep-submicron very large-scale integrated (VLSI) circuits. During the summer of 1998, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he worked on gradient-based optimization and sensitivity analysis of custom-integrated circuits. In August 2001, he joined the University of California, Irvine, where he is currently a Professor of Electrical Engineering. His research interests include the design of high-speed analog, radio-frequency (RF), and mixed-signal integrated circuits. He is the author/coauthor of one book and more than 80 journal and conference papers.

Dr. Heydari is the co-recipient of the 2009 Business Plan Competition First Place Prize Award and Best Concept Paper Award both from Paul Merage School of Business at UC Irvine. He is the recipient of the 2010 Faculty of the Year Award from UC Irvine's Engineering Student Council (ECS), the 2009 School of Engineering Fariborz Maseeh Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin–Cauer Award, the 2005 National Science Foundation (NSF) CAREER Award, the 2005 IEEE Circuits and Systems Society Darlington Award, the 2005 UCI's School of Engineering Teaching Excellence Award, the Best Paper Award at the 2000 IEEE International Conference on Computer Design (ICCD), the 2000 Honorable Award from the Department of EE-Systems at the University of Southern California, and the 2001 Technical Excellence Award in the area of Electrical Engineering from the Association of Professors and Scholars of Iranian Heritage (APSIH). He was recognized as the 2004 Outstanding Faculty at the EECS Department of the University of California, Irvine. His research on novel low-power multi-purpose multi-antenna RF front-ends received the Low-Power Design Contest Award at the 2008 IEEE International Symposium on Low-Power Electronics and Design (ISLPED).

Dr. Heydari currently serves on the Technical Program Committees of Compound Semiconductor IC Symposium (CSICS), Custom Integrated Circuits Conference (CICC) and International Symposium on Low-Power Electronics and Design (ISLPED). He was a Guest Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2007–2009, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2006 to 2008. He was the Student Design Contest Judge for the DAC/ISSCC Design Contest Award in 2003, the Technical Program Committee member of the IEEE Design and Test in Europe (DATE), International Symposium on Quality Electronic Design (ISQED), and International Symposium on Physical Design (ISPD).