A Fully-Integrated Dual-Polarization 16-Element W-band Phased-Array Transceiver in SiGe BiCMOS

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Abstract — **This paper presents a multi-function, dual-polarization phased array transceiver supporting both radar and communication applications at W-band. 32 receive elements and 16 transmit elements with dual outputs are integrated to support 16 dual polarized antennas in a package. The IC further includes two independent 16:1 combining networks, two receiver down-conversion chains, an up-conversion chain, a 40GHz PLL, an 80GHz frequency doubler, extensive digital control circuitry, and on-chip IF/LO combining/distribution circuitry to enable scalability to arrays at the board level. The fully-integrated transceiver is fabricated in the IBM SiGe BiCMOS 0.13um process, occupies an area of 6.6X6.7mm^2, and operates from 2.7V (analog/RF) and 1.5V (digital) supplies. Multiple operating modes are supported including the simultaneous reception of two polarizations with a 10GHz IF output, transmission in either polarization from an IF input, or single-polarization transmission/reception from/to I&Q base-band signals (2.5W RX, 2.9W TX). Measurement results show 8dB receiver NF and 2dBm transmitter output power per element at 94GHz in both polarizations.**

Index Terms — **W-band, dual polarized, SiGe, phased-array.**

I. Introduction

The large available bandwidths, short wavelengths, and ability to operate in dusty and foggy conditions have made millimeter-wave (mmWave) frequencies attractive for high data-rate communication and high-resolution imaging applications. Dual-polarized phased arrays, in particular, can provide advantages to imaging systems in environments with degraded visibility [1-3]. These target usage scenarios can be collectively addressed by adopting a multifunctional design approach, which is advantageous for host systems requiring multiple mmWave sensors and communication devices [1]. The high levels of integration and availability of both high-frequency bipolar devices and low-power digital CMOS make SiGe BiCMOS technologies well-suited for this task. Recently, various phased arrays operating at W-band have been demonstrated in SiGe [4-7]. These previously reported ICs have not integrated complete transmitter and receiver functions on the same die and do not support two antenna polarizations.

This paper summarizes the design and measurement of a SiGe BiCMOS W-band (~94 GHz) phased-array transceiver IC with an in-package antenna array, suitable for building larger scalable arrays at the board level by tiling packaged ICs adjacent to one another. The design targets radar and active imaging applications where light weight and low volume are important considerations; it also supports communication.

In order to realize the vision of a highly-versatile, scalable, monolithic W-band phased array transceiver, this work addresses the following main challenges: (1) architecture design to support the simultaneous reception of two polarizations or transmission in either polarization, (2) transceiver front-end LNA, PA and switch co-design to attain the lowest possible NF, (3) circuit-package co-design to support array scalability at the board level, (4) aggressive physical design to integrate all the desired functionality in a form factor small enough to be compatible with $\lambda/2$ (~1.6mm) antenna spacing, (5) mmWave-digital co-design to achieve system configurability in tens of nanoseconds.

II. Dual-Polarization Transceiver Architecture and Implementation

As illustrated in Fig. 1, the receiver (RX) portion of the IC consists of 32 RF phase-shifting front-ends, arranged in two groups of 16 elements, one for each antenna polarization. Each 16-element sub-array features an independent power combiner and down-conversion mixer to support simultaneous reception in both polarizations (H and V). A common frequency synthesizer and doubler provide the local-oscillator (LO) signal for both RX sub-arrays, as well as the transmitter (TX) up-conversion. A double-conversion superheterodyne architecture with sliding IF is employed, with the ~83 GHz LO at 8/9 of the RF frequency, and providing RX outputs (H and V) at both IF (RF/9 or ~10.4 GHz) and baseband (BB), to support a variety of system architectures.

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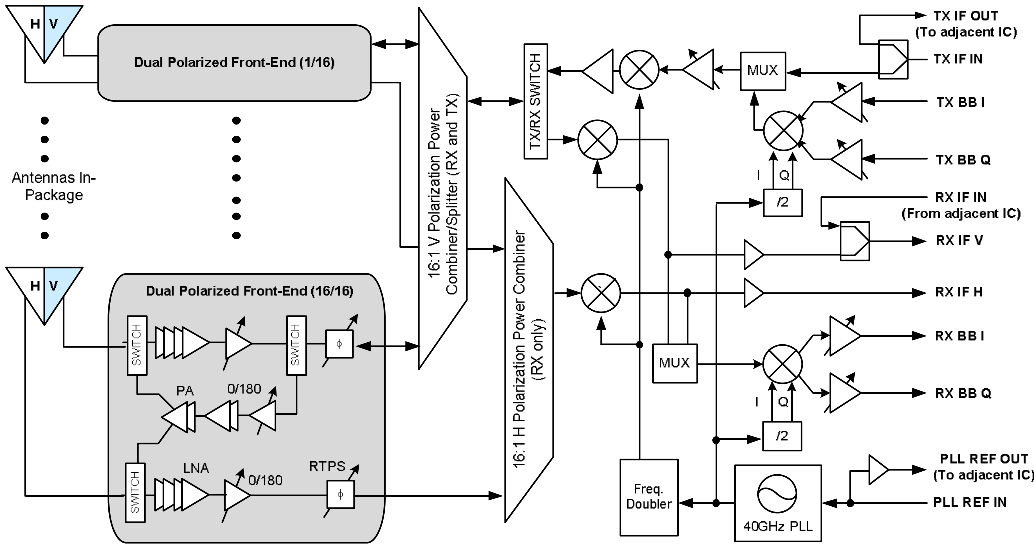

Fig. 1 W-band phased-array transceiver architecture supporting simultaneous reception in both H and V polarizations, and transmission in either polarization.

The TX chain follows the same double-conversion superheterodyne architecture, and the TX shares LO generation and one of the passive combiner trees with the receiver. Two copies of the final PA cascode transistor are included in each of the 16 RF phase-shifting TX front ends in order to drive both polarization feed lines. Only one of these devices is active at any given time, depending on the desired polarization. The phase-shifting RF front ends in both transmitter and receiver feature local memory arrays to facilitate both beamsteering operations and calibration within the overall array.

Each 94-GHz power combining and distribution network has four levels with a total of 15 passive power combiners. The full design thus includes 30 power combiners, as well as transmission lines for signal distribution, that all need to fit in the four columns between the RF front-ends and in the horizontal row along the center of the IC (see Fig. 3).

A transceiver RF front-end in which a single antenna port is shared between the PA output and the LNA input requires a switching mechanism between RX and TX modes. The use of a traditional transmit/receive (T/R) switch would have a significant impact on performance since the insertion loss directly degrades the RX NF. In this work, an alternative solution is proposed which minimizes the impact on NF.

Fig. 2 presents a simplified schematic of the switch as implemented. In TX mode, both the LNA and the switch device are OFF. The PA output network is designed to maximize the power delivered to the antenna in this configuration. In RX mode, the switch device is activated and thus the TX path as seen from the LNA (Z_{PA}) presents high impedance.

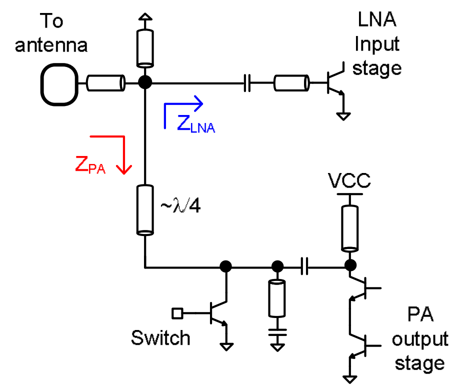

Fig. 2. Conceptual circuit schematic for the switch implementation

The LNA input matching is designed to attain the lowest possible NF in the ON state (RX mode) and present the highest possible load impedance to the PA (Z_{LNA}) in the OFF state.

III. Measurement Results

The IC (6.7x6.6 mm^2) was fabricated in the IBM 130nm SiGe BiCMOS8HP process with variants having aluminum pads for wafer probing and controlled collapse chip connection (C4) solder bumps for packaging. The transceiver integrates more than 1.5 million FETs and 5100 NPNs. Fig. 3 shows a C4 die photograph annotated to show major IC functional blocks. Several IC variants and sub-circuit breakouts have allowed probe-based testing of the overall IC, as well as individual circuit

blocks, including evaluation at various points along the signal chains.

Fig. 4 shows measured RF front-end NF referred to the IC input, including the effect of the T/R switch; we observe 8.2 dB NF at 94 GHz and 25°C, rising to 9.5 dB at 65°C and 9.9 dB at 85°C. As discussed in section II, the T/R switch is designed to favor the LNA (that is, it has less insertion loss for the LNA than the PA) and causes <0.5 dB of NF degradation compared to stand-alone LNA measurements. Gain of the RF front-end in RX-mode (including the phase shifter, as shown in Fig. 1) is 30 dB at 94 GHz, with 3-dB bandwidth extending from 83-100 GHz. The measured S_{11} is better than -10 dB from 75-110 GHz.

The synthesizer consists of a ~40GHz PLL followed by a frequency doubler [8]. It provides measured LO frequencies from 74-83 GHz to the RF mixers, which supports an operating frequency range of 84-93 GHz for full RF to BB up- and down-conversion, slightly lower than the simulated 86-96 GHz range. For this reason, measurements involving BB inputs/outputs extend only up to 93GHz, while transceiver IF to RF operation and breakouts were measured beyond 94GHz. Synthesizer phase noise, measured at the doubler output, is better than -110 dBc/Hz at 10 MHz offset from the carrier for output frequencies in the range 73.9 to 83.5 GHz [8].

Fig. 5 shows the measured TX chain saturated output power from 88-95GHz. For this measurement, the LO frequency is kept constant while the IF is swept from 8 to 12 GHz. The maximum TX gain (from IF input to each of the RF outputs including the T/R switch), oP1dB, and saturated power at 94 GHz are 23dB, -2dBm, and +2dBm, respectively.

Fig. 6 shows vector-network analyzer (VNA) measurement made on a beamformer breakout, which consists of the 16 dual-polarized RF front-ends and the two power-combining/distribution networks. Single-path gain in TX mode is measured from the input of the 1:16 power splitter to an antenna port in one element. Peak gain of 10 dB at 93 GHz is consistent with an RF front-end gain of 29 dB in TX-mode and a loss of 19 dB in the power distribution network (3 dB power distribution per level, or 12 dB, and 7 dB of passive losses). Single-path RX gain is measured from an antenna port in one element to the output of the 16:1 power combiner.

Fig. 7 shows the measured phase shift and gain of the TX path in an RF front-end as the digital settings for the phase shifter are altered. TX gain is represented by radial the distance and phase shift is represented by the angle; a perfect circle would represent ideal phase shifter performance. Gain varies by less than 1 dB over the 360° circle and phase resolution is better than 11.25°.

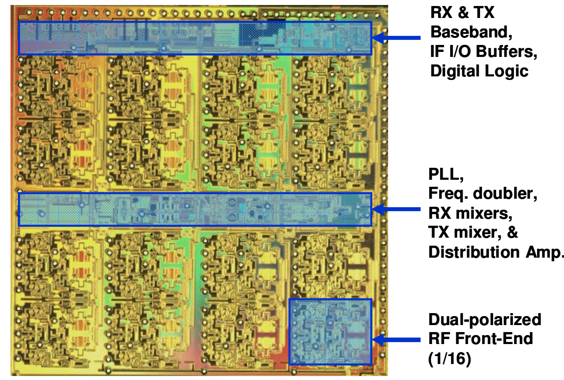

Fig. 3. C4 IC photograph, die area is 6.6X6.7mm^2

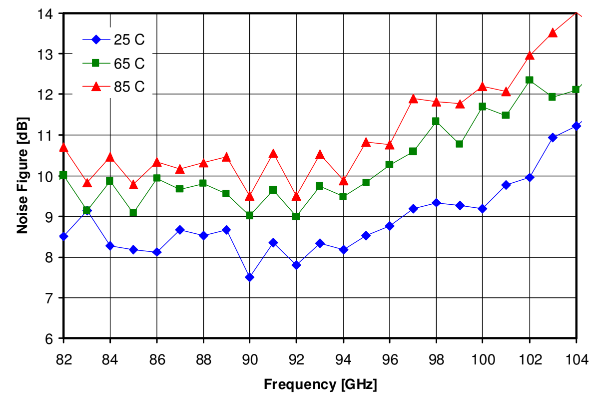

Fig. 4. Measured receiver noise figure

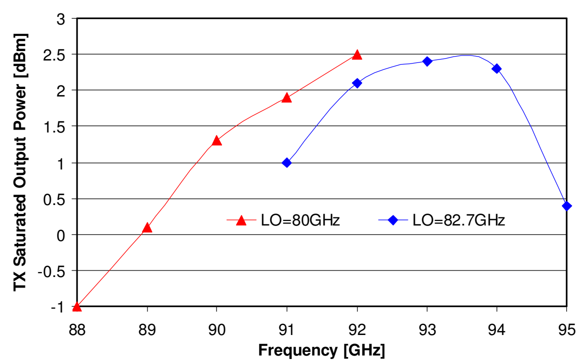

Fig. 5. Measured transmitter saturated output power

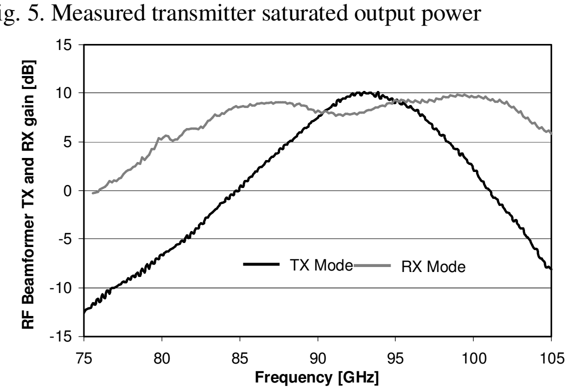

Fig. 6. Measured single-path beamformer gain in TX and RX modes

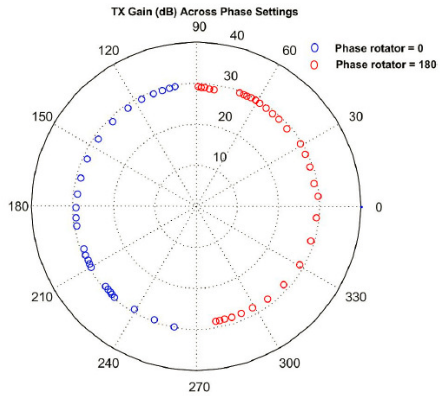

Fig. 7 Measured 94GHz RF front-end TX-path gain and phase across multiple phase shifter settings.

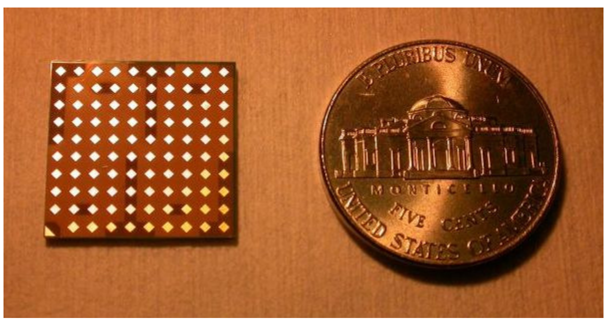

Fig. 8. Fabricated package with 64 antennas to house 4 transceiver ICs

Table I. Performance Summary

RX-mode RF front-end NF (incl. T/R switch)	8.2 dB
RX-mode overall IC maximum gain (16 RF-inputs to BB output at 93 GHz)	43 dB
TX-mode Overall IC Saturated Power Output (per output, including T/R sw.)	>2 dBm
TX-mode Overall IC Maximum Gain (IF-input to RF-output, including input power splitter)	23 dB
Phase Shifter Range	360°
Phase Shifter Resolution	<11.25°
RX-mode power consumption: 32 inputs for simultaneous H & V reception	3.4 W
RX-mode power consumption: 16 inputs for alternate H or V reception	2.2 W
TX-mode power consumption with IF/BB input	2.7/2.9 W
Synthesizer phase noise (for output frequencies from 73.9 to 83.5GHz)	<-110 dBc/Hz @ 10MHz offset
Analog/Digital power supplies	2.7/1.5 V

Data are taken at 94 GHz and 25°C unless otherwise specified.

The C4 version of the IC is designed to be packaged in a 4-IC package containing 64 dual-polarization antennas, as pictured in Fig. 8. The antennas are placed on approximately a λ/2 pitch at 94 GHz in both x and y dimensions and come to within approximately λ/4 of the package edge. By tiling packages adjacent to one another on a PCB, phased arrays of large aperture can be created.

VII. Conclusion

A fully-integrated W-band phased-array transceiver IC supporting dual-polarized antennas has been demonstrated in a mature SiGe BiCMOS process with f_T/f_{MAX} of 210/270 GHz. The achieved NF, output power, phase shift and phase noise performance are suitable to support imaging and communication applications. Important architecture, circuit design, and circuit-package co-design challenges for the implementation of multi-function mmWave phased arrays have been tackled for the first time. To the best of the authors' knowledge, this work presents the highest level of monolithic integration so far achieved in silicon at W-band frequencies.

Acknowledgement

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References

[1] B. Wallace, "Advanced Millimeter-wave Mutlifunction Systems and the Implications for Semiconductor Technology," *IEEE CSICS*, pp. 1-3, October 2011.

[2] K. Sarabandi, and M. Park, "Extraction of Power Line Maps from Millimeter-Wave Polarimetric SAR Images", *IEEE T-AP*, Vol. 48 (12), pp. 1802-1809, December 2000.

[3] L. Schulwitz, A. Mortazawi, "A Compact Dual-Polarized Multibeam Phased-Array Architecture for Millimeter-Wave Radar", *IEEE T-MTT*, Vol. 53 (11), pp. 3588-3594, March 2012.

[4] S. Y. Kim, et al., "A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Build-In-Self-Test System", *IEEE RFIC Symp. Dig*., pp. 127-130, June 2012.

[5] W. Shin, et al., "A 108-112 GHz 4x4 Wafer-Scale Phased Array Transmitter with High Efficiency On-Chip Antennas", *IEEE RFIC Symp. Dig*., pp. 199-203, June 2012.

[6] M. Jahn, et al., "A Four Channel 94-GHz SiGe-Based Digital Beamforming FMCW Radar", *IEEE T-MTT*, Vol. 60, No. 3, pp. 861-869, March 2012.

[7] S. Shahramian, et al., "A 70-100 Direct-Conversion Transmitter and Receiver Phased Array Chipset in 0.18µm SiGe BiCMOS Technology", *IEEE RFIC Symp. Dig*., pp. 123-127, June 2012.

[8] J.-O. Plouchart, et al., "A 73.9-83.5GHz Synthesizer with -111dBc/Hz Phase Noise at 10MHz Offset in a 130nm SiGe BiCMOS Technology", *IEEE RFIC Symp. 2013*, June 2013.