A 60 GHz Wideband Phased-Array LNA With Short-Stub Passive Vector Generator

Ki-Jin Kim, *Member, IEEE*, K. H. Ahn, T. H. Lim, Hyun Chul Park, and Jong-Won Yu, *Member, IEEE*

***Abstract*—This letter presents 60 GHz 5 b phased-array low noise amplifier (LNA) implemented in 90 nm CMOS for a short range wireless application. The design consists of common source two-stage LNA, short-stub vector generator, I/Q modulator with 5 b digital to analog converter and differential to single amplifier. All the proposed amplifiers are designed using a transformer coupled method which results in wideband operation to meet the frequency requirement of the standard. The proposed circuit provides 360 phase controllability over 50–70 GHz band while achieving 12.5 dB gain, 6.55 dB NF and consuming 50 mA from 1.2 V. The measured rms phase error is in the phase accuracy limitation (differential phase array) and gain variation is quite low (< 0.92 dB) over 5 b control range.**

***Index Terms*—Beamforming, I/Q modulator, phase shifter, 60 GHz WPAN, transformer coupled low noise amplifier (LNA).**

I. Introduction

RECENLTLY 60 GHz high speed short range wireless communication for wireless personal area network (WPAN) and wireless high definition (HD) streaming has been released. This new market requires low cost 60 GHz transceiver that has almost 10 m communication range which is hard to achieve especially when a silicon process is adopted.

Fortunately, phased-array transceiver architecture showing a controllability of radiation beam pattern, supplies the required effective isotropic radiation power and spatial coverage even in mm-wave CMOS area [1]. The key component of the phased-array system is the phase shifter that provides low and equal insertion loss and accurate phase controllability over the whole operating frequency.

There are various types of phase shifter: switched delay [2], loaded line [3], and I/Q modulator [1], [4]. Considering low and equal insertion loss and accurate phase shifting across the required band, the I/Q modulator based structure is chosen as a prototype. Fig. 1 shows the proposed block diagram of the 5 b 60 GHz phased-array low noise amplifier (LNA). The design is composed of two stage LNA, passive vector generator, I/Q modulator with 5 b digital to analog converter (DAC), and differential to single (DTS) amplifier. Using transformer coupled differential-to-single ended low noise amplifier and I/Q modulator with short-stub passive vector Generator, the novel phase-array LNA shows average 12.5 dB gain, 6.55 dB noise figure (NF), and accurate 5 b phase characteristics over 53–65 GHz on average.

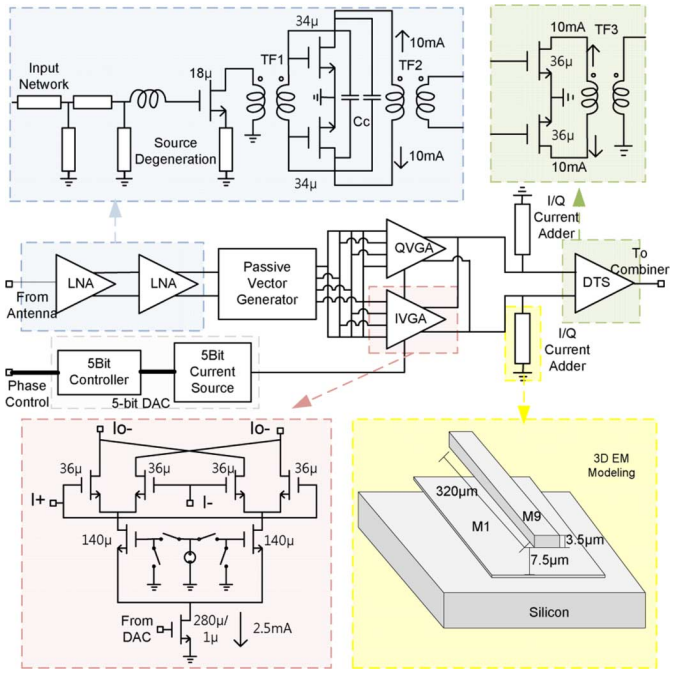

Fig. 1. Block diagram of the proposed phase-array LNA. All devices are designed with minimum channel length except when stated.

II. Proposed Phased-Array Design

A. Transformer Coupled LNA and DTS Amplifier

The proposed 60 GHz DTS LNA is designed based on Common Source (CS) amplifiers (Fig. 1) and all the bias are applied by 1:10 current mirror. The circuits are implemented by 90 nm 9-metal TSMC CMOS technology and biased to have 160 GHz fmax. The CS is used in this letter instead of Cascode because CS shows lower noise figures than Cascode. For the input LNA, simultaneous noise and power matching was achieved by adopting transmission line source degeneration. The input network consisting of shunt transmission lines (100 μm) and series transmission lines (40 μm) is designed for

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K.-J. Kim was with the Korea Electronics Technology Institute, #68, Yatap-dong, Bundang-gu 463–816, Korea. He is now with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea. (e-mail: sergeant@ keti.re.kr).

J.-W. Yu is with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: drjwyu@ee.kaist.ac.kr).

K. H. Ahn, T. H. Lim and H. C. Park are with the Korea Electronics Technology Institute, #68, Yatap-dong, Bundang-gu 463–816, Korea (e-mail: khajoh@ keti.re.kr).

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matching and electrostatic discharge (ESD). All the transmission lines and transformers used in this letter are modeled by full 3-D electromagnetic simulation.

The TF1 (1:2 ratio) transformer is employed to drive differential passive vector generator and to work as a wide band inter-stage matching component. The primary winding serves as a shunt peaking load for the first CS amplifier and the second winding works as a series inductor for the second stage matching.

In the second stage, TF2 (1:1 ratio) transformer load is also used for rejecting common mode signals caused by the first stage amplifier. When the load is tuned for $\omega_o = 1/\sqrt{L_L(C_d + C_L)}$, the peak voltage gain of the second CS LNA is represented as

$$\frac{V_{out}}{V_{in}}(j\omega) = \frac{g_m r_o - j\omega_o r_o C_{gd}}{1 + r_o R_s(\omega_o C_{gd})^2 + j\omega_o R_s[C_{gd} + C_{gd}(1 + g_m r_o)]} \quad (1)$$

where R_s, C_d and C_{gd} are source resistance, effective drain capacitance and overlap capacitance between gate and drain respectively. As shown in (1) the gain is reduced due to the miller capacitor $C_M(= C_{gs}(1 + g_m r_o))$. In the proposed design, the miller compensation capacitor $(C_c = C_{gd})$ is inserted between differential gate and drain nodes to eliminate the undesirable feedback capacitor C_{gd} in the CS amplifier. As explained in [5] adding compensation capacitors not only boosts the gain but also improves linearity. In this letter, the P1dB is improved by 0.5 dB.

The DTS amplifier is located at the end of the proposed building block and transforms a differential signal into a single signal. This block is necessary for the phase shifter to simply drive the following single ended power combining circuit. It also utilizes TF3 (1:1 ratio) transformer for wideband differential-to-single operation.

B. Short-Stub Passive Vector Generator

The vector generator is needed to implement I/Q modulator based phase shifter. There are several major methods to generate a vector signal: reflective-type [6], active vector generator [7], and poly-phase-filter. The reflective-type is difficult to provide reactive termination effectively and has 8 dB loss with 3.5 dB variation. The active vector generator is hard to generate accurate quadature signals, especially, in wideband V-band frequency. The multi-stage poly-phase-filter creates process independent quadrature signal, however it undergoes severe loss especially when used at the receiver front end.

Fig. 2(a) shows the proposed short-sub passive vector generator. It is composed of two-stage poly-phase-filter and 4-resonating short-stubs with 200 μm length for each. When $V_{in}(t)$ is the input and $V_{out}(t)$ $(I_{out}(t) + jQ_{out}(t))$ is the output of the generator, then the transfer function of the generator without short-stub is expressed by

$$H(j\omega) = H_1(j\omega) + jH_2(j\omega)$$
$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{(1 - \omega R_1 C_1)(1 - \omega R_2 C_2)}{D(j\omega)} \quad (2)$$

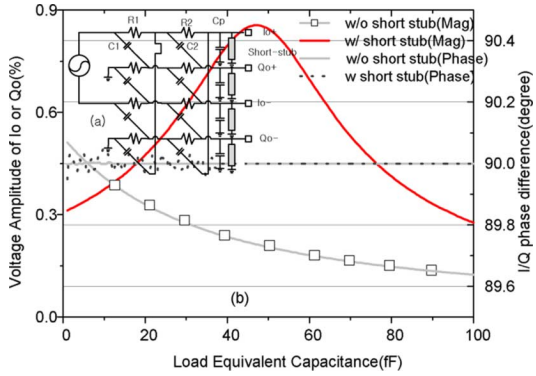

Fig. 2. Proposed short-sub vector generator (a) schematic of the generator (b) simulation characteristics of the proposed circuit.

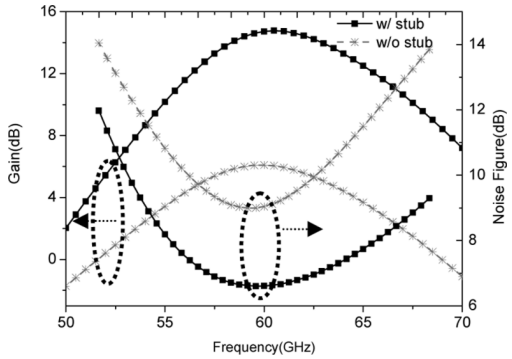

Fig. 3. Simulated Gain and NF of the phase-array LNA comparison between w/ and w/o stub passive vector generator.

where $D(j\omega) = (1 + j\omega[R_1(C_1 + 2C_2 + C_p) + R(C_2 + C_p)] - \omega^2 R_1 R_2[C_1 C_2 + C_1 C_p + C_2 C_p]$ Then the quadrature output of the circuits is

$$I_{out}(j\omega) = H_1(j\omega)V_{in}(j\omega) = \frac{1 + \omega^2(R_1 R_2 C_1 C_2)}{D(j\omega)} V_{in}(j\omega) \quad (3)$$

$$Q_{out}(j\omega) = H_2(j\omega)V_{in}(j\omega) = \frac{j\omega(R_1 C_1 + R_2 C_2)}{D(j\omega)} V_{in}(j\omega) \quad (4)$$

Fig. 2(b) illustrates the sensitivity of the parasitic load capacitance according to (3) and (4). As the load parasitic capacitance (Cp) is increased, the voltage amplitude that is transferred to the next stage (I/Q modulator) is decreased dramatically. This phenomenon deteriorates gain and noise characteristics in the receiver. In this letter, the 200 μm long resonating short-stub loads with the Q value of 24 at 60 GHz are included to cancel the 44 fF load capacitors. As a result, the transferred amplitude becomes four times larger than the case without short-stub and no phase response loss is observed. Because of the previously mentioned enhancement, the proposed vector generator improves the gain and NF significantly. Fig. 3 accounts for the performance enhancement of the proposed design. It shows that the gain in increased by 8 dB and the NF is improved by 2.5 dB.

C. I/Q Modulator

The I/Q modulator is composed of I and Q variable gain amplifier (VGA) controlled by a 5 b DAC and vector adder by cur-

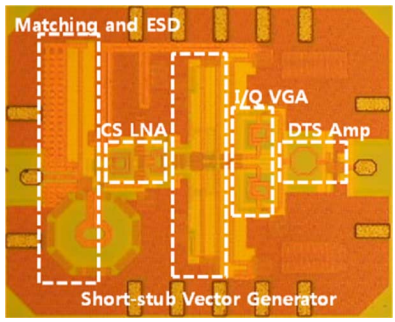

Fig. 4. Chip photograph of the proposed circuit.

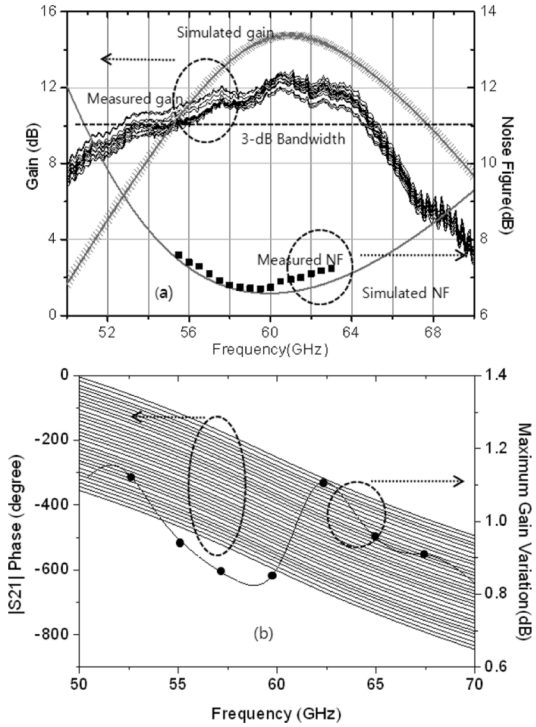

Fig. 5. Measured gain, NF, and phase response.

rent combining short-stub (Fig. 1). The 5 b output of the DAC manipulates the magnitude and polarity of I/Q VGA. The vector adder produces the accurate phase with respect to each output of the VGAs. In this manner, the phase shifter shows excellent performance.

III. Simulation and Measurement Results

The Fig. 4 is the die photograph of the fabricated design. The chip size, including the pads, is 730 μm$\times$ 900 μm. The circuit draws a maximum 50 mA dc current from a 1.2 V supply. The proposed circuit was measured using RF probes. The simulated and measured S-parameters of the designed circuit are compared in Fig. 5. It shows that the difference of the peak gain is only 2 dB and the center frequency is almost same. That is, the 3-D modeled transmission lines and transformers are reasonably evaluated. The measured average gain of 32 phases controlled by 5 b DAC is 12.5 dB with 3 dB bandwidth of 53–65 GHz. The gain variation is less than 1 dB ($< 0.92\,\mathrm{dB}$) over 32 states. This feature is quite important to ensure the efficiency in the phase-array system because the gain imbalance between each channel of the system degrades the array gain. The measured

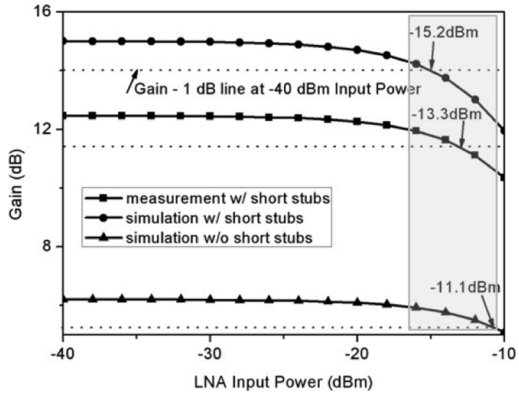

Fig. 6. Comparison of the gain versus input power.

NF is 6.55 dB and quite well matched with the simulation result. Fig. 6. shows the comparison of the gain versus input power. The measured $-13.3\,\mathrm{dBm}$ P1dB is the enough linearity for the 60 GHz arrayed front-end. The relative phase shift can be measured by the phase difference of each transmission coefficient (S21). The 5 b phase accuracy covers more than 50–70 GHz range. To investigate digitally controlled n-bit phase response more qualitatively, differential phase accuracy (DPA) is

$$DPA_i(\mathrm{degree}) = P_{r,i+1} - P_{r,i} - \phi_{\mathrm{nbit}} \tag{5}$$

where $P_{r,i}$ is the real circuit phase with ith code, and Φ_{nbit} is the n-bit quantization phase (11.25°). The S-parameters show the 5.1° maximum DPA which confirms 5 b rms phase accuracy $(\max(\mathrm{DPA}) < 5.625°)$ of the proposed phase shifter.

IV. Conclusion

A wide bandwidth LNA with 5 b digitally controlled phase shifter was implemented in 90 nm CMOS process. The CS LNA with inter-stage matching transformer worked well in V band frequency. The short-stub vector generator significantly improved the gain and NF. The proposed circuit showed outstanding gain and phase characteristics. Thus the presented design can be a good candidate for 60 GHz high speed wireless communication.

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