A Two-Channel Ku-Band BiCMOS Digital Beam-Forming Receiver for Polarization-Agile Phased-Array Applications

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***Abstract* — A 15 GHz two-channel receiver is presented for digital beam-forming applications. The receiver is based on a dual-down-conversion architecture for interference mitigation and results in a channel gain (I and Q paths) of 47.1 dB centered at 15 GHz, with an instantaneous bandwidth of 170 MHz. A 2-bit gain control (0-16 dB) is also provided at the IF stage. The measured NF is 3.1 dB and is independent of the gain state. The measured OP1dB is -11 dBm and the input P1dB is -57 to -41 dBm depending on the gain, and is ideal for satellite applications. The channel-to-channel coupling is < -48 dB. The chip is built using a 0.18-µm SiGe BiCMOS process, has ESD protection diodes on the RF and DC pads, consumes 70 mA per channel from a 3.3 V power supply and is 2.6x2.2 mm^2, including all pads. To our knowledge, this is the first high-performance Ku-band beam-forming chip in SiGe BiCMOS technology.**

***Index Terms* — Digital beam-forming, phased arrays, satellite receivers, SiGe, Ku-band.**

I. Introduction

Satellite systems operating at the Ku-band and located in different earth orbits are used for communication data links with operating bandwidths of 0.1-50 Mbps depending on the receiving aperture size [1]. These satellites operate either with linear or circular polarization, depending on their frequency and orbit. This system is therefore ideally suited for a digital beam-forming array (Fig. 1). In this architecture, each antenna element is connected to an I/Q down-converter, and the received I/Q signals are digitized and sent to a digital beam-forming (DBF) network. The DBF applies the required amplitude and phase (time delay) weighting to each antenna element to result in number of simultaneous patterns (typically 2-6), each with its own scan angle, side-lobe level and bandwidth [2]-[4]. Furthermore, if the antennas are dual-polarized and two channels are available per antenna element, then each beam can have an independent polarization (linear and circular). The DBF architecture is ideal for satellite systems since the required S/N ratio for low bit-error-rate is 12-14 dB for large apertures. However at the element level, the S/N ratio can be -3 dB or lower, and the number of bits in the A/D converter is limited not by the S/N ratio but by the interference levels. Therefore a narrowband band-pass filter is used at each

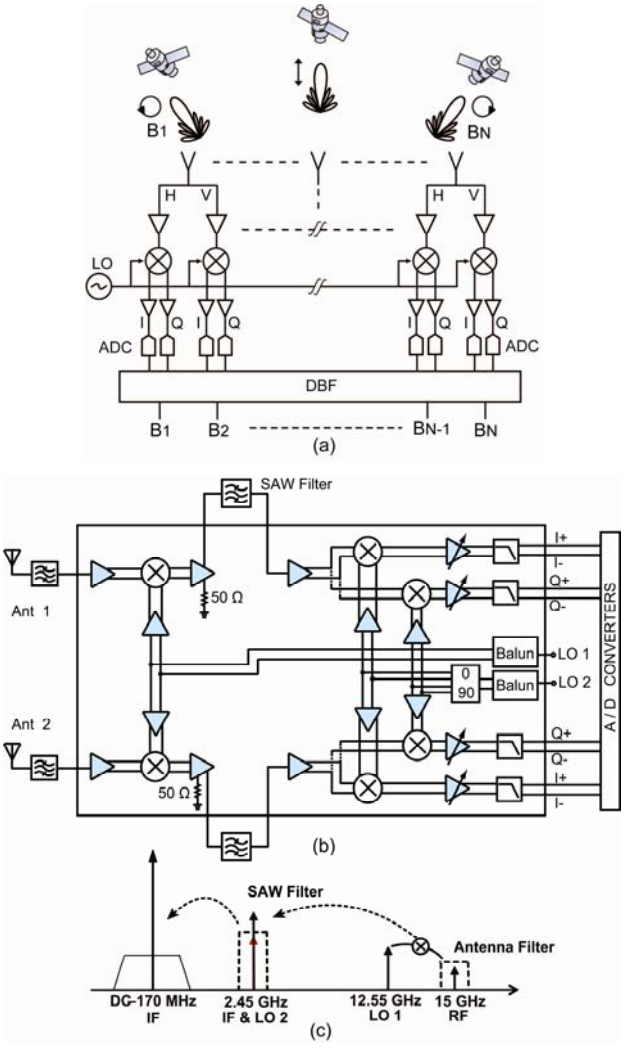

Fig. 1. (a) Digital beam-forming system with polarization agility, (b) two channel down-converter based on a dual-conversion architecture with a common LO feed network, (c) frequency plan.

antenna element, and a dual down-conversion architecture is needed to eliminate any close interferes. Typically such systems require 2-4 bit A/D converters depending on the interference levels (off-the shelf component even for a 200 MSps unit). In most cases, the communication data

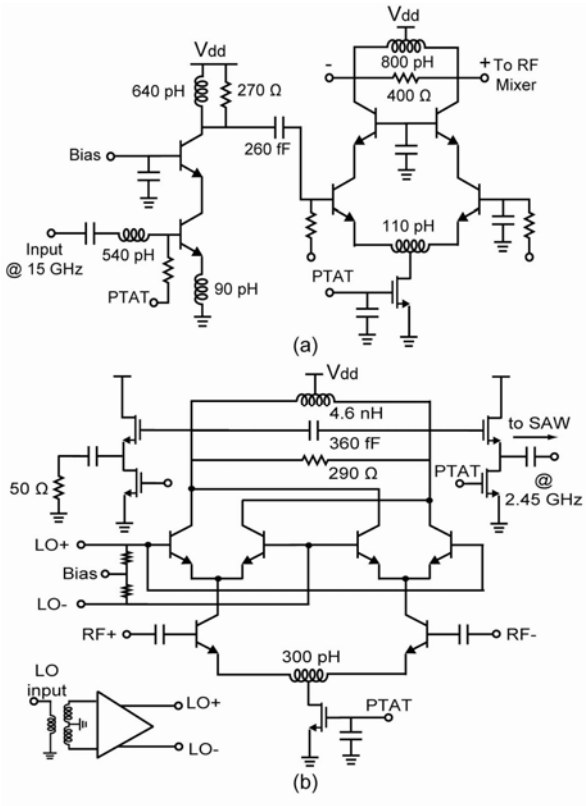

Fig. 2. Schematics for the Ku-band (a) LNA and (b) double-balanced mixer.

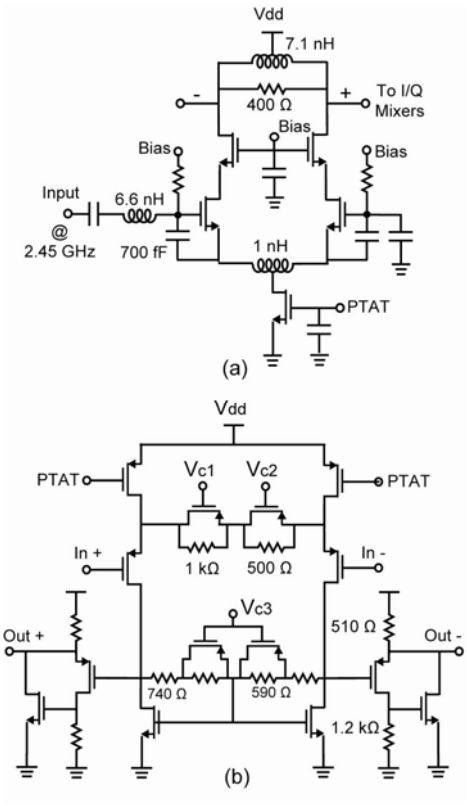

Fig. 3. Schematics for the (a) 2.45 GHz LNA and (b) output VGA.

rate is 0.1-10 Mbps, and a DBF connected to a 16-64 element array can synthesize 2-6 beams using signal processing chips.

The digital beam-former architecture has seen limited use due to the cost and size of GaAs dual-channel Ku-band down-converters. This paper presents the first BiCMOS Ku-band down-conversion chip with two independent channels, each with differential I/Q outputs, and should reduce the cost of DBF systems.

II. Design

Fig. 1 presents the block diagram and frequency plan of the dual down-conversion Ku-band receiver. The 15 GHz input is single ended. A 2.45 GHz off-chip SAW filter with 100-200 MHz bandwidth (depending on the system) is used for IF filtering. The first LO is at 12.55 GHz and the second LO is at 2.45 GHz. Both LOs are external to the chip due to the severe 1/f noise requirements for the satellite communication systems (-120 dBc/Hz at 100 KHz away, typically achieved with DROs [5]). The two channels share common LO busses, and the LO inputs are single-ended and feed directly into passive baluns for differential on-chip distribution. A wideband VGA is placed at the I/Q outputs for linearity control. The chip also contains low-pass RC filtering with a cutoff frequency of 200 MHz at maximum gain. The four A/D

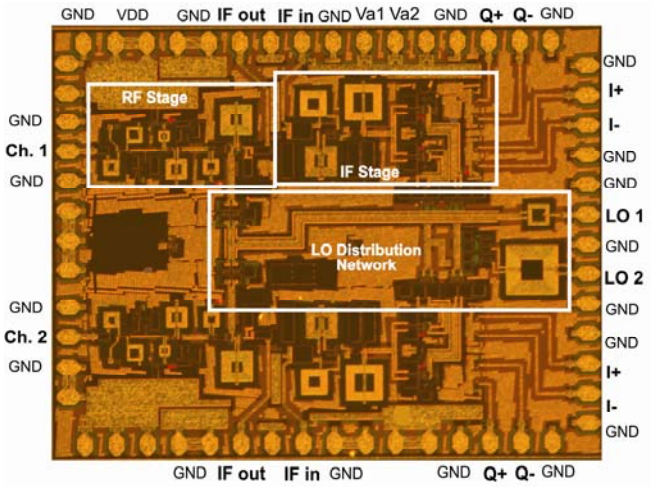

Fig. 4. Micrograph of the Ku-band two-channel down-converter (2.6x2.2 mm^2 including all pads).

converters are off-chip components.

The two-stage LNA/Balun is designed using 0.18 µm SiGe transistors with ft = 150 GHz (Fig. 2a). The first stage is a cascode design with inductive degeneration and a tuned inductive load, and simultaneous noise and input matching is achieved [6]-[7]. The second stage is a single-to-differential converter, also with a tuned load. In order to prevent LO-feed-through and provide common mode suppression, a double-balanced mixer followed by a 0.18 µm CMOS source follower at 2.45 GHz is used (Fig. 2b). One of the mixer outputs is internally loaded with 50 Ω, while the other output is attached to an external SAW filter using GSG pads. The CMOS follower is preferred due to the linearity considerations since the LNA/balun/mixer has a simulated gain and NF of 25 dB and 3.0 dB, respectively, at 15 GHz.

A CMOS active balun is used as the first stage in the 2.45 GHz IF circuit, followed by I/Q double-balanced mixers (Fig. 3a). The 2.45 GHz mixer employ 0.18 µm SiGe transistors in the LO paths for reduced 1/f noise and have resistive loads for wideband operation. An RC polyphase filter with driving amplifiers is used in the 2.45 GHz LO switching core for the dual channel I/Q mixers. The mixers are followed by DC-coupled differential common source pMOS VGAs for reduced 1/f noise, and the gain is controlled by resistive degeneration using Vc1, Vc2 and Vc3 (Fig. 3b). The pMOS stage is optimized for lowest 1/f noise performance, gain and bandwidth. The baseband output impedance is 100 Ω differential to be compatible with high-speed A/D converters. The simulated gain and NF of the IF stage is 25.5 dB and 7.2 dB, respectively, with a 3-dB bandwidth of 200 MHz. The NF increases to 20 dB at 10 kHz due to the 1/f noise from the mixer switching core and pMOS amplifiers.

The chip is fabricated using the 0.18 µm SiGe BiCMOS Jazz SBC18Hx process with 6 metal layers. The inductors, transmission lines, and input/output pads are located on the 2.8 µm-thick top metal layer, and metal levels 4 and 1 are used for ground planes. Full EM modeling (Sonnet [8]) is done on all inductors, the passive LO baluns, and the LO distribution network. All RF and DC pads are ESD protected using 1.2 kV and 3.6 kV diodes obtained from the Jazz library [9]. Each channel consumes 70 mA from a 3.3 V power supply including the LO amplifiers. Fig. 4 presents a microphotograph of the dual- channel Ku-band receiver with two independent RF inputs. The LO

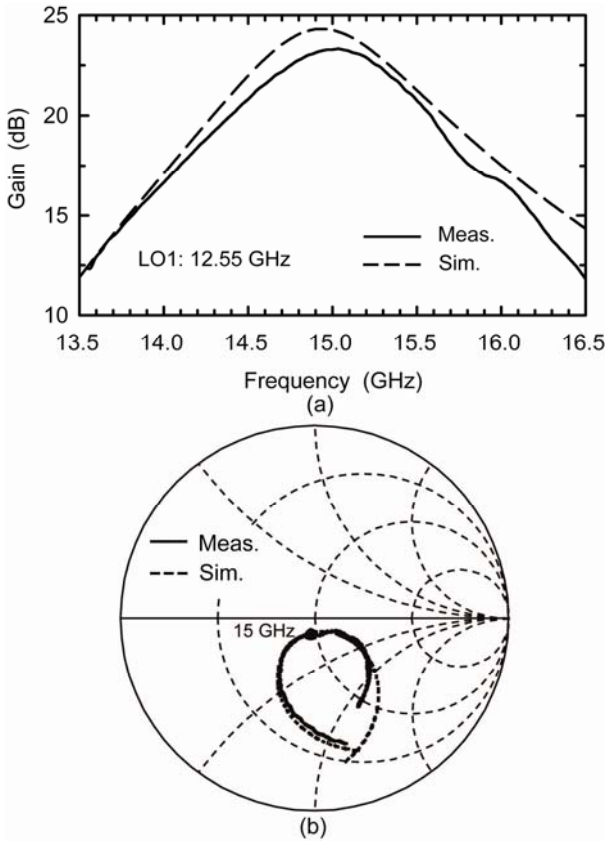

Fig. 5. Measured RF front-end (a) gain and (b) input return loss.

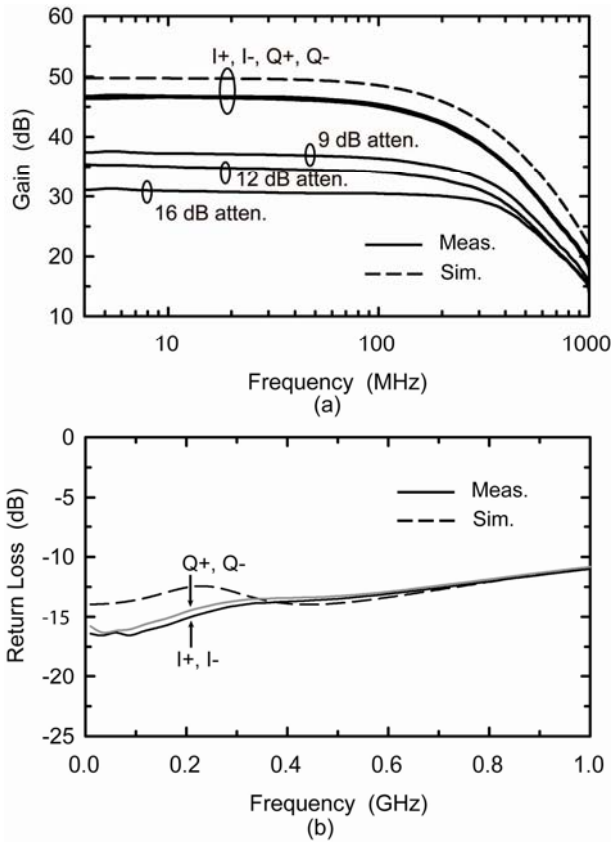

Fig. 6. Measured system (a) gain and (b) output return loss.

distribution network is in the middle part of the chip. The LO power required for proper operation is -6 dBm for both LOs. This ensures that a standard 12.55 GHz DRO with a 20 dBm output power can drive a large number of elements without additional LO distribution amplifiers.

III. Measurements

All measurements are done on-chip using dedicated GSG/GSSG/DC probes and are SOLT calibrated to the probe-tips. The measurements include the RF pads and the ESD diode loading. Measurements were done using Agilent E8361A, E4448A and E8267C PNA, spectrum analyzer and synthesizers.

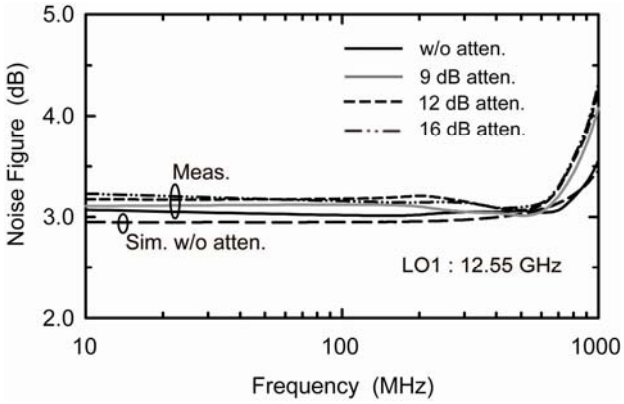

Fig. 7. Measured system NF for different gain states.

A. Single Channel Characterization

The measured RF front-end gain without SAW filter (RF: 13.55-16.55 GHz, LO1:12.55 GHz, IF: 1-4 GHz) and input return loss are shown in Fig. 5 and agree well with simulations. The measured system-level gain (RF: 15-16 GHz, LO1: 12.55 GHz, LO2: 2.45 GHz, IF: DC-1 GHz) shows a maximum gain of 47.1 dB with a 3-dB bandwidth of 170 MHz (Fig. 6a). All four channels, I+, I-, Q+, Q- show identical results with excellent gain and phase match (<1-2° at 10 MHz). The measured output impedance is ~100 Ω differential and is identical for the I and Q channels (Fig. 6b). The gain can be controlled down to 31 dB. The measured noise figure is 3.1-3.2 dB for all gain settings and is constant vs. frequency from 1 MHz to ~ 600 MHz (Fig. 7). The measured OP1dB is -11 dBm and is independent of the gain. This results in a measured input P1dB of -57 dBm to -41 dBm.

B. Dual-Channel Characterization

The two channels are virtually identical to each other and the results are presented above. The spurious coupling measurement on the two-channel array was done by injecting RF power (15 GHz) to channel 1 and measuring the coherent output power at the I/Q ports of channels 1 and 2. A coupling (or leakage) of ~-48 dB was measured in channel 2 compared to the output level of channel 1. This is insignificant and will not distort the synthesized pattern or polarization vector.

III. Conclusion

This paper presented a state-of-the-art SiGe BiCMOS down-converter for polarization-agile DBF phased arrays. A lower system NF can be achieved with a < 1 dB NF GaAs LNA at each antenna port. We are currently assembling these chips on RF boards, and will report on the antenna patterns for an 8-element array.

Acknowledgement

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