A 0.38THz Fully Integrated Transceiver Utilizing Quadrature Push-Push Circuitry

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Abstract

The first fully integrated transceiver operating at 0.38THz has been demonstrated in 0.13μm SiGe BiCMOS with f_T=230GHz. Quadrature push-push circuitry using transformer-coupled stages and Coplanar Strip (CPS) lines are used to realize a terahertz (THz) subharmonic mixer, a quadrature generator, and a quadrupler from a strong fundamental LO quardature signal generated at the W-band. The measured Equivalent Isotropically Radiated Power (EIRP) is -13dBm and the noise figure (NF) is 35dB, while dissipating a power of 364mW.

Introduction

THz spectral range (0.3-3THz) has several applications in imaging and spectroscopy for security and biomedicine, non-destructive testing, and ultra broadband short-range communications [1]. However, it is difficult to realize electronic transceivers in the so-called "terahertz gap" range. Especially in silicon based technology, a fully integrated THz transceiver has not been considered seriously due to the limited device performance and the large propagation losses on a resistive silicon substrate.

One of the critical design issues in a complete on-chip THz transceiver in silicon technology is LO generation and routing, which should be strong enough to drive a down converting mixer for a proper mixing operation. Moreover, routing a THz signal throughout the chip is inappropriate considering the large signal attenuation in the transmission-lines (TL). It is better to generate a strong fundamental signal at millimeter-wave frequency and generate the desired THz signal only before the Tx and Rx antennas in Si(Ge) (Bi)CMOS technology. Therefore, a highly efficient super-harmonic generator with balanced LO inputs is critical in this approach.

0.38THz Transceiver

A. W-band Fundamental LO Generation

Fig. 1 presents the proposed architecture of the FMCW radar transceiver. The W-band balanced signal ({0°, 180°}) is generated with a differential voltage-controlled oscillator (VCO). The Colpitts oscillator architecture is chosen for its wide tuning range and its low phase noise. Furthermore, the cascode topology does not require an additional buffer stage. The branch-line hybrid takes one single VCO output and produces I and Q output signals. The hybrid is made of four Micro-Strip Transmission Line (MSTL) segments and four MIM capacitors to reduce the length of the MSTL. The single-to-differential amplifier amplifies the hybrid outputs to generate the quadrature signal (I:{0°,180°} and Q:{90°, 270°}). The amplifier followed by the hybrid uses the differential cascode topology with an overlay balun at the output-stage to provide the balanced output signal. The balanced gain is 10dB, and P_{sat} is 6dBm.

B. Quadrature Push-Push Circuitry

In order to generate super-harmonics, we use the quadrature push-push technique with two balanced push-push structures made of an emitter coupled pair with collectors in parallel [2] as shown in Fig. 2. The transformer-coupled architecture simplifies impedance matching and dc biasing networks for the push-push structure. CPS lines are used to provide the balanced signals and to provide better signal integrity and higher common mode rejection with a comparable propagation loss compared to CPW and MSTL counterparts [3]. Simulations have been performed with HFSS to find optimal design parameters of the symmetric CPS realized with the metal 6 (M6). The base of the SiGe HBT is biased at a voltage which is slightly higher than the device "threshold" voltage for an optimal 2^{nd} harmonic generation.

C. Receiver

A direct THz LO signal for driving a mixer is not yet available in silicon technology. Instead, we designed a double balanced sub-harmonic mixer which requires a 2^{nd} harmonic quadrature LO signal. From the system perspective, LO to RF isolation is one of the critical issues in a homodyne transceiver, which desensitize the receiver. The sub-harmonic mixer naturally achieves better LO to RF isolation. Throughout the common base devices, both RF+ and RF- input signals from the on-chip patches are fed into two emitter coupled pairs. For RF+, the two push-push structures are driven by 2^{nd} harmonic quadrature LO signals from the quadrature frequency generator. The emitter coupled pairs are driven by the balanced I({0°, 180°}), which generates frequency doubled components with positive polarity which generate IF+. Likewise, the IF- is generated by the pair driven by the Q({90°, 270°}). RF- is mixed with the quadrature LO signal in the same way.

The 2^{nd} harmonic quadrature LO generator consists of two differential frequency doublers and a λ/4 CPS delay line with a loss of 0.3dB (Ansoft HFSS simulation). Each frequency doubler is designed with two push-push pairs combined with a 1:1 overlay transformer for the balanced outputs. The transformer diameter (d=30μm) was chosen to achieve inter-stage impedance matching. A 28fF MIM capacitor is added in parallel with the primary winding of the transformer between the mixer and the generator for the matching purpose. The dc biasing for both blocks are supplied throughout the center-tap of the transformer. The conversion gain of the frequency quadrature block is -11dB, including loss of the input and output transformers, and it provides -5dBm of balanced 2^{nd} harmonic I and Q signals to the mixer LO ports. In simulation, the receiver has -7dB of conversion gain for a differential 100Ω load, allowing for up to 5° of phase mismatch in I and Q paths at the fundamental LO signal. To achieve high radiation efficiency (η_{rad}), on-chip patch antennas are used. The GND plane isolates the signals from the lossy silicon substrate and it prevents surface-wave excitation caused by the high permittivity of the silicon substrate. Each patch is placed in opposite excitation direction for the balanced RF input. The patch has a GND tap at the center for dc current path which suppresses radiation of undesired 8^{th} harmonic generated by the quadrature circuitry in the mixer. Because minimum E-field exists at the center of the patch for the desired 4^{th} harmonic, the effect of the tap is negligible. The antenna has 6.6dBi of gain (G_{ant}) with η_{rad} of 44% at 0.36THz in HFSS simulation.

D. Transmitter

In the transmitter, the 4th harmonic is generated by the quadrature push-push structure. Two overlay transformers (d=45µm) are used to couple the quadrature LO. Tx output power is -13dBm in simulation. The Tx antenna has two patches placed in opposite directions, combined in phase with λ/2 delay line at 4th harmonics, which aligns to the same direction of polarization as the Rx antenna. The λ/2 delay line rejects power combining of the residual 1st and 2nd harmonics. The antenna has 6.3dBi of gain with η_{rad} of 46% at 0.36THz in HFSS simulation.

E. Implementation

For post-layout verification, all inductors, transformers, CPS, and matching networks were simulated (including vias) with full-wave EM simulation (HFSS), and the foundry RF device models were used for intrinsic active devices. The transmitter is realized in a 0.13µm SiGe BiCMOS with process f_T=230GHz. The chip occupies 2.2×1.9mm^2 including the Rx and Tx on-chip antennas (Fig. 3). The chip was assembled chip-on-board (COB) to provide an appropriate antenna environment by avoiding dc probes.

Measurements

From the stand alone VCO, the VCO has the phase noise of -124.5dBc/Hz at 10MHz offset, 8.3% tuning range, and 3dBm (single-ended) output power with f_0=92.7GHz. The VCO in the transceiver was characterized using a W-band horn antenna, a down-converter, and a spectrum analyzer (Agilent E4402B). VCO sweep bandwidth (B_{VCO}) is about 3.65GHz. The transmitting frequency ranges from 0.367THz to 0.382THz. Using the Erickson calorimeter (PM-1B), WR2.2 horn antenna, and WR2.2 to WR10 transition, the measured EIRP is -13dBm. The output power is mainly degraded by the fundamental frequency shift in VCO. The NF is about 35dB from the receiver gain (-7dB) and IF noise floor when the antennas are covered by EM absorbers. We verify the functionality of the entire system from the IF beat signals for a given target. For the target 10cm away from the FMCW radar transceiver, the measured beat frequency is 210kHz when the modulation frequency (f_m) is 10kHz as shown in Fig. 4(b). The estimated beat frequency is 195kHz with BW (=4B_{VCO}) equal to 14.6GHz in the transmitting THz signal. The small discrepancy is mainly due to the VCO sweep non-linearity, which smears the beat spectrum. The IF output shows the strong IF interference around dc due to the Tx leakage which has relatively short propagation delay.

Conclusion

We demonstrated the first fully integrated THz transceiver operating at 0.38 THz with highest reported EIRP (-13dBm) and lowest NF (35dB) in silicon technology.

Acknowledgement

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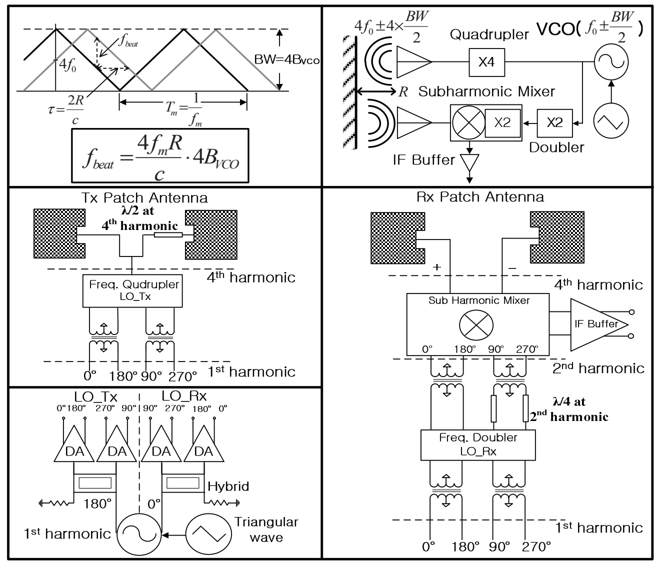


Fig. 1. FMCW radar and the proposed transceiver block diagram.

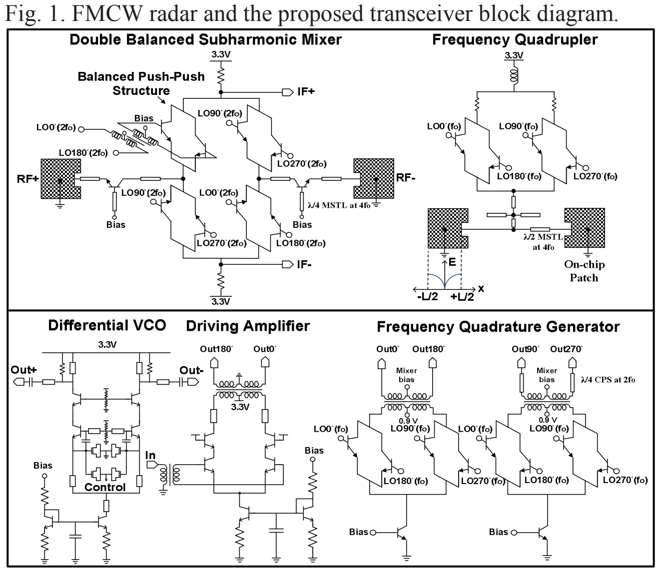


Fig. 2. The Rx and Tx super-harmonic generation circuits (top) and the LO signal generation circuits (bottom).

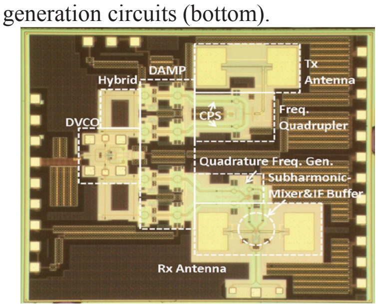
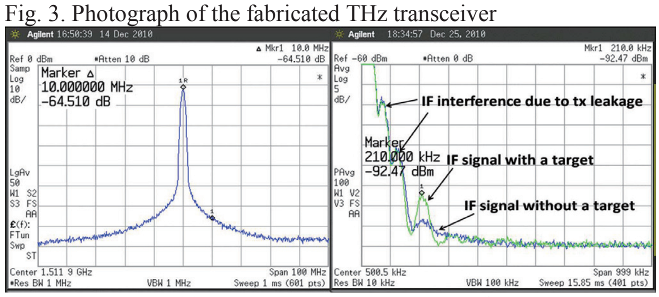


Fig. 3. Photograph of the fabricated THz transceiver



(a) (b)

Fig. 4. (a) Measured down-converted VCO output (f_o=92.7GHz), (b) Measured IF output with and without a target 10cm away from the FMCW radar transceiver (signal averaged 100 times).