A Subharmonic Receiver in SiGe Technology for 122 GHz Sensor Applications

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***Abstract*—The iterative design of an integrated subharmonic receiver for 120–127 GHz is presented. The receiver consists of a single-ended low-noise amplifier (LNA), a push-push voltage-controlled oscillator (VCO) with 1/32 divider, a polyphase filter, and a subharmonic mixer. The receiver is fabricated in SiGe:C BiCMOS technology with $f_T/f_{\max}$ of 255 GHz/315 GHz. In the first design the differential down-conversion gain of the receiver is 25 dB at 127 GHz, and the corresponding noise figure (NF) is 11 dB. The 3 dB bandwidth reaches from 125 GHz to 129 GHz. The input 1 dB compression point is at −40 dBm. The receiver draws 139 mA from a supply voltage of 3.3 V. A subsequent design demonstrates 31 dB differential gain at 122 GHz, and 11 dB NF. The 3 dB bandwidth is from 121 GHz to 124 GHz. The receiver has a NF of 8 dB for 3 GHz IF frequency due to integrated RF bandpass-filtering. It is realized by the lower NF of the LNA, and the LNA itself.**

***Index Terms*—Low-noise amplifier (LNA), millimeter-wave circuits, SiGe technology, subharmonic mixer, voltage-controlled oscillator (VCO), 122 GHz.**

I. Introduction

SILICON technology has made progress towards ever higher device cut-off frequencies, enabling the development of circuits in SiGe or even in CMOS for mm-wave applications beyond 100 GHz [1], [2]. SiGe BiCMOS technologies have become very attractive, as they allow high integration, low cost and combination with digital CMOS control circuits. Recently, SiGe technologies have been demonstrated with frequency $f_{\max}$ of 330 GHz [3] and 400 GHz [4]. The European project DOTFIVE develops novel process modules to push SiGe BiCMOS towards 500 GHz $f_{\max}$ [5]. This allows us to deploy SiGe BiCMOS technology for circuits operating in the 120 GHz frequency range and above. 120 GHz key circuits have been developed and demonstrated [6], [7]. A 165 GHz transceiver frontend was published demonstrating a downconversion gain of −3 dB [8]. A 140 GHz transceiver in 130 nm SiGe BiCMOS was reported [9], which consists of a 140 GHz push-push voltage-controlled oscillator (VCO) with a static divide-by-64 chain, a 140 GHz amplitude modulator, a 140 GHz local oscillator (LO) amplifier, a fundamental frequency mixer, a 140 GHz low-noise amplifier (LNA), and a variable gain IF amplifier. It has a downconversion gain of 30 dB, a noise figure of 12 dB, an output power of −8 dBm, and dissipates 1.5 W. Recently, a SiGe quadrature transmitter and receiver chipset for applications at 160 GHz was presented, which was implemented in SiGe BiCMOS with $f_{\max}$ of 380 GHz [29]. This chipset uses a direct up-/down-conversion architecture, where fundamental I/Q mixers are operated by tripling a VCO frequency for operation at about 160 GHz. The receiver has a downconversion gain of 25 dB, a noise figure (NF) of 14 dB, and it dissipates 1.5 W.

Low-cost SiGe transceivers in the 122 GHz range will be utilized for sensor and imaging applications, as well as for communication. An ISM frequency band at 122.5 GHz with 1 GHz bandwidth is available in Europe and US, which will be mainly used for industrial, scientific, and medical applications, including low-cost radar systems for consumer applications, imaging radar for security applications and bio-medical sensors for medical diagnostics. Furthermore, a 120 GHz-band wireless link for 10 Gbits/s error-free data transmission using InP integrated circuits has been reported [10]. This 120 GHz wireless link operated at a center frequency of 125 GHz and an occupied bandwidth of 116.5–133.5 GHz.

Implementing front-ends for applications in the 122 GHz range in SiGe BiCMOS requires an innovative architecture to fulfill all requirements concerning performance, low power dissipation, and low cost. For low cost the required chip area has to be minimized, imposing restrictions mainly on on-chip passive structures. The usage of inductors and transformers at mm-wave frequencies gives advantage to reduce the chip area far beyond what has been accomplished with transmission lines, distributed baluns and power splitters, as demonstrated in [8]. Furthermore, 90-degree transmission line hybrids, used to generate 90-degree phase shift, can be replaced by more compact *RC* polyphase filters.

For the transceiver architecture, advantage can be obtained by applying frequency doubling techniques, as push-push oscillators, and frequency doublers, to improve the performance and to reduce the power dissipation. Further, implementing a subharmonic mixer (SHM), which uses a sort of frequency doubler technique, is attractive in terms of system budget and local oscillator (LO) rejection [11]. In the case of direct down-conversion the DC-offsets due to LO self-mixing can be significantly reduced compared to a topology with fundamental mixing. The subharmonic receiver topology has also the advantage that the LO generation is performed at half of the RF frequency, which

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results in lower power dissipation. An antiparallel diode pair (APDP) can be used to implement a passive SHM with conversion loss, where the APDP is created by Schottky-diodes [12] or diode-connected SiGe heterojunction bipolar transistors (HBTs) [13]. Another SHM principle, which is similar to a resistive mixer, is based on transconductance mixing, in which the time-varying transconductance of a HBT is the dominant contributor to frequency conversion [14]. Here, both RF and LO signals are applied to the HBT base together through a combiner which is usually a filter or a directional coupler, which however requires relatively large chip area. A SiGe 77 GHz subharmonic balanced mixer has been reported [14], which is based on transconductance mixing. This SHM was implemented in a SiGe technology with 80 GHz transit frequency (f_T).

An active SHM topology, described for 5 GHz applications [15], was used for a 122 GHz SHM in SiGe [16], where integrated hybrid-couplers form the phases in quadrature (I, Q) of the local oscillator (LO) signal. For I- and Q-generation, a more compact integrated polyphase filter was employed in a 94 GHz subharmonic receiver with an external LO source [17].

We have demonstrated a subharmonic receiver in SiGe with an integrated polyphase filter and LO, which reaches 25 dB maximum differential conversion gain at 127 GHz without IF amplifier, a measured noise figure of 11 dB at 127 GHz, and a power dissipation of 460 mW [18].

Heterodyne receivers are often used for communication to get the required performance. A problem in this case is the suppression of spectral components at the image frequency. Bandpass filters can be used to reduce the noise at the image frequency, and thereby decrease the noise figure of the receiver. Recently, the implementation of an integrated passive bandpass filter at 77 GHz was presented, where the bandpass filter was realized with spiral inductors and metal–insulator–metal (MIM) capacitors in SiGe technology [19].

We will show in this work that the transformer coupling between the LNA and the subharmonic mixer in our 122 GHz receiver together with parasitic coupling effects can be utilized for such bandpass filtering. As an alternative solution we optimized also the LNA, to obtain RF bandpass filtering characteristics by the LNA itself.

The present work discusses the design of an integrated receiver for the frequency range from 120 GHz to 127 GHz with emphasis to get optimal receiver performance for 122 GHz ISM-band applications by an iterative design. A 122 GHz subharmonic receiver without IF amplifier is presented, which reveals 31 dB differential conversion gain at 122 GHz for direct down-conversion, and a measured 11 dB noise figure. A lower noise figure of 8 dB is even obtained in the case of IF down-conversion to an IF frequency of 3 GHz. The receiver includes LNA, internal 60 GHz push-push oscillator, 1/32 frequency divider, polyphase filter and subharmonic mixer.

In this work we evaluated receiver chips and its subcircuit chips, which were fabricated in three subsequent technology runs, named in the following as run1, run2, and run3. The results for run1 show that the highest conversion gain of the receiver was obtained around 127 GHz. For run2, the frequency range of the receiver was shifted to the target frequency of 122 GHz by redesign of the VCO. The performance of the SiGe:C HBT, used for run1 and run2, was improved for run3, leading to a higher conversion gain at 122 GHz. The receiver of run3 demonstrated a maximum differential gain of 31 dB and measured noise figure of 11 dB at 122 GHz. The measurement results of the runs 1, 2, and 3 are in reasonable agreement with the simulation results obtained by using the corresponding device models, The design kit model was used for the runs 1 and 2, and an adapted HBT model for run3.

In Section II of this paper, we briefly describe the SiGe technology, which was used for the fabrication of the receiver. Section III is dedicated to the circuit design of the subharmonic receiver and its subcircuits. The measurement results are presented in Section IV, followed by discussion in Section V. The paper ends with conclusions in Section VI.

II. Technology

The receiver was designed with the design kit of IHP for its 0.13 μm BiCMOS technology with five metal layers, and with high-speed SiGe:C HBTs featuring a transit frequency (f_T) of 255 GHz and a maximum oscillation frequency $(f_{\max})$ of 315 GHz [20].

We used three subsequent fabrication runs (run1, run2, and run3) of this technology for the fabrication of our receiver. The vertical profile of the SiGe:C HBT, used for the runs 1 and 2, was further optimized for run3.

Run1 and run2 received the standard process flow whereas for run3 a split with modified SiGe base profile is evaluated. For this split we increased the Boron dose leading to a reduction of the pinched base sheet resistance Rsbi of about 33%. Simultaneously the Ge fraction of the SiGe base was enlarged in such a way that the collector current of the transistors remained approximately constant compared to the case with conventional Rsbi. Transistors with an effective emitter area of $(0.17 * 0.84)\ \mu\text{m}^2$ achieved at $\text{VCE} = 1.5$ V on average peak $f_T/f_{\max}$ values of 245 GHz/350 GHz.

Details of the recent technology are described in [3] and [30]. This 0.13 μm BiCMOS features $f_T/f_{\max}/\text{B}_{\text{VCEO}}$ of 240 GHz/330 GHz/1.7 V.

III. Circuit Design

We used the GoldenGate RF integrated circuit simulator to design and optimize the receiver. The subcircuits of the receiver were designed using GoldenGate and ADS from Agilent. The transmission lines and transformers were simulated with a 2.5D planar EM-simulator (Momentum). A transmission line model of ADS (Physical Transmission Line model TLINP) was used for the design simulations by ADS and GoldenGate. For the transformers we applied S-parameter based models.

A. Topology of the Receiver

The topology of the subharmonic receiver is shown in Fig. 1. This receiver consists of a 122 GHz LNA, a subharmonic mixer (SHM), a 60 GHz push-push VCO for the generation of the internal LO signal, a 60 GHz LO buffer to drive the polyphase filter and a 1/32 frequency divider (FD) for frequency division of the 30 GHz fundamental frequency output of the VCO. The polyphase filter generates the differential I/Q LO signal for the

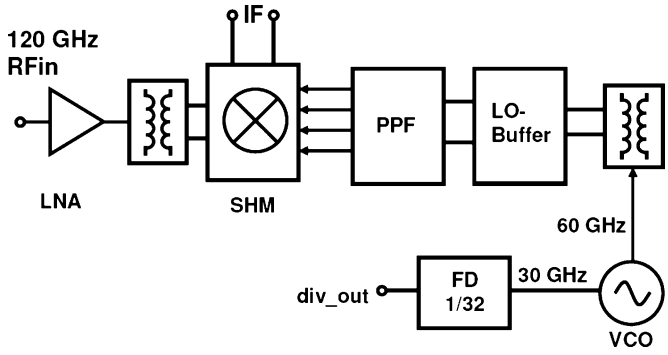

Fig. 1. Topology of the subharmonic receiver.

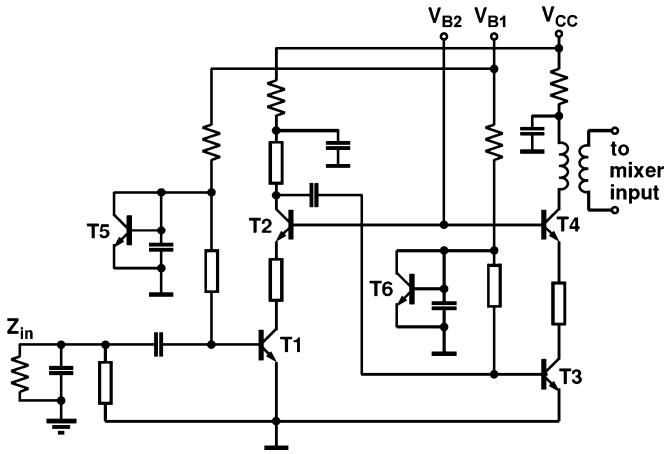

Fig. 2. Schematic of the LNA with transformer coupling at the output.

SHM. The output of the LNA is matched to the SHM by a transformer, and the VCO output is coupled to the 60 GHz LO buffer by a transformer.

The LNA, SHM, and VCO were designed and tested both as separate components with their on-chip transformers with single-ended output, as well as in their fully integrated configuration as receiver. But, for the SHM, the separate SHM chip including polyphase filter was tested with adapted baluns at the RF and LO inputs.

In the following, the details of these subcircuit designs and the complete receiver design are presented.

B. Low-Noise Amplifier

Fig. 2 shows the schematic of the LNA with a transformer coupling at the output as used in the receiver. We used also an LNA with capacitive coupling at the output, as described in [7], as a test structure. The LNA consists of a two-stage cascode with matching networks for input and output matching to 50 Ohm and to the mixer input, respectively [7], [21]. For simplicity, the circuitry for generation of reference voltages $V_{\rm B1}$ and $V_{\rm B2}$ is not included in the schematic. The cascode configuration was chosen for the higher gain per stage in comparison to the common-emitter configuration due to reduction of the Miller effect in the CE-part of the cascode. In addition, the cascode configuration with its stacked transistors is well suited for the intended use of the LNA in RF frontends with 3.0–3.5 V supply voltage. Each stage provides around 7 dB of gain with a biasing of 4.9 mA and 5.4 mA for the first and second stage, respectively, at a supply voltage of 3.5 V. The biasing of the CE transistors T1 and T3 is performed by current mirrors utilizing the transistors T5 and T6 and the transmission lines at the base of these transistors. The transmission lines are ac-shorted at the one side and connected to the base of transistors T1 and T3, respectively, on the other side, thereby transforming the ac-short to an open (or at least high-ohmic state) at the bases. The overall input matching network consists of the parasitic pad capacitance, the transmission line for the connection from pad to the first amplifier stage (not shown in the figure), a transmission line to the ground for ESD protection of the input, a MIM capacitor for dc-decoupling of the input, and the base transmission line. To obtain a high quality factor Q of the input pad capacitor, the pad is shielded from the silicon substrate by a grounded plate in the lowest metal layer. The output of the LNA is transformer coupled to the mixer input. The transformer consists of one loop in the highest metal layer and second highest metal layer for the primary and secondary winding, respectively. This ensures optimal matching to the symmetric input of the mixer.

For the layout design of the LNA, an innovative transmission line structure has been developed providing low-impedance grounding at the whole LNA chip region. In contrast to conventional designs, the top metal 2 is used as the grounding layer with a thickness of 3 μm. The signal line is made of top metal 1 below the grounding layer of top metal 2. The LNA part of the receiver chip microphotograph in Fig. 7 illustrates this design style. The holes in the top metal 2 plate are inevitable for the fabrication of the chip because of mechanical strain in the layers (slit rules).

The S-parameter results of the transmission lines were included in the circuit by means of fitting to the TLINP model. The matching was performed in such a way that a good match to 50 Ohm at the output and minimum noise figure at the input were obtained. For the LNA with capacitive coupling at the output, we obtained the following simulated gain and NF at the target frequency of 122 GHz: 16 dB gain and 8 dB NF for run1, and 22 dB gain and 6.5 dB NF for run3.

C. Subharmonic Mixer

Subharmonic mixing is possible by multiplying the RF signal with the quadrature LO signal at half the RF frequency. We used a subharmonic mixer design described in [16], [17], which is based on two stacked switching quads. This topology has better performance at 122 GHz for conversion gain compared to a topology based on a modified Gilbert cell with parallel transistor stacks [22], as we found by simulations. An active 122 GHz SHM in SiGe, based on stacked switching quads, has been described previously [16], where the supply voltage was at 6.6 V. A cascade of three capacitively loaded branch-line couplers was used to form the I and Q phases of the LO signal, resulting in a relatively large chip area of 0.75 mm^2 without all pads. This SHM includes an IF buffer, consisting of a differential amplifier and an emitter follower, which was added to the IF output of the SHM core, and transformed the differential IF signal to a single-ended signal. The SHM together with the IF amplifier showed a maximum conversion gain of 23 dB for an external 60 GHz LO signal of 3 dBm. For I and Q generation, a more

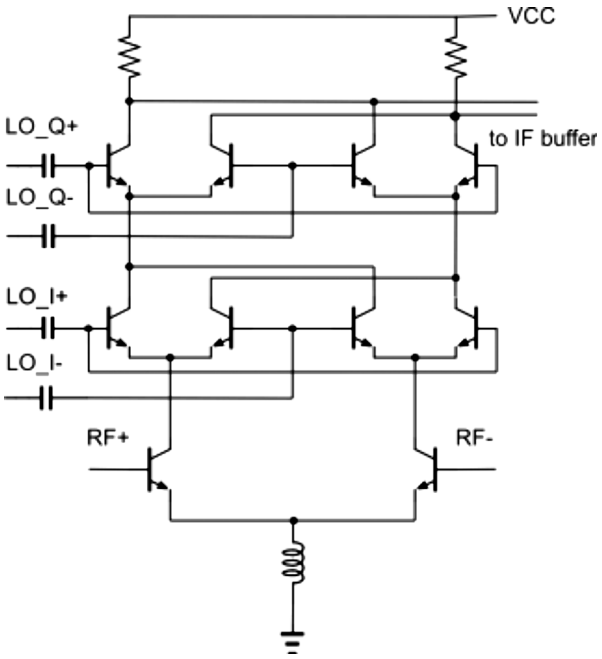

Fig. 3. Schematic of the subharmonic mixer with stacked switching transistors.

compact integrated polyphase filter was employed in a 94 GHz subharmonic receiver with stacked switching quads, which were driven with an external LO source [17]. A supply voltage of 3.3 V was used. This receiver, consisting of LNA and SHM, yields 20 dB conversion gain at 94 GHz RF for 2 GHz IF, with an input 1 dB compression point of -31 dBm and an estimated NF of 15 dB. Here, the LNA gain at 94 GHz was 15 dB, and the estimated LO power at the input of the polyphase filter was 0 dBm.

In this work, a modified SHM was used. Its schematic is shown in Fig. 3 without biasing circuitry. In contrast to [17], we applied a capacitive coupling between the polyphase filter and the SHM, as we connected the LO signal to the polyphase filter in a different way; see Fig. 4. In [17] the signal Lop was only connected to the node 1 and the opposite signal Lon to the node 3. To save headroom, the tail current source in [16] is replaced by an inductor, as proposed in [17], with $L = 50$ pH. The differential IF output was generated by emitter followers connected to the 200 Ohm load resistors of the mixer core. The bias at the base of the RF input transistors allowed to tune the operation point of the SHM. The optimal tail current through the mixer core was 8 mA.

D. Polyphase Filter

The *RC* polyphase filter is attractive for quadrature signal generation in RF circuits due to its small size. To minimize amplitude and phase mismatch, a complete symmetrical layout was proposed for a 5 GHz polyphase filter [23]. Recently, a two-stage polyphase filter for 60 GHz has been reported [24], with the design parameters $R_1 = 120\ \Omega$, $R_2 = 130\ \Omega$, and $C_{1,2} = 20$ fF.

In this work, we implemented only a one-stage *RC* polyphase filter with $R = 67\ \Omega$ and $C = 40$ fF for the quadrature LO signal generation to achieve lower loss of the polyphase filter.

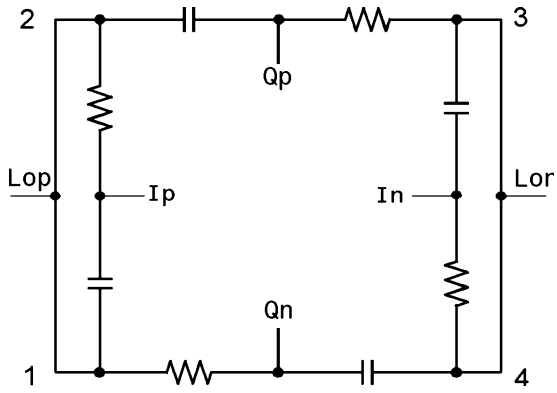

Fig. 4. Schematic of the polyphase filter.

The schematic of the *RC* polyphase filter is shown in Fig. 4. The layout of our polyphase filter is a cross-like structure with a complete symmetrical topology to avoid I/Q mismatch. Here, we utilized unsalicided, p-doped gate polysilicon as resistor material, because these resistors exhibit very small temperature coefficients. Thus, the resonance frequency of the polyphase filter does not change significantly at higher LO power due to increased temperature. The capacitors are implemented as MIM capacitors with 1 fF/μm^2.

E. Voltage-Controlled Oscillator

The oscillator has to provide a 60 GHz differential signal to the polyphase filter with a power level of 5 dBm at minimum. To fulfill all the requirements in terms of tuning range, power, and reliability, a push-push oscillator topology is preferred [25]–[27], which was chosen here also. Push-push oscillators offer several advantages. Because the fundamental tone is not damped by the oscillator's load impedance the loaded Q-factor is equal to the unloaded Q-factor. This will improve the phase noise in comparison to a fundamental oscillator at the same frequency. The tuning range is increased because of the halved oscillation frequency and the temperature sensitivity is reduced. Compared to a solution with an oscillator at half the frequency and frequency doubler the push-push oscillator is less area consuming. Additionally, the push-push oscillator is highly resistant to load pulling effects because the suboscillators are terminated by "virtual ground" [26].

With this topology it is possible to provide a signal path with relatively low fundamental frequency f_0 of around 30 GHz to the frequency divider and following phase-locked loop (PLL) circuitry (if required), and to provide the 60 GHz LO signal via the LO buffer to the polyphase filter.

In this work we implemented the oscillator with buffer as depicted in Fig. 5 and Fig. 6. The oscillator core consists of two sub-oscillators in common-collector topology. In the Vcc supply line a transformer is placed transferring the first harmonic at 60 GHz via buffer to the subharmonic mixer. The fundamental tone at a frequency of 30 GHz is coupled to the 1/32 frequency divider via a second transformer. Because of the voltage divider established by the inductors in series with the second transformer, the loading of the fundamental frequency tone is weak. Only a small fraction of the fundamental power

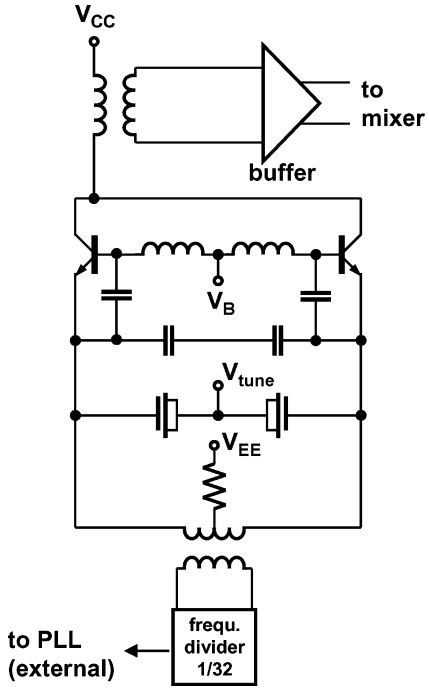

Fig. 5. Schematic of the 60 GHz push-push VCO with LO buffer.

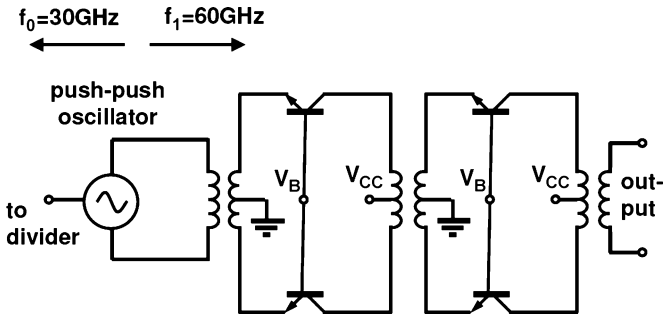

Fig. 6. Schematic of LO buffer after the 60 GHz push-push VCO.

is required for the frequency divider because of the high sensitivity of the divider at 30 GHz. The second harmonic f_1 of the oscillator is transformer coupled to the LO buffer. Thus, we arrive at a symmetrical signal enabling the use of differential circuit principles in the following amplifier stages. Both buffer stages are common-base circuits with the advantage of high gain at 60 GHz and robustness with respect to the supply voltage.

IV. Measurement Results and Discussion

We evaluated the receiver chips of three iterative designs, which were fabricated in three subsequent technology runs, named in the following as run1, run2, and run3.

Fig. 7 shows the microphotograph of the fabricated receiver chip, run1. The layouts of run2 and run3 contain only minor changes compared to this layout. Fillers were generated in all metal layers to achieve best correspondence to the used design kit models. The die area without outer pads is $900\ \mu\text{m} \times 620\ \mu\text{m}$. Note that the chip area is not minimized yet.

The results for run1 reveals that the highest conversion gain and the lowest noise figure of the receiver were obtained around 127 GHz. For run2, the frequency range of the receiver was

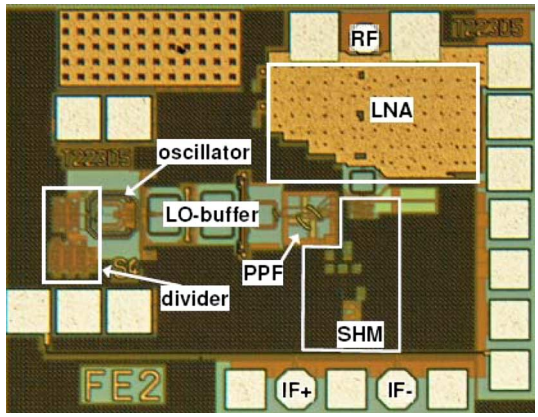

Fig. 7. Receiver chip microphotograph.

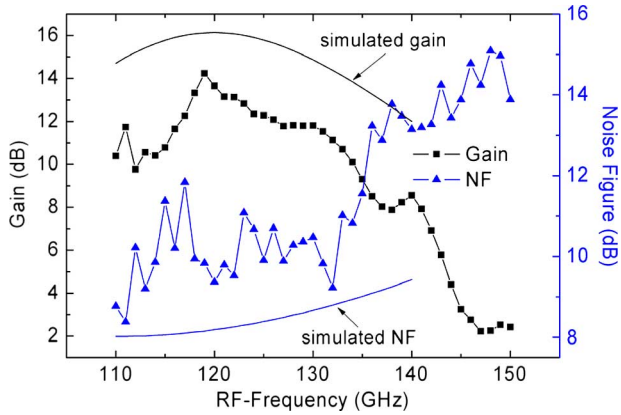

Fig. 8. Gain and noise figure of the LNA with capacitive coupling at the output, run1.

shifted to frequencies around 122 GHz by a redesign of the VCO. For run3 the performance of the SiGe:C HBTs was further improved and the operation points of the subcircuits were optimized, which mainly leads to a higher conversion gain of the receiver.

The measurements of the receiver chips in the 120 GHz range were performed at IAF, Freiburg, Germany [28]. Here, for the noise measurements the hot/cold method was applied using a calibrated noise source.

A. Low-Noise Amplifier

In the following, the measured gain and noise figure of the LNA are presented together with the simulated values, which were obtained by S-parameter simulations.

For run1, Fig. 8 shows the simulated and measured gain and noise figure of the LNA with a capacitive coupling at the output. The maximum gain is 14 dB at 119 GHz and the corresponding noise figure is about 9 dB.

The LNA was also characterized together with the transformer, which realizes the coupling between the LNA output and the SHM input. For run1, the measured gain is 10 dB in the frequency range from 118 GHz to 132 GHz, and the noise figure is about 10 dB, as illustrated in Fig. 9. For run3, the Fig. 10 presents the gain and the noise figure of the LNA with capacitive coupling as function of the frequency. The measured gain reveals a pronounced maximum around 122 GHz with

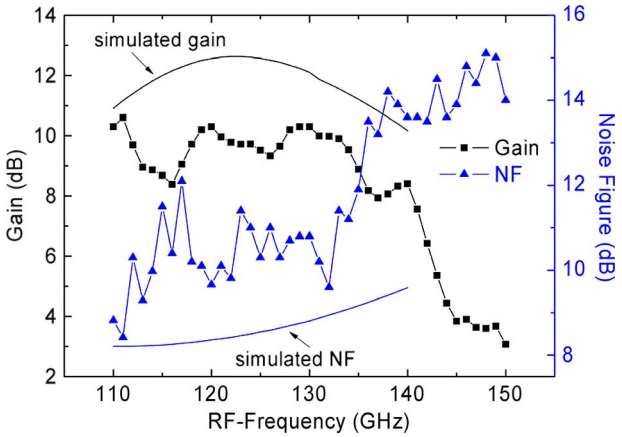

Fig. 9. Gain and noise figure of the LNA with transformer coupling at the output, run1.

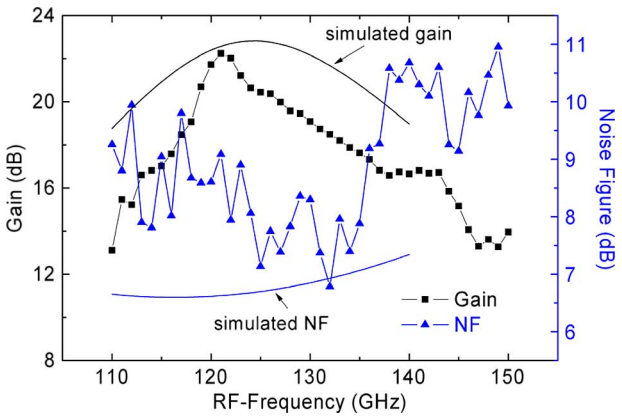

Fig. 10. Gain and noise figure of the LNA with capacitive coupling at the output, run3.

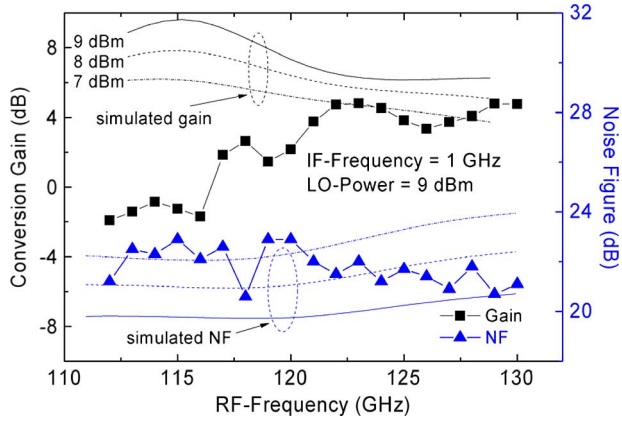

Fig. 11. Conversion gain and noise figure of the SHM, run1.

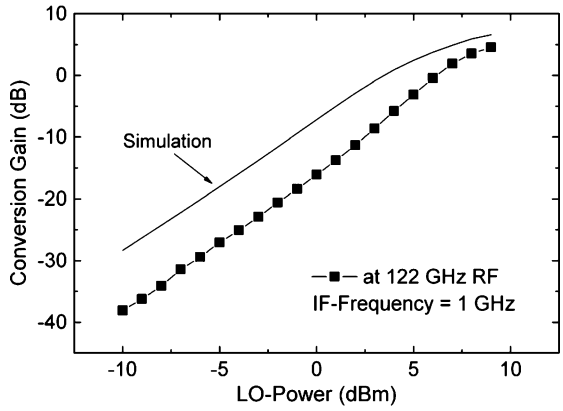

Fig. 12. Conversion gain of SHM versus LO power, run1.

gain of 22 dB, and the noise figure is about 8 dB in the range 120–135 GHz.

The simulated gain and noise figure at the target frequency of 120 GHz are close to the measured values of gain and NF for run1 and run3, respectively, indicating that the used HBT models yield good accuracy for the HBT parameters. However, the pronounced maximum of the gain around 120 GHz is not revealed by the simulation.

We assume that this increased gain is due to parasitic coupling which is not taken into account in our simulation.

B. Subharmonic Mixer

We measured the single-ended IF output signal of the SHM, whereby we used integrated baluns for the RF input and the LO input, which are optimized for the SHM chip. Fig. 11 presents the conversion gain as function of the RF frequency with the LO power on wafer at 9 dBm, whereby the IF frequency is set to 1 GHz. The maximum conversion gain at 122 GHz is achieved at about 5 dB with additionally +3 dB taking into account the differential output, and the noise figure of the SHM is about 21 dB. The conversion gain and the NF of the SHM were simulated with the LO power as parameter using small signal noise analysis (SSNA) of GoldenGate. The simulated gain and NF are plotted in Fig. 11 for LO powers 7 dBm, 8 dBm, and 9 dBm. Seven dBm of LO power gives a reasonable fit in the frequency range from 120 GHz to 130 GHz.

Fig. 12 shows the measured and simulated conversion gain of the SHM as a function of the LO power at the pad of the chip. The simulation was performed using Harmonic Balance. The measured conversion gain reaches saturation at 9 dBm LO power. The comparison of the measured and simulate values suggests that for the measured conversion the actual LO power at the pad is about 2–3 dB lower than given in Fig. 12.

C. Voltage-Controlled Oscillator

Fig. 13 shows the output frequency of the VCO, run1 as a function of the tuning voltage. We measured an output power of about 5 dBm at a tuning voltage of 0 V.

Fig. 14 presents the output frequency of the VCO, run2 as a function of the tuning voltage, showing that the target frequency range is reached. An output power of about 4 dBm was observed at 0 V tuning voltage.

Fig. 15 presents the output power of the VCO with LO buffer from run2 as function of the VCO frequency, controlled by the tuning voltage, with the DC current of the VCO as parameter.

We simulate the output frequency and output power of the VCO with the LO buffer of run1 as function of the varactor capacitance using Harmonic Balance. We obtained 6.7 dBm for 58 GHz output frequency, and 5.4 dBm for 62 GHz. Good agreement with the measured output power is achieved within 2 dB

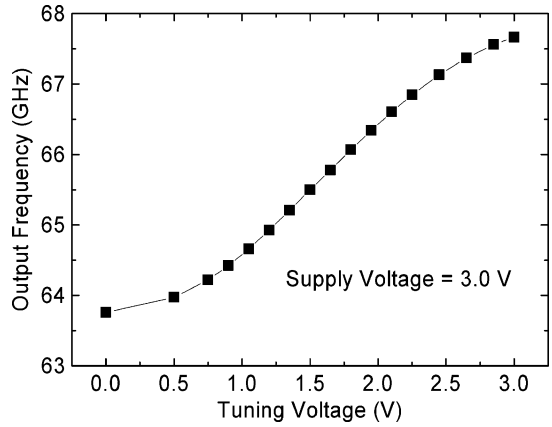

Fig. 13. VCO frequency versus tuning voltage, run1.

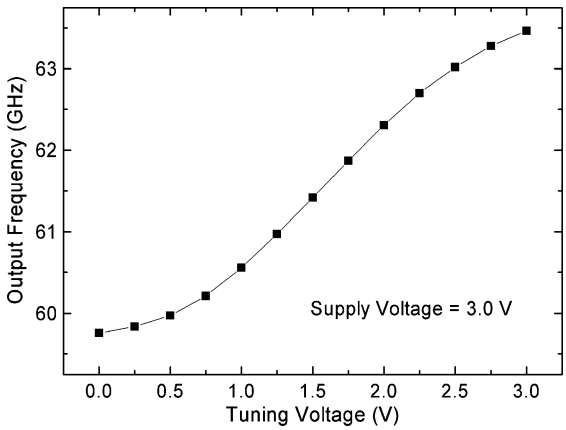

Fig. 14. VCO frequency versus tuning voltage, run2.

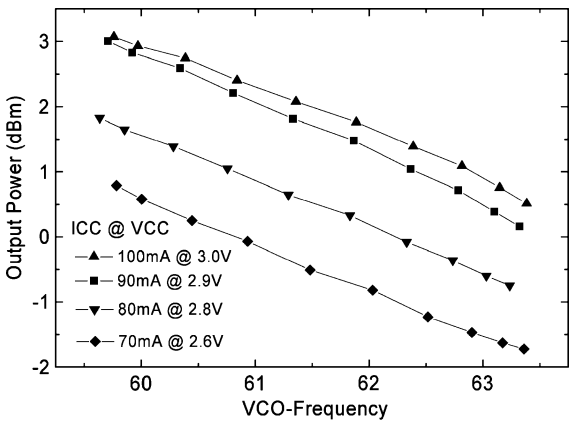

Fig. 15. VCO output power versus frequency with VCO current as parameter, run2.

tolerance. As a device model of the used varactor was not available in our design kit, we were not able to simulate the VCO frequency as function of the tuning voltage.

D. Receiver

In the following, we describe the measurement results of our iterative receiver design. The first design, fabricated in run1, worked at frequencies around 127 GHz. The subsequent design, fabricated in run2, shifted the frequency to the range around

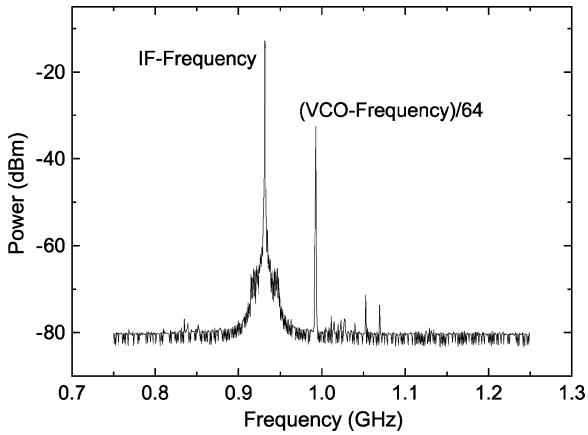

Fig. 16. IF output spectrum of the receiver, run1.

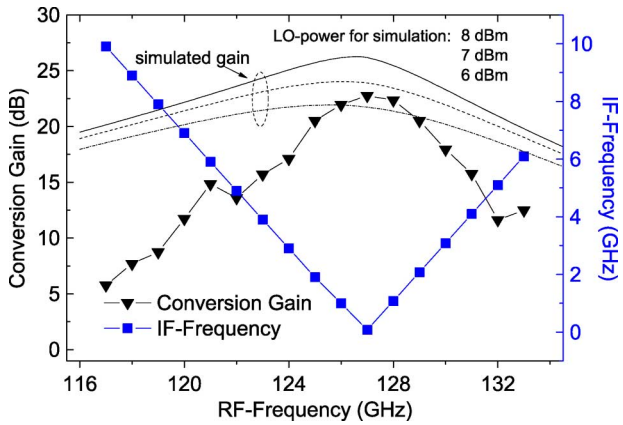

Fig. 17. Conversion gain and IF frequency of the receiver versus RF frequency, run1.

122 GHz. The last design of run3 led to improved performance of this receiver.

The simulation of the receiver on the system level was performed using Spectrasys, Agilent. The conversion gain and the NF of the receiver were simulated with the LO power as parameter using SSNA (small signal noise analysis). We simulated the conversion gain as function of the RF input power using Harmonic Balance analysis.

Results for Run1: The single ended IF output spectrum obtained for a 128 GHz RF input signal is shown in Fig. 16. Note that the 1/64 divided VCO frequency is located at 0.993 GHz, which corresponds to a VCO frequency of 63.55 GHz. We assumed that the relatively strong 1/64 VCO signal was related to the fact that the VCO did have a common ground with the frequency divider. Thus, in the subsequent runs 2 and 3 we implemented a separate VCO ground, and the 1/64 VCO leakage was reduced by few dB.

Fig. 17 shows the measured single-ended conversion gain and the IF frequency as function of the RF frequency for RF power of −50 dBm at the RF input port on wafer. The 3 dB bandwidth extends from 125 GHz to 129 GHz. The maximum differential gain is 25 dB at 127 GHz. In Fig. 17 the simulated conversion gain is plotted for LO power of 6 dBm, 7 dBm, and 8 dBm. The measured maximum gain at 127 GHz agrees well with the simulated gain for 6 dBm LO power.

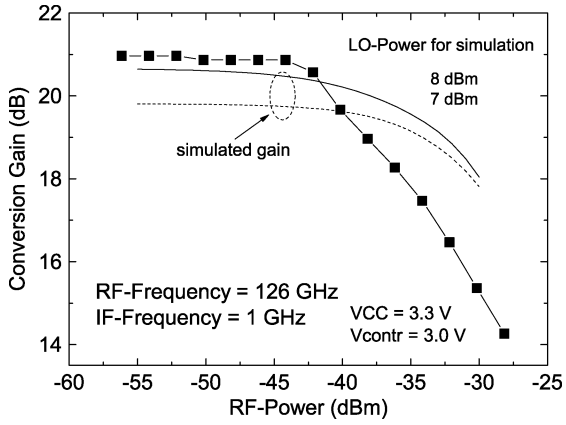

Fig. 18. Conversion gain of the receiver versus input power, run1.

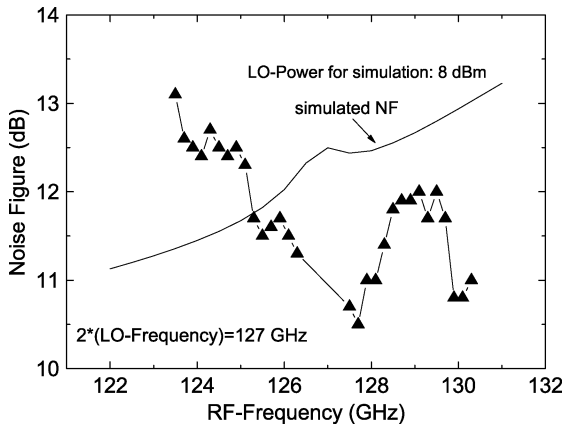

Fig. 19. Noise figure of the receiver versus RF frequency, run1.

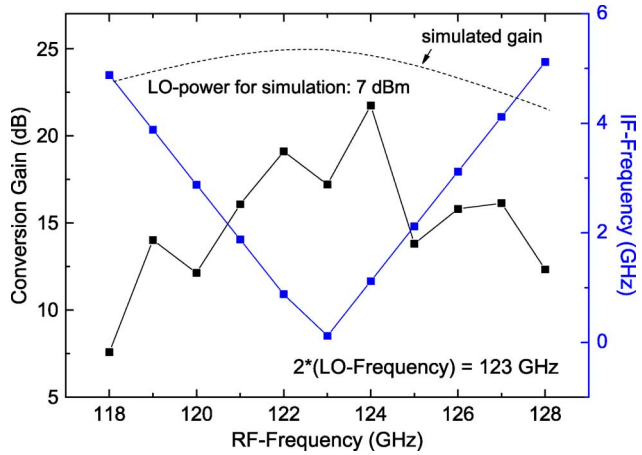

Fig. 20. Conversion gain and IF frequency of the receiver versus RF frequency, run2.

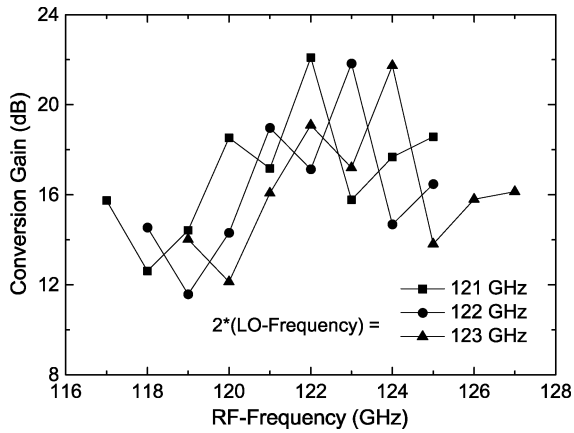

Fig. 21. Conversion gain of the receiver versus RF frequency with the LO frequency as parameter.

In Fig. 18, the single-ended conversion gain of the receiver at 1 GHz IF frequency is shown as function of the RF input power at 126 GHz. It exhibits an input 1 dB compression point of −40 dBm. The simulated dependence of the gain on the RF power for 8 dBm predicts −35 dBm.

The noise figure of the receiver was directly measured as a function of the RF frequency, as illustrated in Fig. 19. Since the 2×LO frequency is located at 127 GHz, the RF frequency range includes the sides below and above the 2×LO frequency. The minimal NF value of about 11 dB, obtained in the region from 126 to 128 GHz, corresponds to the maximum of the conversion gain. The simulated NF is plotted for 8 dBm LO power and gives a 12.5 dB NF at 127 GHz.

We simulated the cascaded gain and noise figure of the receiver on the system level assuming that an image filter is located between the LNA and mixer. If we use for the LNA 14 dB gain and 9 dB NF, and for the mixer 8 dB gain and 22 dB NF, with image filter we get for the receiver 22 dB gain and 11.5 NF. In the case without image filter we obtain 21.9 dB gain and 13.4 dB NF.

Results for Run2: Fig. 20 shows the single-ended conversion gain as function of the RF frequency and the IF frequency with the double LO frequency at about 123 GHz. The maximum gain is obtained at the RF frequency of 124 GHz. In Fig. 20 the simulated conversion gain is plotted for 7 dBm LO power. The measured maximum gain agrees well with the simulated maximum gain.

The single-ended conversion gain as function of the RF frequency with the double LO frequency as parameter is plotted in Fig. 21. Note that the maximum gain is obtained at a RF frequency higher than the double LO frequency by about 1 GHz.

In Fig. 22 the noise figure of the receiver is illustrated as a function of the RF frequency with $2*(\text{LO frequency})$ as parameter in the range from 119 GHz to 123 GHz. The minimum NF corresponds to the maximum conversion gain. The RF frequency range corresponds to the side above the double LO frequency. The minimum NF is about 11 dB. The simulated NF is given for 122 GHz with the LO power in the range from 5 dBm to 8 dBm. The simulated NF increases significantly towards the double LO frequency for lower LO power in correspondence with the measured NF. But, the strong increase of the measured NF at higher frequency does not agree with our simulations.

Results for Run3: Fig. 23 presents the single-ended conversion gain as function of the RF frequency and the IF frequency with the double LO frequency at 120 GHz. Note that the maximum gain is obtained at an RF frequency higher than the double LO frequency by 3 GHz.

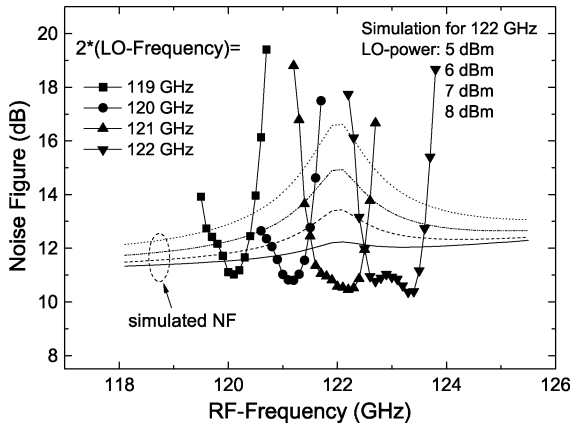

Fig. 22. Noise figure of the receiver versus RF frequency with the LO frequency as parameter, run2.

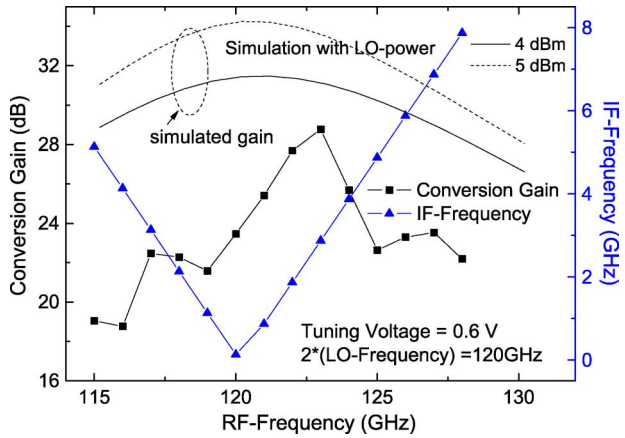

Fig. 23. Conversion gain and IF frequency of the receiver versus RF frequency, run3.

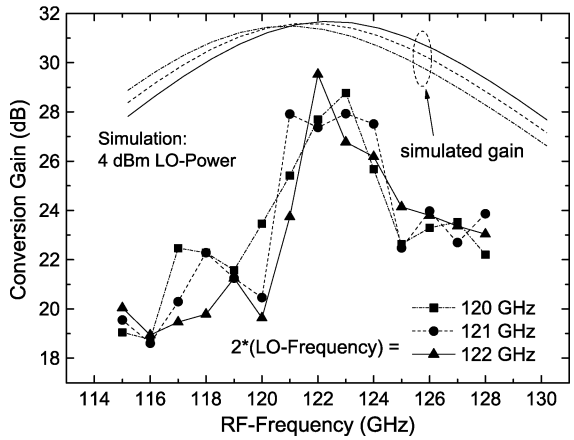

Fig. 24. Conversion gain of the receiver versus RF frequency with the double LO frequency as parameter, run3.

In Fig. 23 the simulated conversion gain is drawn for LO power of 4 dBm and 5 dBm. The measured maximum gain agrees nearly with the simulated maximum gain for 4 dBm LO power.

The single-ended conversion gain as function of the RF frequency with the double LO frequency as parameter is illustrated in Fig. 24. The 3 dB bandwidth is in the range from about

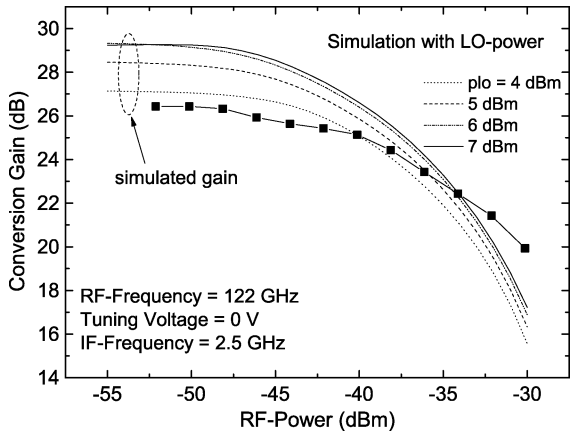

Fig. 25. Conversion gain of the receiver versus input power, run3.

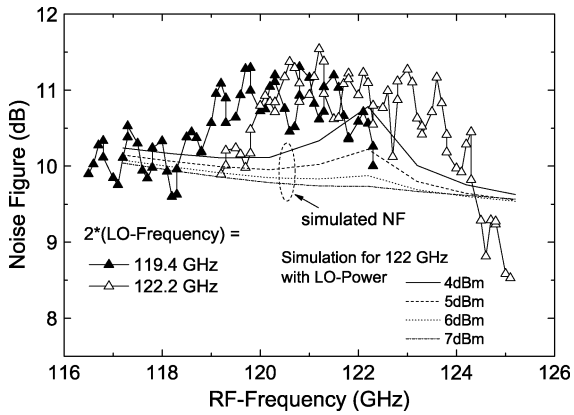

Fig. 26. Noise figure of the receiver versus RF frequency with LO frequency as parameter, run3.

121 GHz to 124 GHz, and does not change significantly with the double LO frequency at 120 GHz, 121 GHz, or 122 GHz. The simulated conversion gain is plotted for 4 dBm LO power. In difference to the simulation results the shape of the measured gain suggests strong band-filter behavior.

The maximum differential gain is 31 dB around 122 GHz, which is 9 dB higher than the 22 dB gain obtained for the LNA.

The single-ended conversion gain of the receiver at 2.5 GHz IF frequency is plotted in Fig. 25 as function of the RF input power at 122 GHz, giving an input 1 dB compression point of the input power at -45 dBm. The simulated gain is plotted with the LO power as parameter. Four dBm of LO power gives sufficient agreement with the measured data.

The noise figure of the receiver was directly measured, and is shown in Fig. 26 as a function of the RF frequency with $2*(\text{LO frequency})$ at 119.4 GHz and 122.15 GHz. The RF frequency range includes the sides below and above the double LO frequency. The maximum NF of about 11 dB, observed in the region from 119 GHz to 121 GHz and from 120 GHz to 123 GHz, respectively, is about 3 dB higher than the NF of the LNA in this range. This difference could be explained by the 3 dB of excess noise, which is expected in the case of a double-sideband mixer. An 8 dB NF of the receiver is observed at 125 GHz RF frequency.

TABLE I
SUMMARY OF MEASUREMENT AND SIMULATION RESULTS FOR THE RECEIVERS

	Run1	**Run2**	**Run3**
2*LO	127 GHz	121 GHz	122.2 GHz
LNA	14 mA at 3.3 V	As run1	15 mA at 3.3 V
LNA gain	12 dB (15dB)	14 dB (16 dB)	22 dB (22 dB)
LNA NF	10 dB (8.5 dB)	9.5 dB (8 dB)	8 dB (6.5 dB)
SHM	27 mA at 3.3 V	As run1	21 mA at 3.3 V
SHM gain	4 dB for 9 dBm LO (4 dB for 7 dBm LO)	4 dB for 9 dBm LO (4 dB for 7 dBm LO)	Without SHM test-structure
SHM NF	22 dB for 9 dBm LO (24 dB for 7 dBm LO)	22 dB for 9 dBm LO (23 dB for 7 dBm LO)	n.a.
VCO + LO buffer	98 mA at 3.0 V	As run1	77 mA at 3.2 V
VCO-frequency	(63.8 – 67.7) GHz	(59.8 – 63.5) GHz	(59.8 – 63.5) GHz
VCO + LO power	5 dBm at 63.8 GHz	4 dBm at 59.8 GHz (6.7 dBm)	4 dBm at 59.8 GHz
VCO phase noise	-96 to -100dBc/Hz at 1MHz offset	As run1	As run2
Receiver	0.46 W	0.46 W	0.37 W
differential gain	25 dB at 127 GHz (25 dB at 6 dBm LO)	25 dB at 122 GHz (27 dB at 7 dBm LO)	31 dB at 122 GHz (34 dB at 4 dBm LO)
3-dB bandwidth	(125 - 129) GHz ((118 – 132) GHz at 6 dBm LO)	(121– 122.5) GHz ((119 – 126) GHz at 6 dBm LO)	(121 – 124) GHz ((118 – 128) GHz at 4 dBm LO)
Input P1dB	-40 dBm (-35 dBm at 8dBm LO)	As run1	-45 dBm (-45 dBm at 4 dBm LO)
Noise figure	11 dB at 128 GHz (12.5 dB at 8dBm LO)	10 dB at 122 GHz (13 dB for 7 dBm LO)	11 dB at 122 GHz (10.5 dB for 4 dBm LO)

We simulated the cascaded gain and noise figure of the receiver on the system level as for the receiver of run1. If we use for the LNA 22 dB gain and 8 dB NF, and for the mixer 6 dB gain and 21 dB NF, with image filter we obtain for the receiver 28 dB gain and 8.5 NF. In the case without image filter we obtain 27.9 dB gain and 11.1 dB NF.

The performance of the receivers, fabricated in the three subsequent runs, is summarized in Table I and compared with the simulation results.

V. DISCUSSION OF RECEIVER RESULTS

The development of the 122 GHz receiver was accomplished basing mainly on simulations and optimizations in the GoldenGate/ADS design environment including planar 2.5D EM-simulation. Restrictions in accuracy of these simulations result from limitations in the models of active and passive components at this high operating frequency and in the limitation in the regard of the final test setup. In the following, the receiver results of the three runs are discussed.

TABLE II
COMPARISON OF mm-WAVE RECEIVERS

	Frequency	Differ. Gain	NF	P1dB	Power DC	SiGe-BiCMOS f_T/f_{max}	Chip-Size	Notes
Laskin [9]	140GHz	30dB	12dB	n.a.	1.5W	0.13µm 230GHz/ 280GHz	1.4mm^2	With IF-amplifier Together with transmitter
Laskin [8]	160GHz	-3dB	n.a.	-20dBm	0.9W	0.13µm 270GHz/ 340GHz	1.2mm^2	Together with transmitter
Pfeiffer [29]	160GHz	25dB	14dB	n.a.	1.5W	DotFive 260GHz/ 380GHz	1.1mm^2	Quadrature receiver
This work, [18]	127GHz	25dB	11dB	-40dBm	0.46W	0.13µm 255GHz/ 315GHz	0.6mm^2 w/o outer pads	Subharmonic mixer
This work	122GHz	31dB	11dB	-44dBm	0.37W	0.13µm 245GHz/ 350GHz	0.6mm^2 w/o outer pads	Subharmonic mixer

We observed for the receiver, fabricated in run1, a maximum differential gain of 25 dB at 127 GHz, and a minimal NF of about 11 dB in the range from 126 GHz to 128 GHz, which is only slightly higher than the 10 dB NF of the LNA. The 3 dB bandwidth of the conversion gain is 125 GHz to 129 GHz, whereby the highest gain corresponds to the lowest IF output frequency. The bandpass behavior is considerably stronger pronounced in the measured conversion gain than in the simulated gain due to the limitations mentioned above.

In our receiver with double-sideband mixer, we would expect 3 dB of excess noise due to the noise contribution at the image frequency, meaning 13 dB NF of the receiver. However, RF bandpass filtering could reduce this noise contribution. The receiver gain of 22 dB at 127 GHz is 5 dB higher than the value, which we obtained by adding the 13 dB gain of the LNA with capacitive coupling and the 4 dB measured gain of the SHM. This indicates that the output power of the integrated VCO is higher than the 5 dBm measured for the separate VCO chip with balun at the output, and that the conversion gain of the integrated SHM is also higher than the measured value of the separate SHM test structure with balun at the output. Therefore, the better performance of the VCO and SHM in the receiver can be explained by an optimized matching between the VCO and SHM, and between the LNA and SHM in the receiver.

The frequency range of our receiver fabricated in run2 was shifted to the target frequency around 122 GHz by a redesign of the VCO. The maximum gain and the minimum NF were now achieved at RF frequencies in the upper sideband, which correspond to an IF frequency of about 1 GHz. The maximum gain is 22 dB, and the minimum NF is about 10 dB. But, this receiver is only suitable for applications, where down-conversion to about 1 GHz IF frequency is possible. In the case of lower IF-frequencies, the noise contribution of the SHM increases the NF of the receiver. We reduced this SHM noise contribution in the subsequent receiver design mainly by implementing an LNA with higher gain. The lower NF of the SHM due to higher output power of the VCO with LO buffer seems also feasible.

In the subsequent run3, we accomplished an LNA design with built-in bandpass filtering around 122 GHz, with maximum gain of 22 dB at 122 GHz, and 8 dB NF in the range 120–130 GHz. This leads to a maximum gain of this receiver with 28 dB gain at around 122 GHz. The 3 dB bandwidth is 121–124 GHz for the double LO frequency at 122 GHz. Here, the maximum NF of the receiver is 11 dB at 122 GHz, which is about 3 dB higher than the NF of the LNA in this range. This difference is related to the 3 dB of excess noise, which is expected in the case of a double-sideband mixer. A lower NF of 8 dB was detected at RF frequency of 125 GHz, corresponding to 3 GHz IF frequency. This decreased NF should be attributed to the utilized RF bandpass filtering.

Table II compares the technical data of our receiver with the state-of-the-art.

VI. CONCLUSION

A subharmonic receiver at frequencies above 120 GHz has been presented with record conversion gain and noise figure. The receiver incorporates an LNA, push-push VCO, 1/32 frequency divider, polyphase filter, and subharmonic mixer. PLL function can be implemented in this design by taking advantage of the integrated frequency divider. The receiver is fabricated in SiGe:C BiCMOS technology with $f_T/f_{\max}$ of 255 GHz/315 GHz. The receiver was optimized by an

iterative design starting with 25 dB maximum differential gain at 127 GHz. We used three subsequent fabrication runs (run1, run2, and run3) of this technology for the fabrication of our receiver. The vertical profile of the SiGe:C HBT was optimized for run3, leading to $f_T/f_{\max}$ of 245 GHz/350 GHz. The measurement results of the runs 1, 2, and 3 are in reasonable agreement with the simulation results obtained by using the design kit model for the runs 1 and 2, and an adapted HBT model for the run3. The receiver of run3 demonstrated a maximum differential gain of 31 dB and a measured noise figure of 11 dB at 122 GHz, while only dissipating 0.37 W of power. A NF of 8 dB was obtained at 3 GHz IF frequency using integrated RF bandpass filtering induced by the LNA itself.

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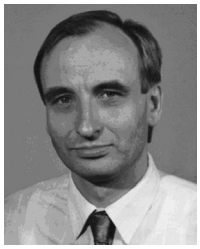

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