A Passive I/Q Millimeter-Wave Mixer and Switch in 45-nm CMOS SOI

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***Abstract*—This paper presents passive integrated circuits for millimeter-wave transmitters and receivers implemented in a 45-nm CMOS silicon-on-insulator (SOI) process. The advantages of SOI over bulk CMOS are discussed for millimeter-wave passive circuits. First, a single pole double throw (SPDT) switch demonstrates a measured insertion loss of less than 1.7 dB at 45 GHz and third-order intermodulation intercept point (IIP3) of 18.2 dBm. Second, a double-balanced passive in-phase/quadrature (I/Q) mixer exhibits a conversion loss of 8.35 dB at 44 GHz and IIP3 of 15.5 dBm. At a fixed IF of 200 MHz, the minimum I/Q gain and phase imbalance is 0.25 dB and 1.9°. The passive mixer and SPDT switch results demonstrate a record minimum insertion loss and linearity performance for the passive millimeter-wave circuits.**

***Index Terms*—CMOS, 45 nm, in-phase/quadrature (I/Q), passive mixer, silicon-on-insulator (SOI), single-pole double-throw (SPDT) switch.**

I. Introduction

HIGHLY SCALED digital CMOS silicon-on-insulator (SOI) is an excellent candidate platform for digital, analog, and RF integration in a monolithic system-on-chip (SOC) package. Monolithic integration in CMOS SOI minimizes the system and packaging complexity, reduces system variability, and supports embedded RAM and microprocessors for radiation hard applications [1]. Other benefits of the SOI devices include negligible substrate leakage, higher isolation, and increased $f_t/f_{\max}$. Therefore, fine-line CMOS SOI is a good candidate for low-loss, high-isolation, and high-linearity switches. However, the application of digital CMOS SOI technologies for RF applications requires more than device scaling. Passive devices, such as inductors, baluns, transmission lines, and pads, degrade as metallization dimensions are scaled down to increase the transistor speed and the integration density. Nonetheless, a variety of efforts based on scaled CMOS SOI technology have demonstrated high-performance low-noise and power amplifiers, mixers, and single-pole double-throw (SPDT) switches [2]–[6].

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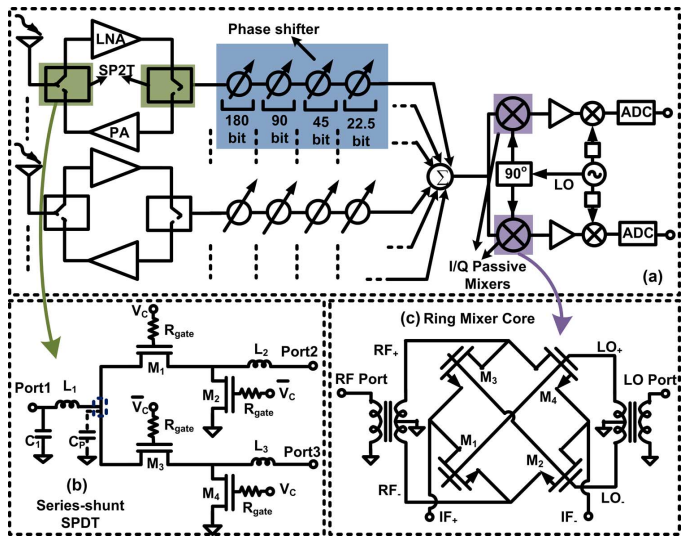


Fig. 1. (a) Block diagram for RF phase-shifting beamformer transceiver with the: (b) SPDT switch and (c) I/Q mixer implemented as passive elements.

Future beamforming systems and phased arrays will be central components for indoor/outdoor surveillance, intelligent sensing, and imaging sensors that require significantly low power consumption. Fig. 1(a) shows the block diagram of a low-power RF phase-shifting beamformer transceiver with several key front-end circuits including the SPDT switch, phase shifter, and in-phase/quadrature (I/Q) mixer implemented as passive circuit blocks. The performance of the passive circuit blocks are dependent on the performance of the switches. The SPDT switch is realized by switching the port 1 between ports 2 and 3 with the help of on/off field-effect transistors (FETs) as switches, as shown in Fig. 1(b). The SPDT switch combines the series and parallel switches to provide isolation between the transmitter and receiver. The switch must exhibit low insertion loss to maintain high transmitter efficiency, output power, and low receiver noise figure to achieve reasonable signal-to-noise ratio (SNR). High linearity is also important to prevent the compression and intermodulation distortion. The passive ring mixers are realized by switching FET gates of a ring topology and biasing the transistor gates at the threshold voltage, as shown in Fig. 1(c). The insertion loss and linearity of the switch determines the performance of the mixer. The phase shifters are composed of cascaded switch elements and the insertion loss of the phase shifter is the sum of the losses through the switches, which generally increases with phase-shift range. The FET channel resistance, $R_{\rm ch}$, and insertion loss of a switch should improve with the CMOS scaling, and consequently, both resistive mixer conversion loss and SPDT insertion loss should demonstrate improvements in fine-line CMOS SOI.

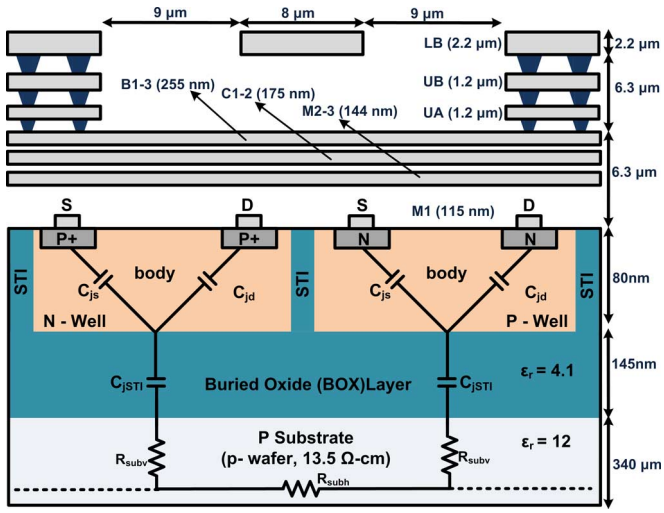


Fig. 2. Cross section of a 45-nm SOI CMOS process.

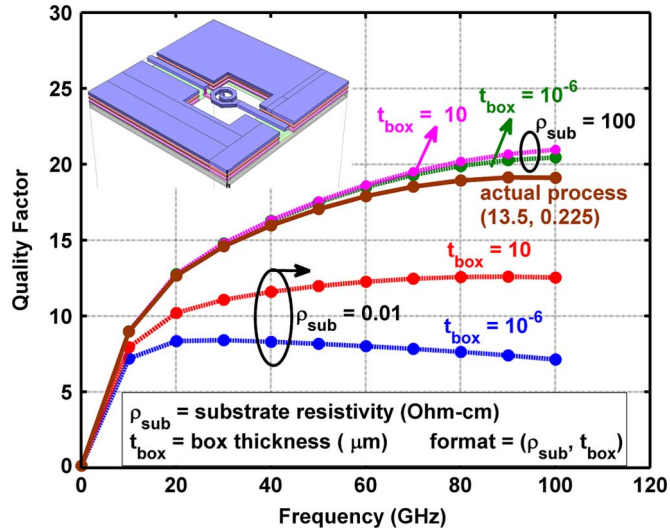


Fig. 3. Effect of the BOX thickness and substrate resistivity on the quality factor of inductors.

In Section II, the 45-nm CMOS SOI process and passive operation performance at millimeter-wave bands is introduced. Circuit analysis, simulation, and measurements of a broadband SPDT switch and the I/Q passive mixer are presented in Sections III and IV. The results indicate that 45-nm CMOS SOI demonstrates the lowest switch insertion loss and lowest conversion loss compared to other CMOS processes.

II. 45-nm SOI CMOS Process

In Fig. 2, the 45-nm SOI CMOS process is shown. In the SOI process, eleven metal layers are available with a 2.2-μm-thick aluminum top metal layer (LB). The SOI substrate is a p-doped "handle" wafer with a resistivity of 13.5 $\Omega \cdot$ cm and is isolated from the active region with a thin buried oxide (BOX) layer, which isolates the transistor from the substrate. The BOX thickness is 145 nm in this process—roughly three times the minimum gate length. Nonetheless, the BOX mitigates many of the problems associated with bulk processes at millimeter-wave frequencies. The BOX layer isolates the active transistor area from the substrate without degrading the voltage threshold of the n-channel FET (NFET). Shallow trench isolation (STI) provides isolation between transistor diffusions and extends 80 nm through the active silicon layer.

These process features mitigate some limitations of bulk CMOS transistors when used as a switch. The junction diode between the source/drain node and the substrate, $C_{\rm jd}$ and $C_{\rm js}$, is much less compared to the one in bulk processes enabling high isolation. The junction capacitances are limited to the BOX capacitance and are 4–7 times smaller than in bulk CMOS. As shown in Fig. 2, the substrate resistance network, $R_{\rm sub}$, from the junction to the substrate ground is isolated due to the BOX layer and $C_{j\rm STI}$ in the SOI CMOS process compared to the uncertain value of $R_{\rm sub}$ in bulk CMOS resulting in the insertion loss and isolation discrepancies. The SOI process offers body-contacted NFETs (f_T of 280 GHz) and floating-body NFET (f_T of 380 GHz) with low drain/source coupling to the substrate and low high-frequency noise.

The effect of the substrate resistivity and BOX thickness on the quality factor (Q) of the spiral inductors is investigated using SONNET in Fig. 3. The spiral inductor Q is investigated as a function of frequency for different combinations of substrate resistivity and BOX thickness.

When the substrate resistivity is increased from 0.01 to 13.5, the Q increases significantly. Increasing its resistivity beyond 100 $\Omega \cdot$ cm reduces the impact of thinner BOX on parasitic capacitance and also improves the Q. With a highly resistive substrate, the BOX thickness has an insignificant effect on the Q. However, the Q increases with the increasing BOX thickness when the substrate is more conductive. Higher Q is mainly attributed to the increasing substrate resistivity of the SOI wafer beyond 10 $\Omega \cdot$ cm, which dramatically decreases coupling loss to the Si substrate.

A vertical natural capacitor model (VNCAP) is formed with inter-digitated metal fingers composed of C1–B3 metal layers with a density of 1.8 fF/μm^2. Lower metal layers are not used since they result in higher parasitic shunt capacitance for a given series capacitance, which degrades the performance at millimeter-wave frequencies. A shielded coplanar waveguide (CPW) transmission line is designed using LB for the signal line and B3 for the ground plane, and the LB side grounds are connected to B3 using UA and UB metal layers, as shown in Fig. 2. A signal line width of 8 μm with 9-μm spacing to the side grounds results in a 50-Ω transmission line at millimeter-wave frequencies.

A. SOI CMOS Process Versus Bulk CMOS

A small-signal model of the switch in the on and off states are illustrated in Fig. 4. When the FET is on and off, the equivalents impedances $Z_{\rm on}$ and $Z_{\rm off}$ are

$$Z_{\rm on} = R_{\rm ch} = \frac{L_g}{\mu_n C_{\rm ox} W_t (V_{\rm gs} - V_t)} \quad (1)$$

$$Z_{\rm off} = \frac{1}{j\omega_{\rm RF} C_{\rm eqv.}} \quad (2)$$

$$C_{\rm eqv.} = C_{\rm gs} \parallel C_{\rm gd} + C_{\rm js} \parallel C_{\rm jd} \quad (3)$$

where $C_{\rm gs} \simeq W_t L_g C_{\rm ox}/2$.

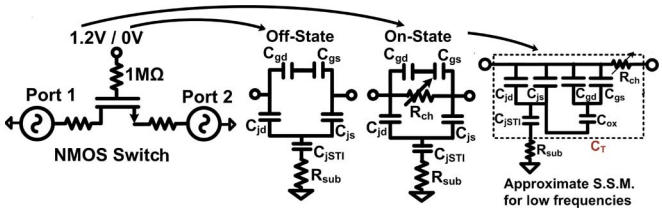


Fig. 4. Test bench for an nMOS switch and its simplified small-signal circuit model in the ON and OFF states.

The $Z_{\rm on}$ impedance is dominated by the channel resistance $R_{\rm ch}$. The $Z_{\rm off}$ impedance is dominated by the parasitic capacitances—parallel combination of the series capacitance of the gate–drain and gate–source capacitances ($C_{\rm gd}$ and $C_{\rm gs}$) and series capacitance of the drain and source junction capacitances ($C_{\rm jd}$ and $C_{\rm js}$).

B. Insertion Loss and Isolation of a Series Switch

The insertion loss is determined mostly by the $Z_{\rm on}$ impedance. A larger FET width, W_T, provides lower channel resistance and lower insertion loss. However, it also reduces the off-state impedance $Z_{\rm off}$, degrading the isolation. The choice of W_T establishes the tradeoff between $Z_{\rm on}$ and $Z_{\rm off}$, and between insertion loss, isolation, and linearity. In the off-state, $R_{\rm ch}$ is high. Since $C_{\rm eqv.}$ is proportional to W_T, increasing the off-impedance requires a smaller device width, W_T.

To assess the impact of the BOX layer and substrate resistance, the insertion loss from a single MOS transistor has been analyzed based on the MOS transistor shown in Fig. 4. Since the impedance of the junction capacitance is very low at millimeter-wave frequencies, the substrate resistance $R_{\rm sub}$ plays a critical role. It has been shown that insertion loss can be reduced by increasing $R_{\rm sub}$ to a very large value or by decreasing $R_{\rm sub}$ to near zero [7]. In terms of the underlying physical mechanism, when $R_{\rm sub}$ becomes large, signals cannot couple through $R_{\rm sub}$ and the power delivered to $R_{\rm sub}$ is small. When $R_{\rm sub}$ is zero, there is no loss associated with $R_{\rm sub}$ and the power loss is once again reduced. In this digitally compatible SOI process, $R_{\rm sub}$ is smaller comparatively to the other technologies and the BOX layer provides a capacitance $C_{j\rm STI}$ that is small and isolates the body from the substrate. In other words,

$$C_T = \left(\frac{(C_{\rm gs} + C_{\rm gd})\, C_{\rm ox}}{C_{\rm gs} + C_{\rm gd} + C_{\rm ox}} + C_{\rm js} + C_{\rm jd} \right) \parallel C_{j\rm STI} \qquad (4)$$

is the equivalent capacitance shown in the approximate small signal model in Fig. 4. C_T is 0 when $C_{j\rm STI} \sim 0$ and when $C_T = 0$, the insertion loss is defined by [7]

$$\text{IL} \sim \left(\frac{R_{\rm ch} + 2Z_0}{2Z_0} \right)^2 \text{ when } C_T = 0 \qquad (5)$$

which is used to estimate the insertion loss at low frequencies. The insertion loss and isolation of a series switch is compared in Fig. 5(a) against various CMOS processes at 45 GHz. In bulk processes, higher insertion loss results from high channel resistance of the ON switch and coupling loss through the substrate via parasitics. Therefore, deep n-well transistors, high substrate contact resistance, and deep trench isolation are provided for bulk CMOS in the literature. As shown in Fig. 5(a), the insertion loss starts to degrade again after an optimum value of transistor width since signals start to leak to the substrate through the parasitics in bulk processes (i.e., 50 μm for 90-nm processes). In the CMOS SOI process, selecting larger transistor width enables to design switches, passive mixers, and passive phase shifters with less insertion/conversion-loss characteristics. Fig. 5(b) shows the isolation of the switch in various technologies. Although $C_{\rm jd}$ and $C_{\rm js}$ are much smaller compared to bulk CMOS devices, $C_{\rm gd}$ and $C_{\rm gs}$ are comparable to 130- and 45-nm CMOS and the SOI process do not improve the series transistor isolation.

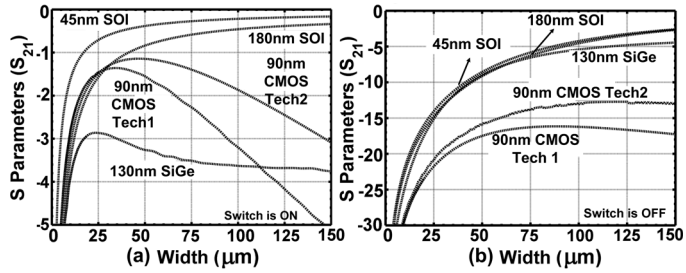


Fig. 5. Insertion loss and isolation of a series transistor switch versus transistor width in various technologies at 45 GHz.

III. SPDT Switch Circuit Design and Measurements

RF transceivers use an SPDT switch to isolate the transmitter and receiver. The switch must exhibit low insertion loss to maintain high transmitter efficiency, output power, and low receiver noise figure. High linearity is also important to prevent intermodulation distortion. Previously, SPDT switches have been demonstrated using bulk CMOS processes, which tend to increase the signal coupling to the semiconductive silicon substrate at millimeter-wave bands [8], [9], as reported in [10]. In bulk processes, higher insertion loss and lower isolation is found as a result of resistive coupling through the substrate. CMOS SOI processes improve the insertion loss and isolation of millimeter-wave SPDT switches [6].

Shown in Fig. 6 are four different topologies for SPDT switches, which switch between port 1 and ports 2 and 3. The switches consist of NFETs with aspect ratio of 40 μm/45 nm. The return loss of each design is simulated to be better than 25 dB. The $\lambda/4$ transmission line in the shunt–shunt switch creates an open circuit at the common node when the shunt FET is biased at triode, which limits the bandwidth of the switch. On the other hand, the series-shunt switch is more broadband and offers more compact layout. However, neither the series-shunt and shunt–shunt switches tend to offer as much isolation as the series-shunt cascaded switches ($>$ 60 dB). The additional series FETs degrades the insertion loss. A comparison of the insertion loss and isolation for each type of switch is shown in Fig. 7. The series-shunt switch offers the lowest insertion loss and highest bandwidth with acceptable isolation.

Fig. 1(b) shows the implemented SPDT switch schematic based on a combination of two series-shunt SPST circuits with input and output matching networks [10]. Electromagnetic (EM) simulation models series inductors at ports 1–3 to isolate the parasitic capacitance. As shown in Fig. 1(b), the capacitance at the common node is matched using a wideband

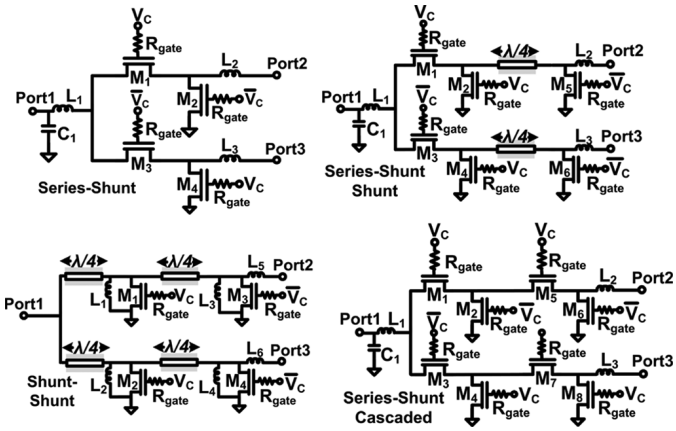
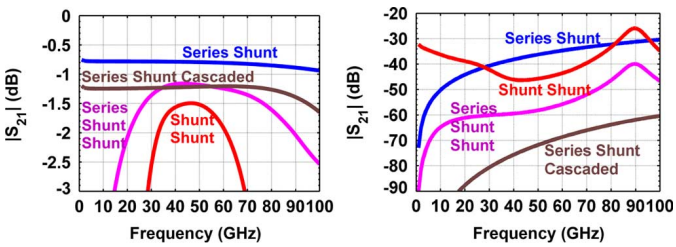


Fig. 6. Various SPDT circuit architectures.



(a) (b)

Fig. 7. Comparison of the simulated insertion loss and isolation for various SPDT circuit architectures.

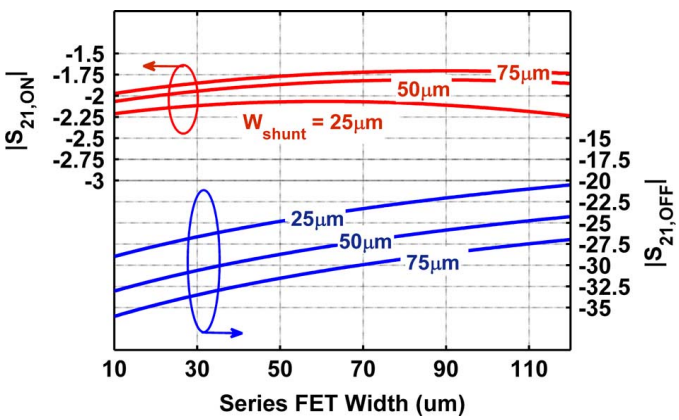


Fig. 8. Simulation for the optimization for series and shunt transistor width.

$C_P - L_1 - C1$ circuit, where $L_1 = 198$ pH and $C1 = 52$ fF. The output matching circuit is implemented using a series 115-pH inductor. The insertion loss and isolation are plotted as a function of the FET width, W_T, as shown in Fig. 8. The insertion loss is mostly dependent on the size of the series FET, M_1. As W_T increases, the parasitic capacitance also increases the capacitive coupling to the substrate and eventually results in unacceptable signal loss.

As explained in Section II-A, the 45-nm SOI process enables to choose a larger device width without degrading the isolation of the switch. $M1$ is chosen as 90 μm with 30 fingers for a minimum insertion loss of 1.8 dB at 45 GHz. Next, the shunt size is chosen based on the required isolation. The isolation improves with a wider shunt FET; however, in this case, it requires a large shunt inductor to resonate out the equivalent capacitance of the FET in the off-state. An FET width of 50 μm (25 fingers) is chosen for an isolation of 26 dB, as shown in Fig. 8, and maintains more than 60 GHz of bandwidth.

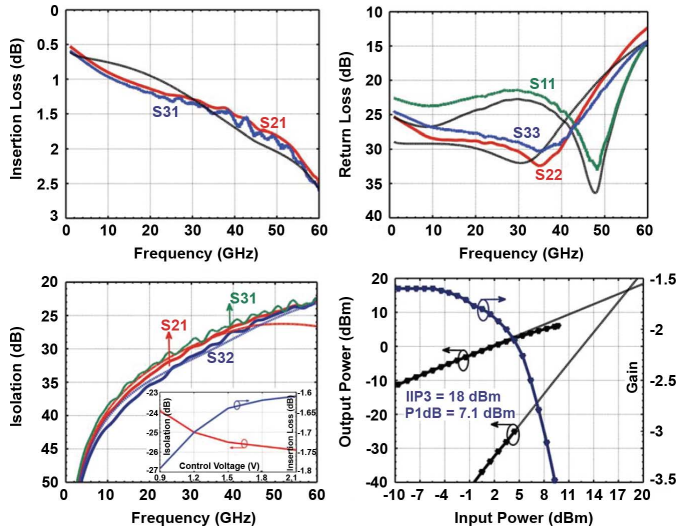


Fig. 9. Measurement results of the insertion loss, return loss, isolation, and high power handling of the SPDT switch.

The SPDT switch is fabricated in a 45-nm SOI CMOS process. The switch active area is 0.18 mm $\times$ 0.22 mm (0.04 mm^2), not including the pads. S-parameter measurements were performed to 60 GHz using the 67-GHz Agilent E8361A PNA and 60-GHz RF probes. As shown in Fig. 9, the SPDT results in an insertion loss of 1.7 dB at 45 GHz and less than 2.5 dB at 60 GHz with excellent input and output match. The measured insertion loss and reflection coefficient are nearly identical for port 2 and port 3, showing the symmetry of the layout, and agreement with simulations. The measured isolation between the two output ports is better than 25 dB at 45 GHz. The power-handling capability was measured at 45 GHz using an Agilent E8257D signal source, an Agilent V8486A V-band power sensor, and the results are also confirmed with the Agilent E4448A spectrum analyzer. The switch results in a P1 dB of 7.1 dBm and a third-order intermodulation intercept point (IIP3) of 18.2 dBm at 45 GHz. [10] presents the comparison of the 45-nm SOI SPDT switch design with other reported millimeter-wave CMOS and III–V SPDT switches indicating that this design offers similar bandwidth and lowest insertion loss compared to those implemented in bulk CMOS technologies.

IV. I/Q Passive Mixer

Passive mixers realize the highest linearity and eliminates the $1/f$ noise contribution. The primary drawback of the passive mixer is high conversion loss. However, the FET channel resistance improves with device scaling and both resistive mixer conversion loss and noise figure improve due to the FET scaling, consequently. Double-balanced mixers generally help eliminate the LO-to-RF and LO-to-IF feedthrough.

Additionally, the double-balanced passive mixer is inherently bidirectional allowing the I/Q mixer to be used for both up-conversion and down-conversion. Sharing components between the transmit and receive paths greatly simplifies the implementation of phased arrays.

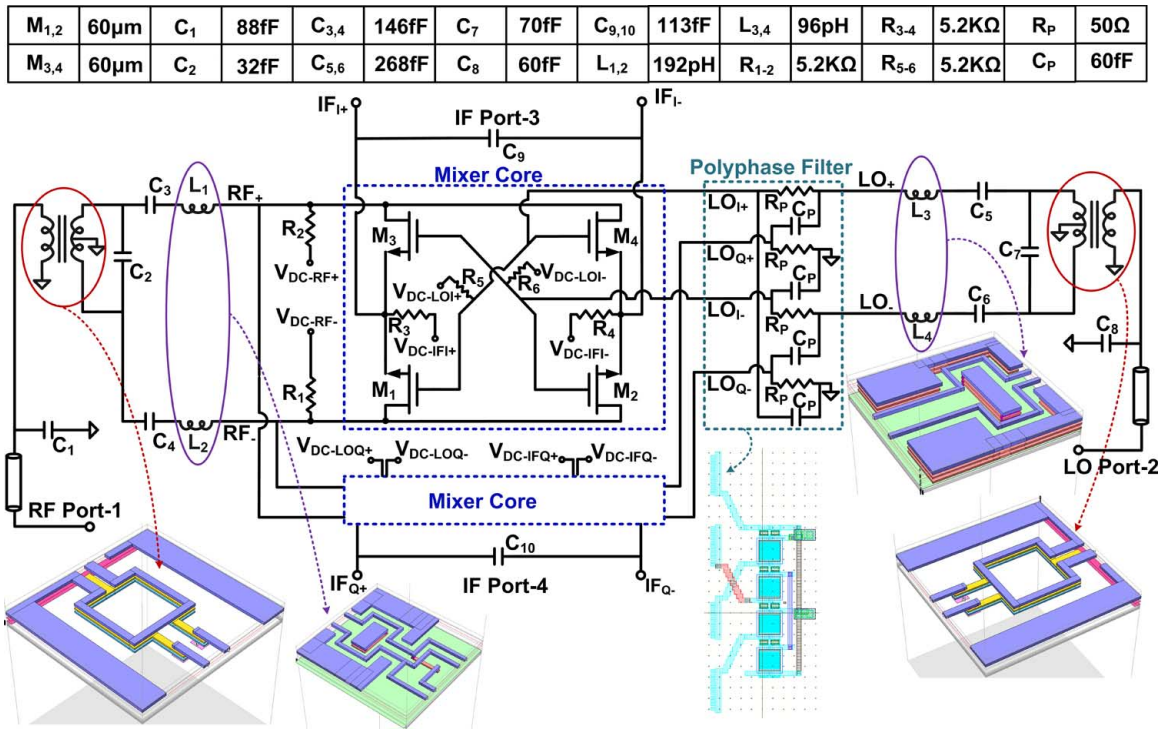


Fig. 10. Circuit schematic of the I/Q passive resistive ring mixer and illustrating the associated passive models.

A simplified schematic and equivalent circuit of the balanced resistive ring mixer is presented in Fig. 1(c). When the gate voltage bias is below the threshold voltage, the switch is off and the channel resistance is high with a set of parasitic capacitances in parallel. When the switch is on, the on-impedance is dominated by the channel resistance $R_{\rm ch}$. The bandwidth of the resistive mixer is basically controlled by the on impedance and the associated capacitances. Increasing the FET size decreases the RF bandwidth because of the larger capacitance. On the other hand, decreasing the device size is detrimental to the conversion loss. A tradeoff also exists between linearity, conversion loss, and matching. Wider FETs provide lower on-resistance, which improves conversion loss. However, increasing the FET width increases parasitic capacitance and contributes to worse linearity, port-to-port isolation, and the requirement for higher local oscillator (LO) power.

A. Circuit Design

The schematic of the I/Q mixer is illustrated in Fig. 10 along with the layout for inductors, baluns, and transmission lines. The LO signal of the mixer is used to drive the channel resistance of the FET. To reduce the conversion loss for moderate LO power, the gates of the mixing transistors, M_1–M_4, are biased near the threshold voltage with on-chip biasing. The transistor bias condition is crucial for mixer conversion gain and return losses of the RF and LO ports. The RF, IF, and LO bias voltage should be set correctly to minimize the conversion loss. As shown in Fig. 10, the dc path at the drain, source, and gate has been realized with resistors R_1, R_2, and R_3 of 6 kΩ. Ten dc pads are placed in the final circuit to tune the passive mixer for minimum conversion loss, I/Q gain, phase mismatch, and return losses.

The conversion loss contours are simulated with RF (IF) and LO bias voltage, as shown in Fig. 11. The minimum conversion loss occurs when the difference in the dc bias across the LO and RF (IF) ports is set to 0.3 V, roughly the threshold of the floating body NFET. The minimum conversion gain mismatch occurs when the difference in the dc bias across the LO and RF (IF) ports is set to 0.35 V and the respective dc bias is kept the same for both in-phase and quadrature mixers.

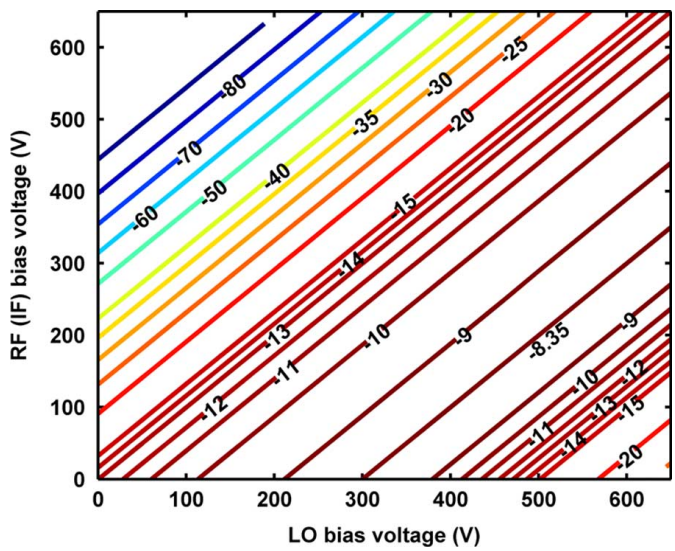


Fig. 11. Simulated conversion loss contours.

1) Differential Generation: Single-ended to differential conversion is provided at the RF and LO ports of the mixer with a passive balun. The IF port is differential to allow homodyne mixing. The IF signals are fed to the pads through a CPW line from the center of the chip. For a balun with a primary or a secondary inductor with more than one turn, a gain and phase imbalance cannot be avoided [11]. The passive spiral balun, shown in Fig. 10, has a one-turn primary square inductor using the top

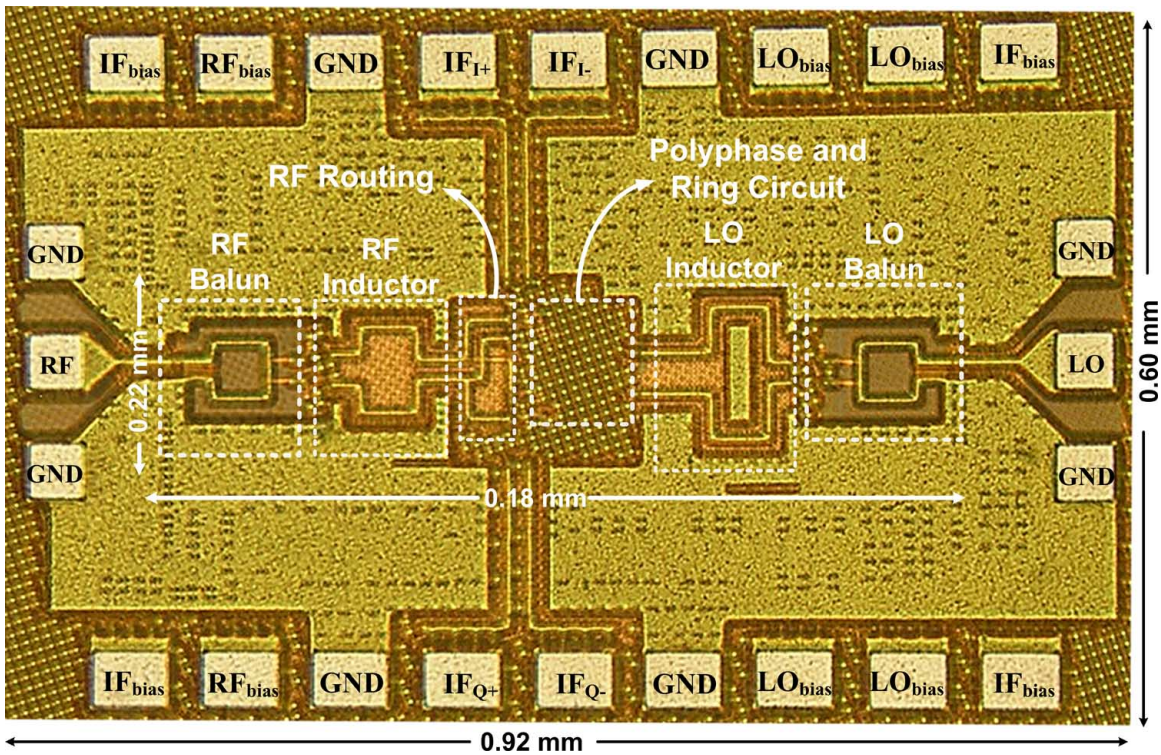


Fig. 12. Chip microphotograph of the mixer.

metal layer LB, and the secondary coil comprising stacked UB and UA metals, as shown in Fig. 10. The grounded nodes are connected to the UB layer through vias. Magnetic coupling occurs vertically between the primary and secondary coil. The distance to the ground plane is 17 μm on each side and the trace width is 5 μm. The thickness between the metal layers LB and UB is 3.3 μm and determines the resonant frequency of the balun. The core balun has a size of 5 and 56 μm and has a resonant frequency of 128 GHz for three ports terminated into 50 Ω. The balun has a gain imbalance of 0.3 dB and a phase imbalance of 1.5° at 45 GHz.

2) Quadrature Generation: Quadrature LO generation is based on an RC polyphase filter, which is satisfactory for the bandwidth required in this application. The RC filter can be designed for accurate amplitude balance over a wideband, but the correct quadrature phase relationship occurs only at the center frequency. Alternatively, the phase relationship can be wideband at the expense of amplitude balance.

The constant phase structure polyphase circuit is illustrated in Fig. 10. With increasing frequency, additional effects are considered, such as parasitic capacitances of the filter resistors, the interconnect inductance, and the finite Q of the filter capacitors. Final optimized polyphase filter component values were based on simulations of the extracted layout. The filter resistor values are chosen to be $R_1 = 50\ \Omega$ (two p+ doped polysilicon resistors in parallel), leading to a required capacitor of $C_1 = 70$ fF (vertical natural capacitors) at the filter resonance frequency $f_{\mathrm{PPF}} = 1/2\pi RC = 45$ GHz. The simulated transfer loss due to polyphase filter is 3.3 dB at 45 GHz and the maximum absolute gain variation is 0.2 dB from 40 to 50 GHz, which restricts the LO signal to be relatively narrowband. Multistage polyphase circuits remedy the situation at the expense of additional insertion loss. Due to the lossy passive components, the insertion loss of the LO input network is around 7 dB and LO power delivered to the mixer is less than 14 dBm when a LO signal of 20 dB is applied at the LO port. To drive the mixer in the test setup, a Q-band amplifier is placed at the LO port to generate enough LO power.

3) Matching Networks: A multistage, π network at the RF input is formed from a 88-fF shunt capacitor, C_1 at the input, the RF balun, a 32-fF differential capacitor, C_2 at the balun output, and 146-fF series capacitors, $C_{3\text{–}4}$. Similarly the LO matching network is formed with a 60-fF shunt capacitor, C_8, the LO balun, a 70-fF differential capacitor, C_7, and 268-fF series capacitors, $C_{5\text{–}6}$. Resonant elements are not included for matching at the IF output port. To attenuate the high-frequency LO and RF signal, capacitors C_9 and C_{10} have been added to the IF outputs to provide a low-impedance path to ground for the input RF and LO signals at higher operation frequencies. Additionally, wideband on-chip bypass networks composed of a 5-Ω polysilicon resistor in series with 0.6–2-pF thick-oxide capacitor banks have been connected to the power supply lines to clean the dc voltages.

B. Measurements

The chip microphotograph of the passive resistive ring mixer chip is shown in Fig. 12. The area excluding the RF and dc pads is 0.18 mm $\times$ 0.22 mm ($\sim$ 0.40 mm^2).

S-parameters are measured on-wafer with the Agilent E8361A network analyzer. The RF and LO signals are provided via GGB Model 50-A ground–signal–ground (GSG) probes. The RF and LO input signals are generated by two

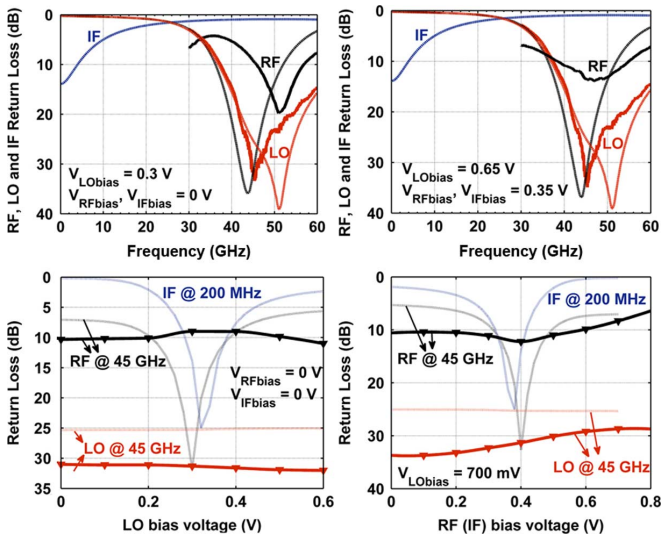


Fig. 13. Measured (solid) and simulated (dashed) RF/LO/IF port return loss with various voltage control.

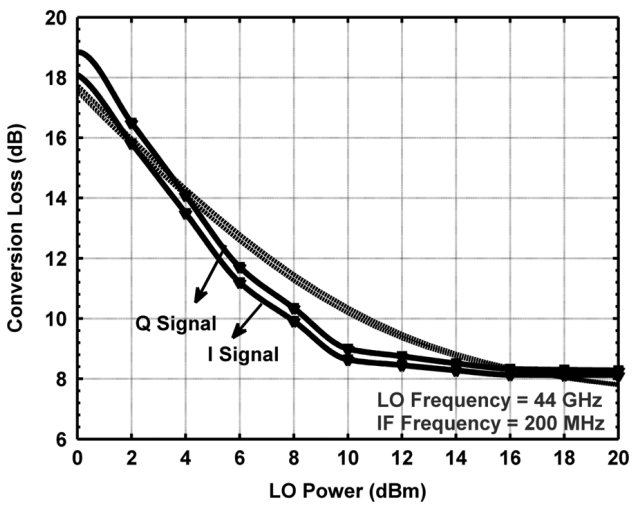


Fig. 14. Measured (solid) and simulated (dashed) conversion loss versus LO power.

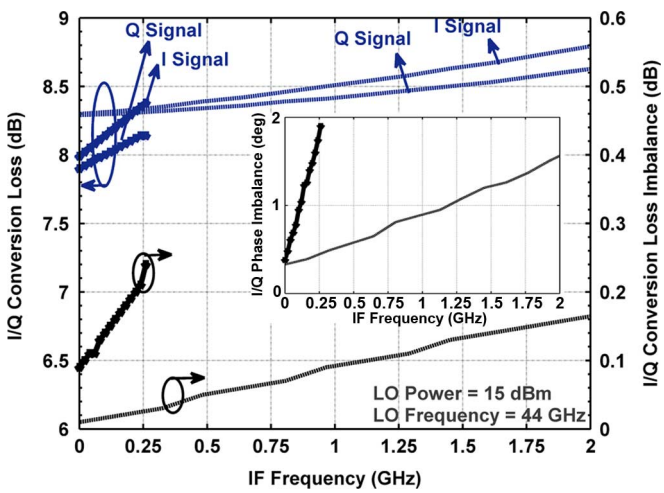


Fig. 15. Measured (solid) and simulated (dashed) conversion loss and gain and phase imbalance with fixed LO frequency.

Agilent E8257D signal generators. The RF signal at the Q-band is downconverted to an I/Q IF with a maximum bandwidth

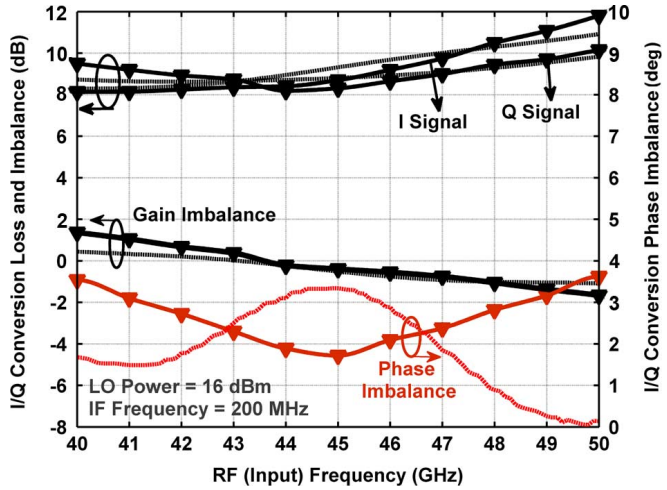


Fig. 16. Measured (solid) and simulated (dashed) conversion gain/phase imbalance of the mixer with fixed IF frequency of 200 MHz.

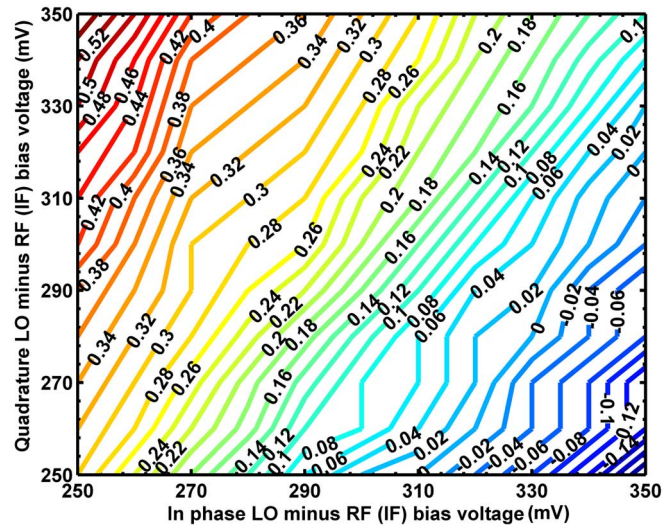


Fig. 17. Measured conversion loss I/Q mismatch contours with independent in-phase dc biases, $V_{\mathrm{BIAS\text{-}LO,RF,IF}}$, and quadrature dc biases, $V_{\mathrm{BIAS\text{-}LO,RF,IF}}$.

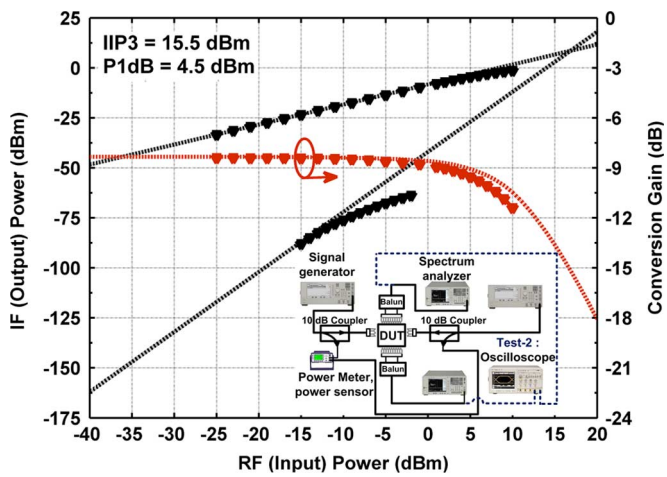


Fig. 18. Measured (solid) and simulated (dashed) input–output power characteristics and associated setup.

of 250 MHz via the LO quadrature signals generated by the polyphase filter and the quadrature mixers. An off-chip balun is used to combine the IF differential signals.

TABLE I
COMPARISON TO REPORTED MIXERS

Ref.	Tech.	Topology	LO Power (dBm)	Bandwidth (GHz)	Conversion Gain (dB)	LO-RF Isolation (dB)	LO-IF Isolation (dB)	Input P1dB (dBm)
[2]	90nm CMOS	Drain-pumped	7.5	30-40	-4.6	11	45	-6
[3]	90nm CMOS	Gate-pumped	0	26.5-30	-10.3	24	22	2.7
[12]	130nm CMOS	Resistive ring	10	15-50	-15.5 ± 1.5	> 35	>40	5-10
[13]	130nm CMOS	Passive distributed drain	10	0.8-77.5	-5.5 ± 1	>10	N/A	-4 @ 20GHz
[14]	180nm SiGe	Single-balanced	3	22-39	> -10	15-40	40-60	-1.5
[15]	150nm GaAs pHEMT	Resistive Star	7	25-55	-11± 2	>25	>30	5 @ 30 GHz
[16]	150nm GaAs HEMT	Diode	12.5	46-78	-9 ± 1	>20	N/A	N/A
[17]	130nm CMOS	Diode	11	16-46	-13 ± 1.5	>20	>37	4
This work	45nm SOI CMOS	I/Q Resistive ring	15	40-50	-8.35	>49	N/A	4.5 @ 45 GHz

The measured and simulated return losses of the LO and RF ports are shown in Fig. 13. External pads for the dc biasing of LO, RF, and IF ports are placed on chip to alter the matching of the RF and LO ports, if necessary. Fig. 13 shows the return losses when $V_{\mathrm{BIAS\text{-}LO}}$ and $V_{\mathrm{BIAS\text{-}RF}}(V_{\mathrm{BIAS\text{-}IF}})$ are 300 mV and 0 V, respectively. The bias is altered to improve the RF return loss. The RF matching gets better and LO matching remains unchanged when $V_{\mathrm{BIAS\text{-}LO}}$ and $V_{\mathrm{BIAS\text{-}RF}}(V_{\mathrm{BIAS\text{-}IF}})$ are altered to 650 and 300 mV, respectively as shown in Fig. 13. Fig. 13 also shows the sensitivity of the return losses to the LO and RF/IF bias voltages. The measured return loss of the RF and LO port is better than 14 and 32 dB at 45 GHz.

The simulation and measurement of conversion gain versus LO input power is presented in Fig. 14. Measurement and simulations show that LO power of 10 dBm is sufficient to achieve within 1 dB of the minimum conversion loss. As illustrated in Fig. 15, when the LO frequency is fixed at 43.4 GHz, the conversion gain versus IF frequency is measured while the RF frequency is varied from 43.4 to 43.65 GHz. Measurement and simulations show that the gain and phase imbalance increases when the IF frequency is increased.

To determine the gain and phase imbalance, the IF frequency is fixed at 200 MHz and the RF frequency is varied from 40 to 50 GHz and LO frequency is varied from 39.8 to 49.8 GHz as both the I and the Q signals are down-converted. The conversion gain and gain/phase mismatch of the I/Q path is shown in Fig. 16. The I/Q balance is measured by comparing the IF using the Agilent DSO80604B oscilloscope. The minimum conversion loss of one channel is 8.35 dB when the LO and RF frequency is fixed at 43.4 and 43.6 GHz. The minimum gain and phase imbalance of 0 dB and 2° occurs at 43.5 and 45 GHz, respectively.

Small gain and phase imbalances are compensated by independently altering the ten dc voltage biases of the I and Q mixers without significant impact on the conversion gain of the mixer. Fig. 17 shows that zero gain imbalance occurs when the difference in the dc bias across the LO and RF (IF) ports of the I and Q mixers is set to 0.35 and 0.31 V, respectively. However, phase imbalance degrades and further optimization provides the minimum I/Q gain and phase imbalance at the same time and is found as 0.25 dB and 1.9°, respectively.

As shown in Fig. 18, the power-handling capability was measured using an Agilent E8257D signal source, an Agilent V8486A V-band power sensor, and the results are also confirmed with the Agilent E4448A spectrum analyzer.

The RF and LO frequency are 43.3 and 43.1 GHz, respectively. The mixer results in a gain compression point (P1 dB) of 4.5 dBm at 43.3 GHz, as shown in Fig. 18. Finally, the third-order intermodulation products are measured at two tones at 43.20 and 43.22 GHz (spaced by 20 MHz). The extrapolated intermodulation intercept point (IIP3) is $+15.5$ dBm, as illustrated in Fig. 18(b).

The isolation between the ports LO-RF and RF-LO is simulated and measured. LO suppression at RF (LO-RF isolation) is simulated and measured as 66.5 and 49 dB, respectively. The measured port-to-port isolation at LO port for the RF feedthrough is better than 65 dB at the center frequency of 44 GHz. The LO-IF and RF-IF isolation is not measured due to the probe limitations mentioned before. The LO-IF and RF-IF isolation is simulated and found as 68 and 48 dB, respectively.

Table I presents a comparison of reported millimeter-wave mixers. Most prior work does not provide results discussing gain and phase mismatch. In this table, wideband performance mixers are presented by [12] and [13]. Reference [13] provides very wide operation bandwidth and good conversion efficiency; however, LO-RF isolation is poor due to the distributed structure of the mixer. Good performance passive mixers in SOI is demonstrated in [2] and [3]. A compact mixer compared to the previously reported star mixers, which is due to the novel balun structures, is proposed in [15]–[17]. This design is the first millimeter-wave I/Q passive mixer in SOI and offers very low insertion loss and high LO-RF isolation at satellite bands.

V. CONCLUSIONS

This paper has demonstrated the design and state-of-the-art measurement results of the balanced resistive ring mixer and SPDT switch in 45-nm SOI CMOS. The technology provides the substrate isolation; therefore, 45-nm CMOS is an excellent candidate for millimeter-wave passive circuits: SPDT switches and ring mixers. EM simulations were extensively used to model the high-frequency behavior of any passive components

such as the conventional CPW line, grounded stubs, inductors, and baluns.

The passive resistive I/Q ring mixer demonstrates a conversion loss of 8.35 dB and input $P_{1\ \mathrm{dB}}$ of 4.5 dBm at 43.3 GHz. The gain and phase imbalance is minimized using the provided dc pads and is 0.25 dB and 1.9°, respectively. The record SPDT insertion loss is 1.7 dB at 45 GHz and less than 2.5 dB at 60 GHz with an isolation of greater than 25 dB at 45 GHz. The input $P_{1\ \mathrm{dB}}$ of the switch is 7.1 dBm.

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