

A Low Power and High Gain Double-Balanced Active Mixer with Integrated Transformer-Based Baluns dedicated to 77 GHz Automotive Radar Applications

A. Mariano, B. Leite, C. Majek, T. Taris, Y. Deval,
J-B. Bégueret
IC Design Team – IMS Laboratory
University of Bordeaux
Bordeaux – France
andre.mariano@ims-bordeaux.fr

D. Belot
Innovation & Collaborative Research
STMicroelectronics
Crolles, France

Abstract— In this paper, we present a low power and high gain mixer dedicated to 77 GHz automotive radar applications. The architecture is based on a double-balanced active Gilbert cell with integrated transformer-based Baluns. These Baluns allow converting the single-ended input signals to differential with an amplitude and phase imbalance of 0.3 dB and 179°, respectively. Interconnections between devices, capacitor accesses and Tee-junctions are modeled using HFSS simulator in order to improve the simulation accuracy. The proposed mixer consumes 105 mW and achieves 16.4 dB of conversion gain and 13.2 dB of noise figure.

I. INTRODUCTION

The rapid development of microwave communication systems has led to a great effort on the design of low-cost radar sensors for the automotive industry. Hence silicon-based technologies, like 130 nm BiCMOS, challenge III-V devices in term of high frequency performances thus allowing low-cost implementation of millimeter-waves (mmW) systems [1-2].

Among the most critical building-blocks in a Front-End receiver is the mixer. It performs frequency down-conversion from the radio-frequencies (RF) to the intermediate-frequencies (IF). This operation alleviates the specifications of the receiver back-end and enables the analog-to-digital conversion at low frequencies. The linearity is a major of importance in mixers since the frequency shift is a typical non-linear operation [3]. To help in lowering noise figure (NF) of the system, the multiplier, located after the Low-Noise Amplifier (LNA), also needs to achieve gain and a suitable NF.

After describing the design flow of a fully balanced Gilbert cell, this work focuses on its high-frequency implementation. First, the Tee-junctions and cross-sections are modeled by 3D

electromagnetic (EM) simulations. This step implies transistors resizing. Then the design of Baluns, converting single to differential signals, are investigated with HFSS [4]. At last, the performances of the mixer, implemented in a 130 nm BiCMOS technology, are discussed.

II. MIXER TOPOLOGY

Figure 1 depicts the block diagram of the proposed mixer. It consists of a double-balanced active mixer topology (Gilbert cell) [5]. Two Baluns are implemented in order to convert the single-ended input to differential. The high-frequency application of the mixer results in merging conventional RF circuit design with microwave 3D electromagnetic simulations. A great interaction between electrical and electromagnetic simulations is required in order to optimize transistors sizing and EM coupling. These design considerations are presented in the remaining of this paper.

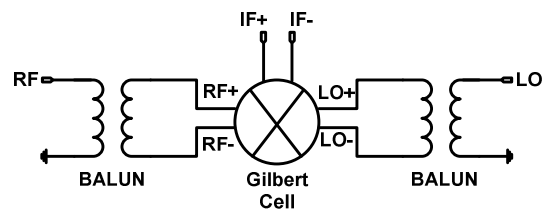


Figure 1. Block diagram of the proposed double-balanced active mixer

A. Circuit Design

The schematic of the double-balanced active mixer is presented in Figure 2. It is based on the Gilbert cell which operates as it follows: a transconductor stage (T_1 and T_2) converting the input RF voltage into current and a switching

stage ($T_3 - T_6$), which commutates the RF current between the two output branches. The double-balanced topology presents advantages compared to the single-balanced one, such as increased linearity, better suppression of spurious products, high intercept point, good supply voltage rejection and better IF output isolation from LO and RF inputs [6-8]. In the Figure 2, transmission lines ("TL"), Tee-junctions ("T") and crossing points ("X") are presented. Designing at mmW frequencies requires the modeling of all interconnections and accesses to devices (transistors, capacitors, resistors, etc.). More details about this modeling are given in Section III.

As mentioned before, the linearity of the mixer strongly contributes to the system performance. To further improve the linearity, the emitter is degenerated by transmission line TL_3 .

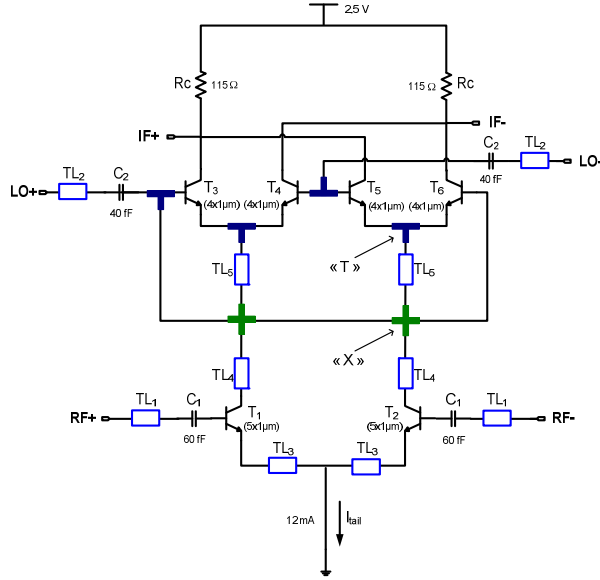


Figure 2. Double-balanced mixer topology

The maximum the f_T is the higher the gain is. Unfortunately the current density performing the best f_T does not correspond with the minimum NF. Hence, the sizing of T_1 and T_2 is led by the optimal current density for a large gain at the expense of noise figure.

The conversion gain (CG) of the Gilbert cell can be expressed as follows:

$$CG = \frac{2}{\pi} \cdot g_{m1/2} \cdot R_c \quad (1)$$

From (1), it comes the larger the I_{tail} current and R_c are the higher the CG is. I_{tail} is here fixed to 12mA and R_c 115 Ohms. The trouble nodes in a fully balanced mixer are the connecting points between the transconductor stage and switching stage. Indeed, the parasitics, here located, contribute to lower both the isolation between LO and RF ports and the CG. To overcome this bottleneck, TL_4 and TL_5 are introduced, Figure 2, resonating with the local parasitic capacitors.

If we consider that the switching is almost perfect which means $T_3 - T_6$ are as small as possible, the NF is mainly supported by the transconductor stage. To reduce the NF, the base-emitter area as well as the number of fingers are set very large. The input matching of RF and LO ports are performed by the AC coupling capacitors, C_1 and C_2 , combined with the TL_1 and TL_2 , respectively.

III. MIXER IMPLEMENTATION

Operating at 80 GHz, the wavelength of the signal, a roughly 1 mm, is in the range of the circuit size. As a matter of consequence, interconnections and metal path rather behave like distributed devices than mere RC type elements. EM simulations are so required to characterize them. The chosen simulator is Ansoft HFSS [4], a finite element based 3D field calculator.

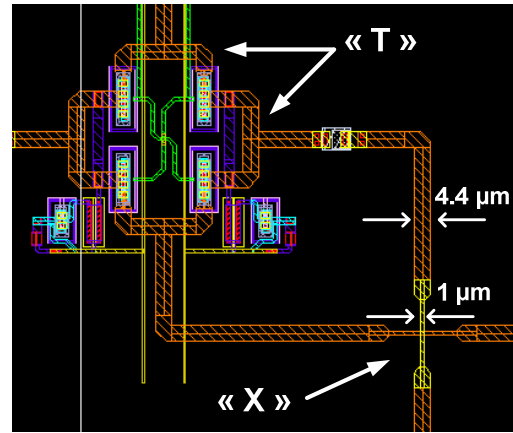


Figure 3. Layout close-up of the double-balanced mixer, highlighting the Tee-junction ("T") and crossing point ("X")

A. Gilbert cell layout and cores

In the Figure 4, a close-up of the mixer core is depicted. The capacitors accesses and straight connections are modeled with TJs from the design kit (DK). The active devices are extracted up to metal 6. In order to keep good balance and LO to RF isolation, a specific investigation has been led at the points "T" and "X" (Figures 2 and 4). The Tee-junction "T" and crossing-point "X" had been characterized according to the models presented in Figure 5.

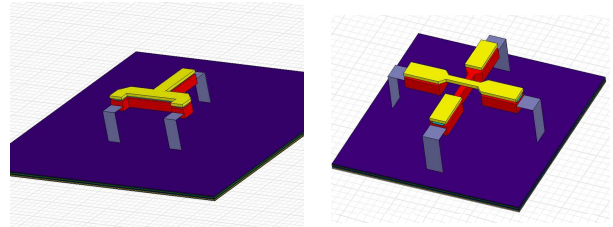


Figure 4. HFSS simulation models for Tee-junction and crossing point

These 3D elements are generated from the 2D layout of CADENCE. A simplified back-end of the 130 nm BiCMOS technology is detailed in HFSS in order to perform accurate

simulations with reasonable time computing. The main advantage of using 3D simulations is the possibility to choose the best geometry and the best metal layer for a given path in the layout. This allows minimizing coupling effects and improving the accuracy of the simulation. Let us consider the example of a crossing point. The LO and RF paths intersect at “X” (Figure 4), due to the cross-coupled connections between the transistors ($T_3 - T_6$) in the switching stage. A strong coupling is observed, lessening the isolation between LO and RF ports. Modeling this intersection with HFSS, one can demonstrate that reducing the width of these paths at the crossing point allows minimizing the coupling effect. Figure 6 depicts the simulation results for three different path widths. Note that the port-to-port isolation is improved by more than 10 dB when the path width decreases from $4.4\ \mu\text{m}$ to $1\ \mu\text{m}$. In the proposed mixer, paths with $1\ \mu\text{m}$ width are implemented in the intersect points.

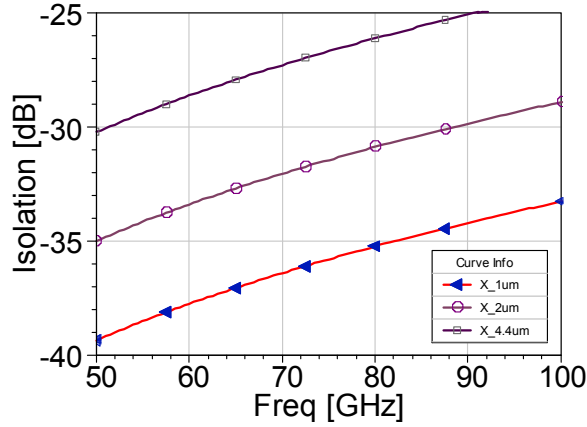


Figure 5. Isolation between RF and LO paths at crossing point as a function of path width

B. Balun Realization

Usually, single-ended to differential conversion at mmW frequencies is performed using coupler or distributed structures. However, these solutions are silicon-consuming and narrow band. Another approach consists in employing transformer-based baluns [9]. Such components are capable of providing a good phase and amplitude balance over a broad band, whereas it accepts a moderate silicon area.

The Balun, presented in Figure 7, has been implemented with the two top thick metal layers. Primary and secondary access lines are located on opposite sides of the transformer (*flipped* topology) and the primary is center-tapped. Each winding exhibits a single octagonal turn with an average diameter of $70\ \mu\text{m}$ and a trace width of $4.4\ \mu\text{m}$.

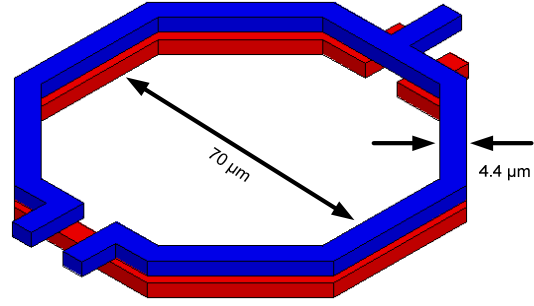


Figure 6. HFSS simulation model for the transformer-based Balun

The stacked topology as well as the octagonal shape of the balun were selected since they are low loss compared to interleaved and square transformers [10]. The conductors width and the flipped topology, on the other hand, were adopted to match the mixer layout. The diameter of the coils is optimized to yield the best trade-off between insertion loss and phase / amplitude balance.

At 77 GHz, Figure 8, the amplitude and phase imbalance are 0.30 dB and 179° respectively. Furthermore, a low variation is observed over a 50 to 100 GHz range, reaching less than 0.6 dB and 3° . This wideband behavior is a typical skill of transformer-based Balun. The insertion loss is estimated to 5.5 dB at 77 GHz.

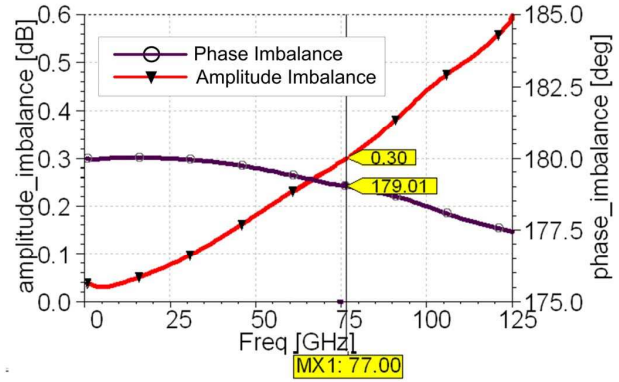


Figure 7. Phase and amplitude imbalance simulation results

IV. SIMULATION RESULTS AND DISCUSSIONS

The full layout of the double-balanced active mixer, including the transformer-based Baluns, is presented in Figure 9. It takes place in a $0.57\ \text{mm}^2$. All transmission lines are laid-out as symmetric as possible in order to preserve the differential operation of the mixer. Decoupling capacitors are placed as near as possible to the more critical blocks.

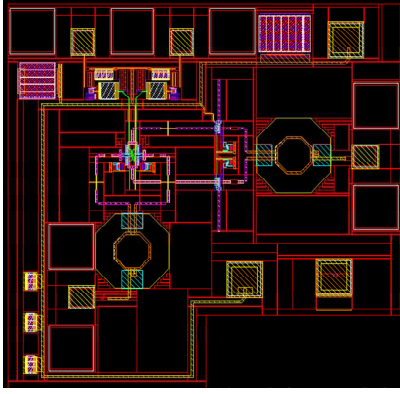


Figure 8. Layout of the double balanced mixer

Figure 10 depicts the simulation results for the RF and LO input matching. The wideband performance is mainly supported by the transformer-based Baluns.

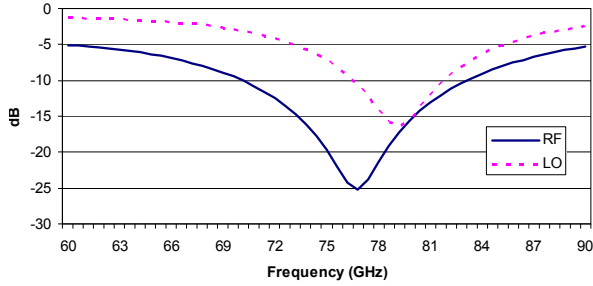


Figure 9. RF and LO input matching

The conversion gain and noise figure are presented in Figure 11. As the transformer-based Baluns are used for measurements purpose, the insertion loss is deembedded in the reported results. The mixer achieves a CG of 16.4 dB, a NF_{SSB} of 13.2 dB and an ICP1 of -9 dBm, consuming 105 mW under 2.5V.

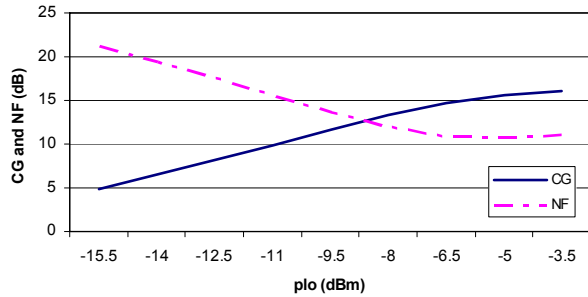


Figure 10. Conversion gain and NF_{SSB} as a function of LO power ($f_{RF} = 77$ GHz and $f_{LO} = 80$ GHz)

The mixer is designed for a high gain and low power consumption, at the expense of fair NF and linearity. Notice that, Figure 11, both CG and NF varies with the LO input power. Within the 77 to 80 GHz range, the output power of

signal generators is a primordial drawback. For this reason, the proposed mixer achieves its best values for CG and NF at an acceptable LO input power of -5 dBm. Beyond this value, CG and NF start reaching the saturation.

V. CONCLUSION

A low power and high conversion gain double-balanced active mixer is presented. Transformer-based Baluns have been implemented on-chip in order to convert the single-ended inputs to differential. The amplitude imbalance between the ports over a wideband of 125 GHz is not superior to 0.6 dB and the phase does not deviate more than 3.5 degrees from 180°. The application of 3D models allows evaluating the impact of the layout interconnections over the mixer performances, resulting in more accurate simulations. The proposed mixer presents a good trade-off between gain, noise figure and power consumption. It reaches a conversion gain and noise figure of, respectively, 16.4 dB and 13.2 dB, while consuming only 105 mW under 2.5V.

ACKNOWLEDGMENT

The authors would like to thank European authorities supporting SIAM project and STMicroelectronics for technology support.

REFERENCES

- [1] S. Voinigescu *et al.*, "Comparison of Silicon and III-V Technology Performance and Building Block Implementations for 10 and 40 Gb/s Optical Networking ICs", in *Journal of High Speed Electronics and Systems*, vol. 13, no. 1, pp. 27-57, Mar. 2003.
- [2] P. Chevalier, et al, "High-Speed SiGe BiCMOS Technologies:120-nm Status and End-of-Roadmap Challenges," *IEEE SiRF*, pp. 18-23, Jan. 2007.
- [3] Trotta, S., Dehlink, B., Knapp, H., Aufinger, K., Meister, T.F., Bock, J., Simburger, W., Scholtz, A.L., "Design considerations for low-noise, highly-linear millimeter-wave mixers in SiGe bipolar technology", *ESSCIRC 07*, pp. 356 – 359, Sept. 2007.
- [4] R. Ansoft Corporation. High frequency structure simulator HFSS, version 11, 2007.
- [5] B. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *IEEE Journal of Solid State Circuits*, vol. SC-3, N4, pp. 365-373, December 1968.
- [6] W. Perndl, H. Knapp, M. Wurzer, K. Aufinger, T. Meister, J. Böck, W. Simbürger, and A. L. Scholtz, "A low-noise and high-gain doublebalanced mixer for 77 GHz automotive radar front-ends in SiGe bipolar technology," *IEEE RFIC Digest*, pp. 47–50, June 2004.
- [7] B. Dehlink, H.-D. Wohlmuth, H. Forstner, H. Knapp, S. Trotta, K. Aufinger, T. Meister, J. Böck, and A. L. Scholtz, "A highly-linear SiGe double-balanced mixer for 77 GHz automotive radar applications," *IEEE RFIC Digest*, pp. 235–238, June 2006.
- [8] L. Wang, R. Kraemer, and J. Borngräber, "An improved highly-linear low-power down-conversion micromixer for 77 GHz automotive radar in SiGe technology," *IEEE MTT-s Digest*, pp. 1834–1837, June 2006.
- [9] T. O. Dickson, M. A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 123–133, Jan. 2005.
- [10] B. Leite, E. Kerherve, J. B. Begueret, and D. Belot, "Transformer topologies for mmW integrated circuits," in *European Microwave Conference*, September 2009.