4.1 A Blocker-Tolerant Wideband Noise-Cancelling Receiver with a 2dB Noise Figure

David Murphy[1,2], Amr Hafez[1,2], Ahmad Mirzaei[2], Mohyee Mikhemar[2], Hooman Darabi[2], Mau-Chung Frank Chang[1], Asad Abidi[1]

[1]University of California, Los Angeles, Los Angeles, CA
[2]Broadcom, Irvine, CA

As narrowband off-chip RF filtering is not compatible with the concept of software-defined radio (SDR), an SDR receiver must be designed to tolerate large out-of-band blockers with minimal gain compression and noise figure degradation. A recent circuit [1] tackles this problem by dispensing with the LNA entirely. This *mixer-first* approach achieves impressive linearity, but at the expense of noise figure and, since such a receiver has no gain prior to down-conversion, the flicker noise corner can be unacceptably high. Other SDR attempts invariably use a noise-cancelling LNA at the front end, which provides wideband matching, however such approaches have either inadequate linearity [2] or display too large a noise for our purposes [3]. In this work, we propose a hybrid *frequency-translational, noise-cancelling* (FTNC) receiver that employs two separate down-conversion paths to enable noise cancelling *with no voltage gain prior to baseband filtering*. The resulting design has a sub-2dB noise figure and tolerates 0dBm blockers with no gain back-off, breaking the traditional noise-linearity trade-off common in all receivers.

Noise-cancelling as applied to LNAs [4] is a straightforward idea: The noise originating from a 50Ω impedance-matching resistor at the input of a wideband receiver can be cancelled by measuring the current in that resistor and the voltage at the input port, as shown in Fig. 4.1.1a. While the resistor's noise is cancelled using two gain paths, the wanted signal appears in phase and is reinforced. Our approach exploits this concept, but avoids voltage gain entirely by using two separate downconversion paths, as shown in Fig. 4.1.1b. The main path provides *impedance matching* and the *current measurement*, while the *auxiliary* path provides a measure of the *voltage* at the RF input. By employing passive mixers and high-gain baseband operational amplifiers, the virtual ground appears ideally at the RF side of the mixers and suppresses voltage swing prior to baseband filtering. Thus, without sacrificing noise figure, the system can be considered *blocker-tolerant*. Since passive mixers are reciprocal, the noise of the op-amp in the main path upconverts at the receiver input to RF, but it is cancelled along with the noise contribution of R_{IN} and the series resistance of the passive mixer. The noise of the auxiliary op-amp contributes negligibly when driven by a current-source like G_M cell, and large feedback resistors across the post-mixer transimpedance amplifiers (TIA) contribute little noise of their own. Therefore, the G_M cell, which does *not* need to provide matching, determines the receiver noise figure. This enables us to employ a very simple G_M such as an inverter, which in addition to being wideband has far better linearity than a typical matched common-source LNA.

Figure 4.1.2 shows the complete schematic of the receiver. A 50Ω match is provided by a combination of the series resistance of the passive mixer switches and the upconverted input impedance of the main-path TIAs. The TIAs use a single-pole inverter-based amplifier to boost large-signal linearity and maximize g_m/I_D. In the auxiliary path, the RF G_M cell is realized using an inverter as well. A scaled replica of this inverter with the input and output shorted is used to bias the entire receiver, which ensures that no DC current flows through the mixer switches and, so, eliminates the need for large decoupling capacitors at the inputs of the passive mixers. A low impedance (≈10Ω) at the input terminal of the auxiliary passive mixer suppresses voltage swing at the output of the G_M cell. By limiting the output swing, and by setting the common mode at half V_{DD}, the G_M cell is able to tolerate an input swing of 0dBm without excessive gain compression.

Downconversion is achieved using eight-phase passive mixers that are driven with non-overlapping 12.5% duty-cycle clocks. Eight-phase mixers are used for two reasons: First, by using appropriately weighted combinations of the TIA outputs, the I/Q components of the wanted signal around the LO frequency (F_{LO}) can be generated, while all folding terms up to $7*F_{LO}$ are nulled. By comparison, the 4-phase mixer used in [3] results in unwanted downconversion of signals around the 3rd and 5th harmonic of F_{LO}, which is unacceptable for a true SDR. Secondly, by increasing the number of mixer phases, the amount of noise that folds down from higher-order harmonics is also reduced, improving noise figure.

In addition to cost implications and degraded noise figure, a *wideband external balun* as required in [3] is simply not practical for an SDR. Our design does not require a balun, however, its single-ended nature does complicate the design of the LO: When single-ended passive mixers are employed, any uncorrelated noise between differential LO signals can couple onto the signal path and corrupt the noise figure. For this reason the shift-register-based divider shown in Fig. 4.1.3 was used. This divider re-times each clock pulse and limits the amount of significant uncorrelated differential noise to the contribution of the highlighted NMOS transistor.

Unlike the standard noise-cancelling LNA, the proposed receiver can correct for phase and amplitude mismatch between the two paths. Amplitude mismatch is corrected by varying the feedback resistors of the auxiliary TIAs, whereas changing the weighting of the G_M blocks in the harmonic recombination circuitry can correct for both phase and gain. Around the optimum point, however, noise cancelling is quite robust, and measurements show that varying auxiliary phase by ±20° or gain by ±20% results in less than 0.3dB degradation in NF.

A test chip was fabricated in 40nm CMOS. The divider was functional from 80MHz to 2.7GHz, and an S_{11} of around -10dB was observed across the band. As shown in Fig. 4.1.4, the noise figure was measured at or below 2dB across most of the band. When the auxiliary path is powered down, the receiver becomes a mixer-first receiver and the noise figure degrades. Interestingly, in the mixer-first configuration, a large flicker noise corner is observed due to the main path TIAs. When the auxiliary path is enabled, however, this noise is upconverted to RF and then cancelled, causing the 1/f noise corner to drop from 100kHz to below 20kHz. As shown in Fig. 4.1.5, at maximum gain, a 0dBm blocker located at 80MHz from the carrier degrades the noise figure to 4.1dB; this degradation is mainly due to gain compression (~1.6dB), while reciprocal mixing of the blocker with the divider phase noise plays a lesser role, thanks to the divider retiming. Out-of-band IIP3 was measured at +13.5dBm, and *un-calibrated* out-of-band IIP2 was better than +54dBm, all at maximum gain. The LO path consumes 3 to 36 mA, the RF G_M cell draws 8mA, and the baseband circuits consume 16mA. The entire receiver occupies an active area of 1.2mm^2. The die micrograph is shown in Fig. 4.1.7.

The FTNC RX can also be realized as a fully differential circuit and, in fact, we have verified such a design on silicon. That differential version has similar noise performance, but has improved common-mode rejection and IIP2 (+68dBm).

Figure 4.1.6 compares this work with other recently published blocker-tolerant receivers. Even when compared to a state-of-the-art *narrowband* receiver [5], our design improves small-signal noise figure, achieves better blocker performance, and consumes substantially less current. Finally, unlike the SDR proposed in [3], our approach achieves better small-signal and blocker noise figure, requires no external balun, and is immune to 3rd/5th harmonic folding.

References:

[1] C. Andrews and A.C. Molnar, "A passive-mixer-first receiver with baseband-controlled RF impedance matching, < 6dB NF, and > 27dBm wideband IIP3," *ISSCC Dig. Tech. Papers,* pp. 46-47, Feb 2010.
[2] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, M. Tang, and A. Abidi, "An 800MHz-to-5GHz Software-Defined Radio Receiver in 90nm CMOS," *ISSCC Dig. Tech. Papers,* pp. 1932-1941, Feb. 2006.
[3] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40nm CMOS highly linear 0.4-to-6GHz receiver resilient to 0dBm out-of-band blockers," *ISSCC Dig. Tech. Papers*, pp. 62-64, Feb 2011.
[4] F. Bruccoleri et al., "Noise cancelling in wideband CMOS LNAs," *ISSCC Dig. Tech. Papers*, pp. 406-407, Feb 2002.
[5] I.S.-C Lu, Chi-yao Yu, Yen-horng Chen, Lan-chou Cho, C.-h.E. Sun, Chih-Chun Tang, and G. Chien , "A SAW-less GSM/GPRS/EDGE receiver embedded in a 65nm CMOS SoC," *ISSCC Dig. Tech. Papers*, pp.364-366, Feb 2011.

 978-1-4673-0377-4/12/$31.00

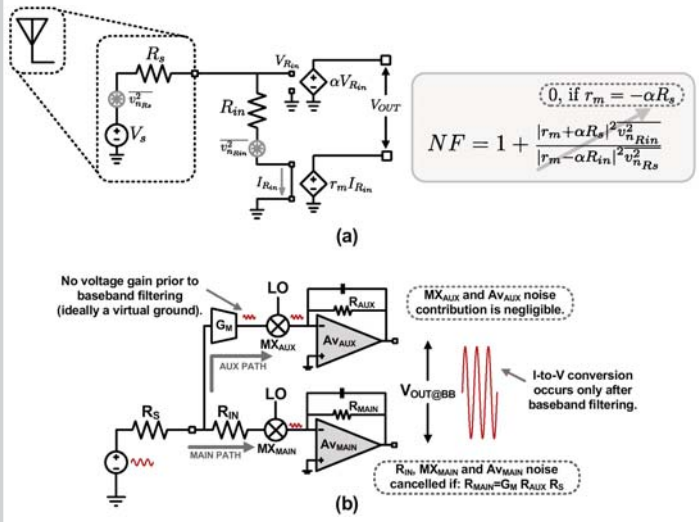

Figure 4.1.1: Noise Cancelling: (a) basic concept (b) the proposed noise-cancelling receiver.

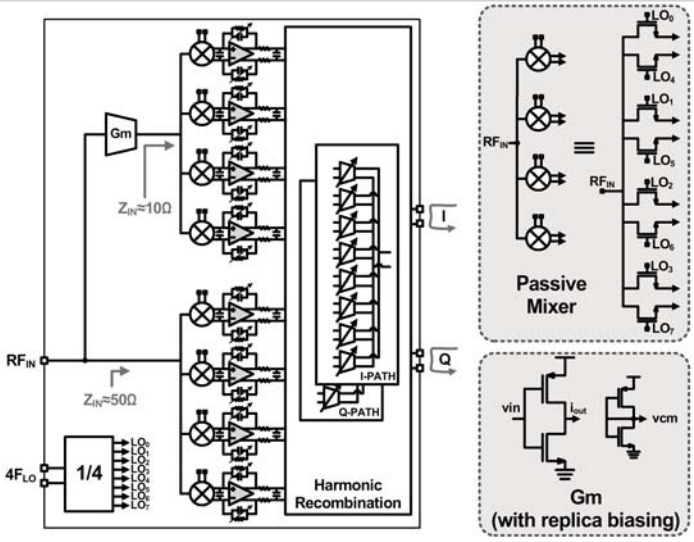

Figure 4.1.2: The complete Frequency-Translational, Noise Cancelling (FTNC) receiver.

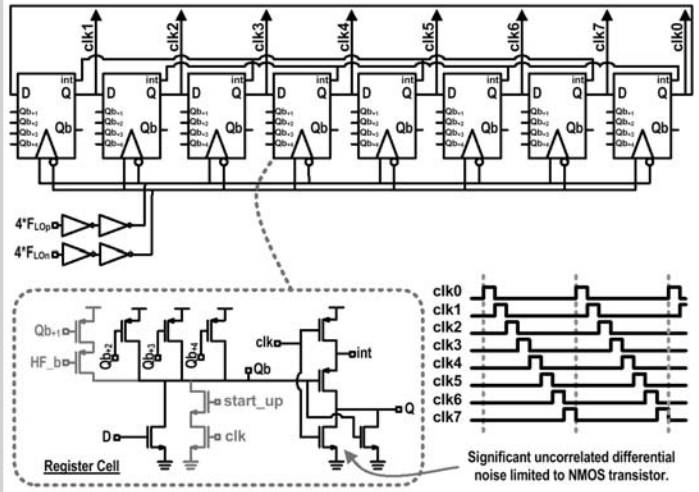

Figure 4.1.3: Eight-phase LO generation circuitry.

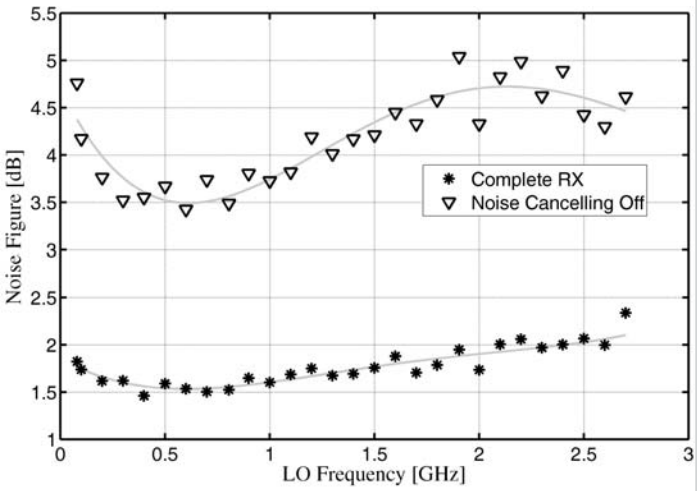

Figure 4.1.4: Measured noise figure.

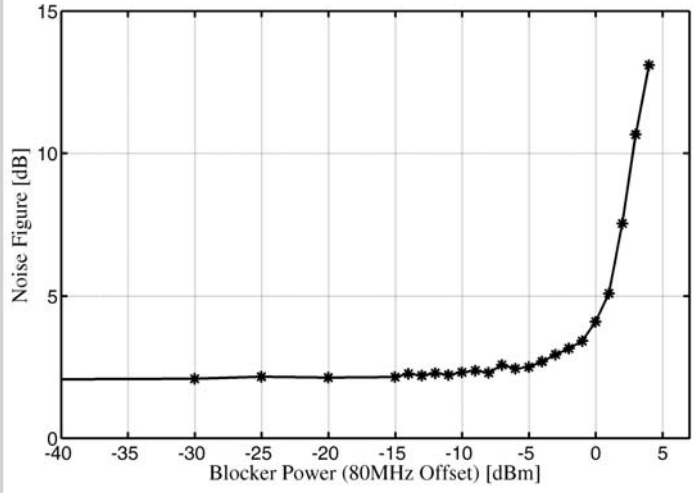

Figure 4.1.5: Measured blocker noise figure.

	[1]	[3]	[5]	This work
Architecture	Mixer-first	NC-LNA & voltage mixer	Saw-less narrowband	FTNC RX
RF Frequency [MHz]	100-2400	400-6000	850/900/ 1800/1900	80-2700
RF Input	Single-ended	Differential	Differential	Single-ended
Gain [dB]	40-70	70	60	70
NF @2GHz [dB]	7	4.4*	4.1*	1.9
0dBm Blocker NF [dB]	-	15	7	4.1
3rd/5th Harmonic Rejection [dB]	35.4/42.6 (F_{LO}<1GHz only)	No	No	42/45
OB-IIP3 [dBm]	+25	+10	N/A	+13.5
Active Area [mm²]	2	2	1.4	1.2
Supply Voltages [V]	1.2/2.5	1.1/2.5	3.8	1.3
RX Current** [mA]	12	12	37	12
CMOS Technology	65nm	40nm	65nm	40nm

* Includes assumed 1.2dB balun loss

**Estimated Battery Current, where $I_{BATTERY} \approx I_{SUPPLY>1.5V} + 0.5*I_{SUPPLY<1.5V}$

Figure 4.1.6: Comparison with recently published blocker-tolerant receivers.

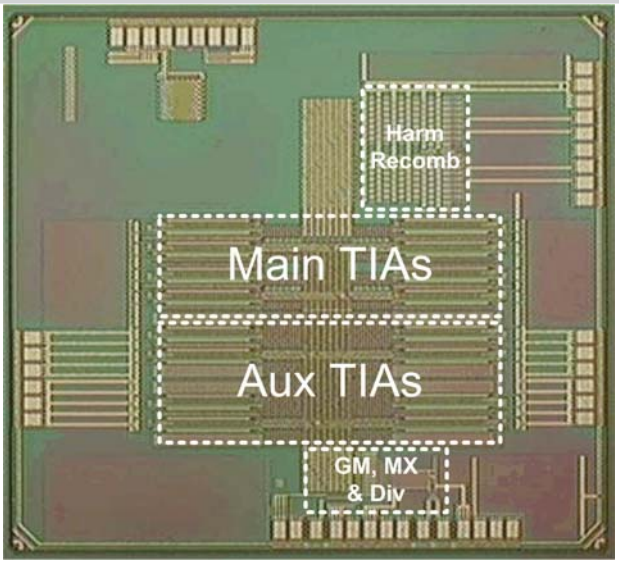

Figure 4.1.7: Die photograph.

978-1-4673-0377-4/12/$31.00