A 77 GHz Low LO Power Mixer With a Split Self-Driven Switching Cell in 65 nm CMOS Technology

Seong-Kyun Kim, Chenglin Cui, *Student Member, IEEE*, Guochi Huang, SoYoung Kim, and Byung-Sung Kim, *Member, IEEE*

***Abstract*—A low LO power mixer with high gain by using a split self-driven switching cell for automotive applications at 77 GHz is presented. By splitting the switching cell, the required LO power is reduced and the VCO has less capacitive loading. The mixer has a peak conversion gain of 6.8 dB and the input 1 dB compression point is −7 dBm at LO power of −5 dBm. The chip is fabricated in 65 nm CMOS technology and the chip size including a Marchand balun is 790 μm × 590 μm. The total power consumption is 3 mW from a 1.2 V supply.**

***Index Terms*—Automotive radar, CMOS integrated circuit, mixers, phased-array, 77 GHz down-converter.**

I. Introduction

THE continued development of CMOS technology enables the applications to expand into mm-wave frequencies such as 60 GHz wireless systems and 77 GHz automotive radar systems. Recently, to improve the sensitivity of mm-wave systems, many applications adopt the phased-array systems. Automotive industries also expect the phased-array 77 GHz long-range radar for adaptive cruise control (ACC) system. To configure the phased-array system, several receiving channels are essential, which are composed of many low-noise amplifiers (LNAs) and mixers with a common local oscillator (LO). In CMOS mm-wave design, the active switching mixer is widely used [1], [2], but it requires high LO power to turn on/off the switching cell abruptly to get high gain and low noise figure. However, it is difficult to get high LO power at mm-wave frequency. Furthermore, since the LO buffer of the phased-array system should drive multiple mixers, it requires very high-power due to heavy capacitive loading of several switching pairs. Even though high LO power can be obtained by inserting amplifying stages into LO distribution network, it requires high power consumption because of the poor efficiency in the mm-wave range. Instead of the switching mixer, single-gate or dual-gate FET nonlinear mixers can be used for mm-wave application at moderate LO power. But, they show a low conversion gain, poor LO-to-RF isolation and require an additional large sized hybrid (see Table I) [3], [4], [11], [12].

Manuscript received July 11, 2012; accepted August 01, 2012. Date of publication August 22, 2012; date of current version August 30, 2012. This work was supported by Mid-career Researcher Program and Basic Science Research Program through NRF Grant funded by the MEST (No. 2009–0086266, 2010–0001960), MKE/ETRI, SW-SoC R&BD Center provided funding for the research work, and the chip fabrication and CAD tools in this work were supported by IDEC.

S.-K. Kim, C. Cui, S. Kim, and B.-S. Kim are with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, Korea (e-mail: bskim@ece.skku.ac.kr).

G. Huang is with the Analog Devices, Inc., Limerick, Ireland.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2012.2213076

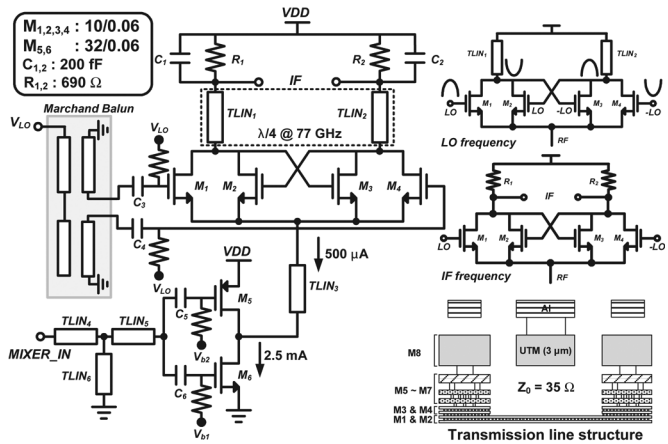

Fig. 1. Schematic of the proposed mixer.

This letter presents a 77 GHz high gain mixer with low LO power using a split self-driven switching cell. The proposed mixer can reduce the required LO power and enhance the conversion gain without additional power consumption. The details of the operating principle are explained in Section II, and experimental results are summarized in Section III. Finally, Section IV concludes this letter.

II. Circuit Design

Fig. 1 shows the schematic of the proposed mixer. The mixer employs a single-balanced topology because the intermediate frequency (IF) of FMCW radar is low enough to suppress the LO feedthrough simply by using small capacitors C_1 and C_2. The FETs M_5 and M_6 compose the transconductance stage with current bleeding through the PMOS M_5 [5]. Series transmission line matching is used between the transconductance and switching stage to improve the conversion gain of the mixer and reduce the noise contribution of the switching stage [6].

The switching stage is composed of the conventional switching pair $M_1 - M_4$ and the split cross-coupled switching pair $M_2 - M_3$. The gates of the split switching FETs M_2 and M_3 are connected to the drains of the switching FETs in the opposite side and driven by the LO feedthrough signal. Therefore, the FETs M_1 and M_2 (M_3 and M_4) are switched at the same LO phase. Especially, to boost the LO feedthrough

TABLE I
PERFORMANCE COMPARISON OF mm-WAVE MIXERS

	This work	[3]	[4]	[11]	[12]
Process	65 nm CMOS	130 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS
Type	Single-Balanced	Single-Gate	Dual-Gate	Double-Balanced	Dual-Gate
Frequency (GHz)	77	60	60	60	77
Gain (dB) @ LO power (dBm)	6.8 @ -5	-1 @ 0	-2.7 @ 0	2 @ -	5.5 @ 0
NF (dB)	21	11.5*	21.5 (18.9*)	15	-
P_{1dB}/IIP_3 (dBm)	-7 / -	-3.5 / -	-8 / -	- / -6	-
Power Consumption (mW)	3	2.4	7.2	6 (including buffers)	43.5 (including LNA)

* simulated

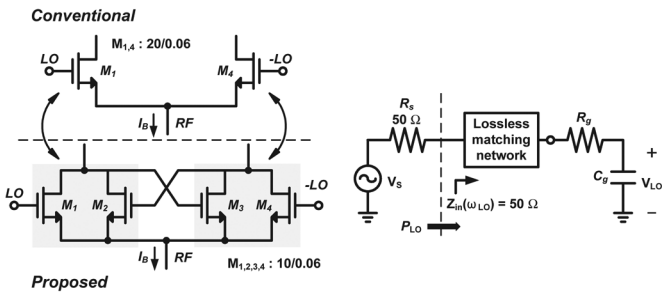

Fig. 2. (a) Split switching cells of the proposed mixer, and (b) the simplified input equivalent circuit at the LO port.

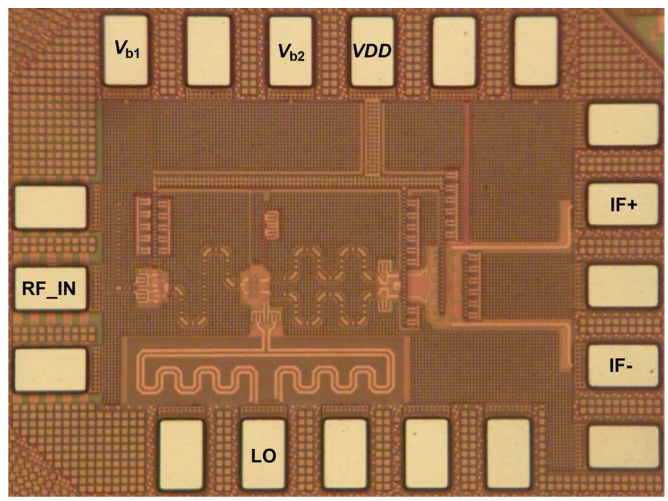

Fig. 3. Chip microphotograph.

signal at the drain nodes, approximately quarter wave length transmission lines TLIN_1 and TLIN_2 at LO frequency are inserted as loads of M_1 and M_4 and grounded by the capacitor C_1 and C_2 to prevent the LO feedthrough to the IF load R_1 and R_2. The effect of transmission line loads at IF is negligible due to the huge frequency offset between LO frequency and IF. As a result, the proposed mixer seems to reuse the LO leakage power to drive the split cross-coupled switching pair instead of simply dumping the LO feedthrough power through the bypassing capacitor in the conventional single balanced mixer.

Use of the split cross-coupled switching cell can reduce the required LO power and enhance the gain. In the conventional active switching mixer design, to achieve good gain, linearity and noise figure performance, it is necessary to optimize the bias current and the size of the switching FETs [7]. When the switching pair uses the FETs of the width W with the bias current I_{B} as shown in Fig. 2, the minimum required drive level V_{LO} at the input of the switching pair can be determined according to the complete switching condition. Then, the required LO power, P_{LO}, under the impedance matching condition at the LO port as shown in Fig. 2(b) is given [8] by

$$P_{LO} = \frac{1}{2} V_{LO}^2 \omega_{LO}^2 C_g^2 R_g \propto V_{LO}^2 \omega_{LO}^2 W \tag{1}$$

$$C_g \propto W, \quad R_g \propto \frac{1}{W} \tag{2}$$

where the $\mathrm{R_g}$ and $\mathrm{C_g}$ represent the equivalent input resistance and capacitance of the switching pair seen from the LO port. Since the $\mathrm{R_g}$ and $\mathrm{C_g}$ of the switching pair are inversely and linearly proportional to the width W of the FETs as in (2), respectively, the required LO power increases as the width of the switching FET increases.

When the total gate width and bias currents of the proposed mixer are identical to those of the conventional one, V_{LO} and current conversion ratio from RF to IF are unchanged. However, since the VCO only drives a fraction of the conventional switching FETs and the split cross coupled pair is self-driven, the required P_{LO} can be reduced according to (1). Determining the optimum ratio requires a trade-off between the LO power and the current conversion gain. If M_1 (M_4) has a larger size, reduction of the LO power is insignificant. When M_2 (M_3) has a larger size, the driving strength for the self-driven transistor M_2 (M_3) gets weaker and therefore, the gain and noise performance are degraded. Simulation results showed that the equal splitting was the best trade-off. Theoretically, splitting the conventional switching cell by half reduces the required P_{LO} by 3 dB maintaining the mixer performance. However, input impedance of the half sized device shows that the input capacitance $\mathrm{C_g}$ is reduced approximately by half, but the input resistance $\mathrm{R_g}$ does not increase as much due to the decrease of metal resistances interconnecting gate manifolds, and the fixed resistances of additional gate feed lines [9]. Therefore, the resultant reduction of the P_{LO} can be larger than 3 dB for the same V_{LO}, which is confirmed by experimental results.

In addition, introducing the split cross-coupled switching pair accompanies the enhancement of the mixer conversion gain. As shown in Fig. 1, the cross-coupled switching pair boosts the load resistance of the mixer at IF due to its negative resistance at the IF ports. Therefore, the effective load resistance is given by

$$R_{load} \approx \frac{1}{1/R_{1,2} - g_{m2,m3}} \tag{3}$$

, where $\mathrm{R}_{1,2}$ is the load resistance and $g_{\mathrm{m2,m3}}$ is the transconductance of the transistor $\mathrm{M}_{2,3}$ in Fig. 1.

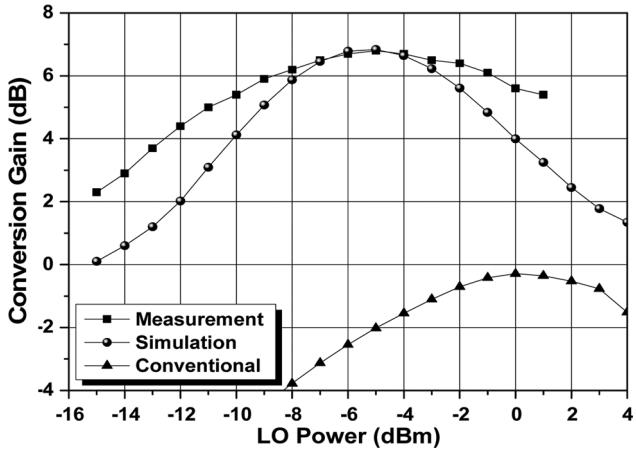

Fig. 4. Measured and simulated conversion gains versus LO power with RF of 77 GHz, IF of 1 MHz and RF input power of −30 dBm. The maximum available LO power is limited to +1 dBm in the measurement setup.

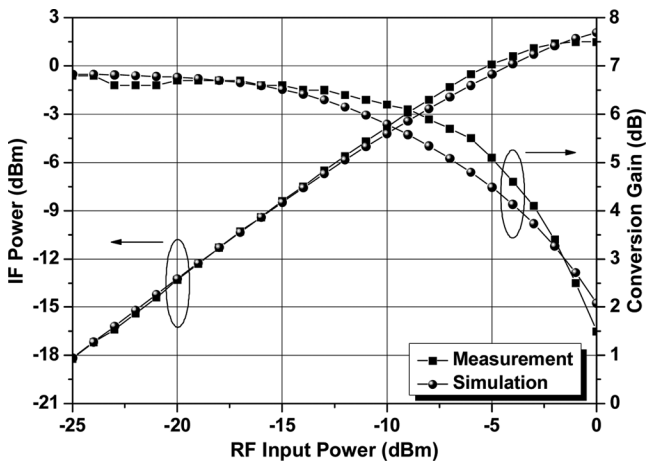

Fig. 5. Measured and simulated IF output power and conversion gain versus RF input power to illustrate 1 dB compression point with RF of 77 GHz, IF of 1 MHz and LO power of −5 dBm.

III. Experimental Results

The proposed mixer is fabricated using 65 nm CMOS technology with 1-poly and 8-metal layers (see Fig. 3). The width of the switching FET is equally divided between the normal switching cell and the split cell and therefore, all the FETs have the same width of 10 μm. The size of the chip is 790 μm × 590 μm, including all pads and on-chip balun. To convert single-ended LO input to differential one, a Marchand balun is used. The mixer consumes 3 mW from 1.2 V supply voltage.

The input matching for RF port uses transmission lines. The stacked grounded coplanar waveguide transmission line structure is adopted [10], where the lowest two metal layers are used for ground, and the signal line uses the top metal layer (copper) with thickness of 3 μm. The full-wave electromagnetic simulation is performed for extracting the S-parameters of transmission lines and layout parasitics.

The fabricated chip is measured by wafer probing. The RF and LO signals are generated with W-band source modules, and the power is measured using a power meter through a coupler. An external unity-gain buffer stage is used at the IF output port to transfer the output voltage to a spectrum analyzer without loss.

Fig. 4 shows measured and simulated conversion gains versus LO power with the RF of 77 GHz and IF of 1 MHz because the IF of the FMCW radar system is usually below 1 MHz. As shown in Fig. 4, the proposed mixer has a peak conversion gain when the LO power is −5 dBm, which is much smaller than that required for the conventional mixer and matched well with the simulation results. The conversion gain of the conventional mixer is simulated with the same-sized transistors without cell splitting. The conventional mixer has a peak conversion gain of 0 dB at LO power of 0 dBm, which confirms the advantage of the split switching cell. Fig. 5 shows the conversion gain and IF output power along with the RF input power. The LO power of −5 dBm is used to obtain the maximum conversion gain. The peak gain is 6.8 dB and the input 1 dB compression point is −7 dBm. The measured noise figure of the mixer is 21 dB, and the measured RF and LO input return losses are about 10 dB and 9 dB at 77 GHz, respectively.

IV. Conclusion

In this letter, a 77 GHz down-conversion mixer with low LO power and high gain by using a split self-driven switching cell is presented. The mixer achieves a peak conversion gain of 6.8 dB driven by low LO power of −5 dBm, while consuming 3 mW in 65 nm CMOS technology. The measurement results are in good agreement with the theoretical predictions and the simulation results.

References

[1] J. Lee, Y.-A. Li, M.-H. Hung, and S.-J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, Dec. 2010.

[2] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, I. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.

[3] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A 60-GHz down-converting CMOS single-gate mixer," in *RFIC Symp. Dig.*, Jun. 2005, pp. 163–166.

[4] H.-C. Kuo, C.-Y. Yang, J.-F. Yeh, H.-R. Chugng, and T.-H. Huang, "Design of a 60-GHz down-converting dual-gate mixer in 130-nm CMOS technology," in *Proc. Eurr. Microw. Conf.*, Sep. 2009, pp. 405–408.

[5] S.-G. Lee and J.-K. Choi, "Current-reuse bleeding mixer," *Electron. Lett.*, vol. 36, pp. 696–697, Apr. 2000.

[6] B. Afshar, Y. Wang, and A. M. Niknejad, "A robust 24 mW 60 GHz receiver in 90 nm standard CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2008, pp. 182–183.

[7] B. Razavi, "A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 477–485, Feb. 2008.

[8] S. A. Maas, *Nonlinear Microwave and RF Circuits*. Norwell, MA: Artech House, 2003, ch. 11, pp. 501–505.

[9] W. Choi, G. Jung, J. Kim, and Y. Kwon, "Scalable small-signal modeling of RF CMOS FET based on 3-D em-based extraction of parasitic effects and its application to millimeter-wave amplifier design," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3345–3353, Dec. 2009.

[10] J. Kim, B. Jung, P. Cheung, and R. Harjani, "Novel CMOS low-loss transmission line structure," in *Proc. IEEE Radio Wireless Conf.*, Sep. 2004, pp. 235–238.

[11] P. Sakian, R. Mahmoudi, P. van Zeijl, M. Lont, and A. van Roermund, "A 60-GHz double-balanced homodyne down-converter in 65-nm CMOS process," in *Proc. Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2009, pp. 258–261.

[12] R. Berenguer, G. Liu, A. Akhiyat, K. Kamtikar, and Y. Xu, "A 43.5 mW 77 GHz receiver front-end in 65 nm CMOS suitable for FM-CW automotive radar," in *Proc. Custom Integr. Circuits Conf. (CICC)*, Sep. 2010, pp. 1–4.