Single-Chip W-band SiGe HBT Transceivers and Receivers for Doppler Radar and Millimeter-Wave Imaging

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***Abstract*—This paper presents the first single-chip direct-conversion 77–85 GHz transceiver fabricated in SiGe HBT technology, intended for Doppler radar and millimeter-wave imaging, particularly within the automotive radar band of 77–81 GHz. A 1.3 mm $\times$ 0.9 mm 86–96 GHz receiver is also presented. The transceiver, fabricated in a 130 nm SiGe HBT technology with f_T/f_{MAX} of 230/300 GHz, consumes 780 mW, and occupies 1.3 mm $\times$ 0.9 mm of die area. Furthermore, it achieves 40 dB conversion gain in the receiver at 82 GHz, a 3 dB bandwidth extending from 77 to 85 GHz at 25 °C, and covering the entire 77–81 GHz band up to 100 °C, record 3.85 dB DSB noise figure measured at 82 GHz LO and 1 GHz IF, and an $\mathrm{IP}_{1\mathrm{dB}}$ of -35 dBm. The transmitter provides $+11.5$ dBm of saturated output power at 77 GHz, and a $\div 64$ static frequency divider is included on-die. Successful detection of a Doppler shift of 30 Hz at a range of 6 m is shown. The 86–96 GHz receiver achieves 31 dB conversion gain, a 3 dB bandwidth of 10 GHz, and 5.2 dB DSB noise figure at 96 GHz LO and 1 GHz IF, and -99 dBc/Hz phase noise at 1 MHz offset. System-level layout and integration techniques that address the challenges of low-voltage transceiver implementation are also discussed.**

***Index Terms*—Automotive radar, correlation, Doppler radar, low-noise amplifiers, millimeter-wave imaging, noise figure, phase noise, power amplifiers, SiGe HBT, W-band transceivers.**

I. Introduction

A VARIETY of applications, including multigigabit wireless data communications, automotive radar, and imaging are driving the development of millimeter-wave (mm-wave) transceivers in silicon. The development is occurring simultaneously in 130 nm SiGe BiCMOS [1] with f_T/f_{MAX} greater than 230/300 GHz, and 65 nm CMOS [2] with f_T/f_{MAX} up to 180/270 GHz. Silicon W-band transmitter and receiver integration efforts to date include a SiGe HBT 77 GHz phased array transceiver with 52 GHz VCO [3], [4], and individual W-band receivers and transmitters with fundamental frequency VCOs in SiGe HBT [5]–[13], in CMOS [14], and III-V [15] processes. None of the transceivers fabricated in silicon to date is direct-conversion with fundamental-frequency VCO, which is the preferred architecture for automotive radar sensors [16] and phased arrays [17].

As system architectures move toward phased arrays, implementation of a W-band automotive radar system in silicon requires careful attention be paid to minimizing power consumption. Circuit topologies and design methodologies which are robust at low voltage and high temperature are required [13], [18]–[23], as well as accurate modeling techniques for lumped and distributed passive components [22], [24], [25], and an understanding of the noise performance of fine-lithography SiGe HBTs [26]. However, a single-chip transceiver also presents system-level challenges related neither to circuit block performance, nor to a transmitter or receiver alone.

First, locating the transmitter and receiver on the same die makes the receiver vulnerable to on-chip LO leakage from the transmitter. Second, the transceiver architecture must be chosen to minimize power consumption for the desired maximum usable range. Adequate range and velocity resolution of at least 1 m and 1 km/h, respectively, are also needed in automotive applications, and the transceiver must be capable of a maximum unambiguous range of 150 m and a maximum detectable velocity of at least 250 km/h [17]. Frequency sweep linearity better than 0.1%, as described in [27], as well as minimum receiver noise figure and phase noise, and sufficient linearity must all be assured. Finally, the VCO in a transceiver must drive multiple circuit blocks, necessitating an LO distribution network to avoid overloading the VCO.

This paper presents a set of SiGe HBT single-chip direct-conversion receivers and transceivers operating in the 76–96 GHz band. Section II describes a transceiver design methodology for maximum range and minimum power consumption. In Section III, the top-level implementation of the transceiver is discussed, including the LO distribution network. Circuit block design methodologies are also briefly reviewed. Section IV presents a systematic layout methodology which maximizes transmitter-receiver isolation and minimizes I^2R losses. Sections V and VI summarize the transceiver fabrication technology and provide measurement results, respectively.

II. SiGe HBT Doppler Radar Design Methodology

A block diagram of a direct-conversion transceiver suitable for the implementation of an automotive radar sensor is shown in Fig. 1. The FM signal is applied directly to the VCO tuning input (V_{TUNE}). Although the VCO tuning may be nonlinear, the frequency divider monitors the precise frequency of the VCO

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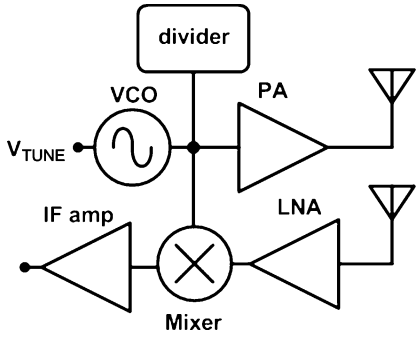

Fig. 1. General block diagram of a direct-conversion transceiver.

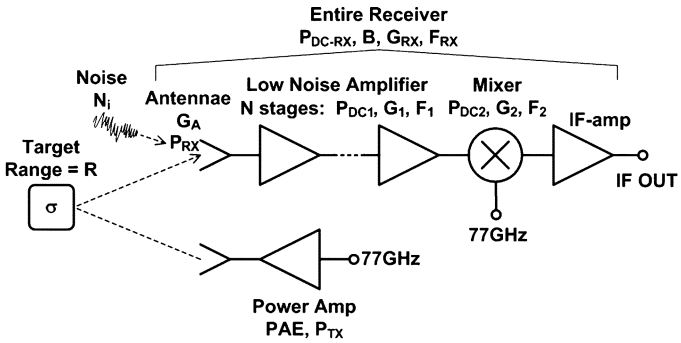

Fig. 2. Block diagram used for determination of the optimum transceiver topology.

and may be used to correct any nonlinearity. In this way, the frequency modulation linearity required in automotive radars may be achieved, and a phase-locked loop (PLL) may be implemented on-chip if desired.

A. Maximizing Usable Range and Power Consumption

The diagram in Fig. 2 is used to maximize the radar usable range for a given total system-level DC power consumption. In Fig. 2, the receiver is defined by its power dissipation $(P_{\mathrm{DC-RX}})$, the application-dependent IF bandwidth (B), total conversion gain (G_{RX}), and noise factor (F_{RX}). The transmitter supplies an output power of P_{TX} at a power-added efficiency of $\mathrm{PAE_{TX}}$, which is reflected from a target with radar cross-section σ at range R, producing an incident power of P_{RX} at the receiver antenna. The low-noise amplifier (LNA) is considered to contain N identical stages, all noise and impedance matched, consuming DC power P_{DC1}, having noise factor F_1, and gain G_1. Similarly, the mixer consumes DC power P_{DC2}, has a noise factor F_2, and a gain G_2. Because the IF amplifier is assumed to have no influence on the transceiver noise figure (NF), its gain and power dissipation are included in G_2 and P_{DC2} for simplicity. The transmitter and receiver antennas are identical with gain G_A, and noise temperature of 300 K.

The power incident on the receiver (P_{RX}) can be calculated using the radar equation

$$P_{\mathrm{RX}} = \frac{P_{\mathrm{TX}} G_A^2 c^2 \sigma}{(4\pi)^3 f_{\mathrm{LO}}^2 R^4} = 2.3 \times 10^{-2} \frac{P_{\mathrm{TX}}}{R^4} \tag{1}$$

TABLE I
PARAMETERS USED FOR THE CALCULATION OF EQUATIONS (4)–(7)

Parameter	Value	Notes
G_1	7 dB	3-stage LNA in [13] with 25dB gain, results in 7dB per stage for the common-source stages, and 11dB for the cascode stage.
F_1	3 dB	HBT noise figure estimated from extraction of noise parameters from y-parameters [26].
P_{DC1}	12.5 mW	LNA matching methodology presented in [13] and [31], LNA design presented in [19].
G_2	10 dB	Measured from the mixer + IF amp in [12] and [19].
F_2	13 dB	See above
P_{DC2}	70 mW	See above
PAE	15.7 %	PA measurements in [19].

where the target radar cross-section σ is assumed to be 30 m^2 for an automobile [28], c is the speed of light $(3 \times 10^8$ m/s), and f_{LO} is the local oscillator frequency (77 GHz). The antenna gain (G_A) is assumed to be 25 dB, with 100% radiation efficiency. Radar cross-sections of other important targets include motorcycles (5 m^2), pedestrians (0.5 m^2), and large trucks (200 m^2) [29], [30].

The signal-to-noise ratio (SNR) at the receiver IF output is then calculated using (2). The required receiver IF bandwidth (B) is approximately given by (3), where R_{MIN} is the required range resolution (or alternatively, the minimum target range). In this case, the values in (3) are chosen for the automatic cruise control application. It is assumed that signal processing at IF limits the overall receiver bandwidth. The receiver topology and transmitter output power were chosen to maximize the *range efficiency* of the radar, that is, the range per unit power dissipation, given by (4). In (4), the total power dissipation of the transceiver (P_{DC}) is given by (5), and the noise factor of the receiver (F_{RX}) can be found by calculating the contributions from the LNA and the mixer using the Friis equation. Numerical values for the parameters G_1, F_1, P_{DC1}, G_2, F_2, P_{DC2}, and PAE used in the calculation of (4) and (5) are given in Table I, along with notes on how they were obtained.

$$SNR_{\mathrm{IF}} = 2.3 \times 10^{-2} \frac{P_{\mathrm{TX}}}{kTBF_{\mathrm{RX}}R^4} = 3.7 \times 10^{10} \frac{P_{\mathrm{TX}}}{R^4 F_{\mathrm{RX}}} \tag{2}$$

$$B \approx \frac{c}{2R_{\mathrm{MIN}}} = \frac{3 \times 10^8}{2 \times 1m} = 150\ \mathrm{MHz} \tag{3}$$

$$\eta_R = \frac{R_{\mathrm{MAX}}}{P_{\mathrm{DC}}} = \frac{1}{P_{\mathrm{DC}}} \left(\frac{3.7 \times 10^{10} P_{\mathrm{TX}}}{F_{\mathrm{RX}}} \right)^{\frac{1}{4}} \tag{4}$$

$$P_{\mathrm{DC}} = \frac{P_{\mathrm{TX}}}{\mathrm{PAE_{TX}}} + NP_{DC1} + P_{DC2} \tag{5}$$

Illustrated in Fig. 3 is the maximum usable range (R_{MAX}) in meters versus the transmitted power (P_{TX}) in dBm for receivers having LNAs of 1–4 stages. Illustrated in Fig. 4 is the transceiver DC power dissipation (including only the LNA, power amplifier (PA), and mixer) in watts versus the maximum usable range in meters. As the maximum usable range increases, a multistage LNA results in lower overall power dissipation. High PAE is also critical to minimizing power consumption.

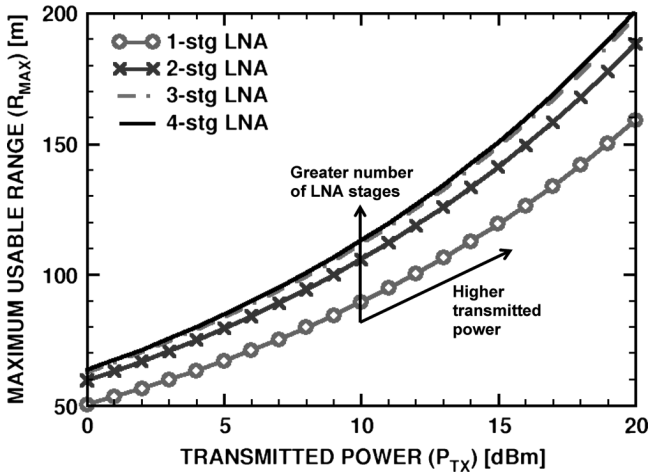

Fig. 3. Maximum usable range versus transmitted power for LNAs of 1–4 stages.

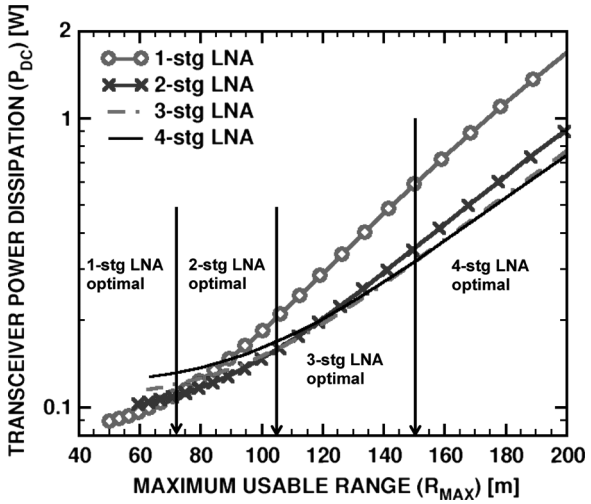

Fig. 4. Transceiver DC power dissipation ($P_{\rm DC}$) versus maximum usable range ($R_{\rm MAX}$).

At 150 m range, a transceiver with a 10% transmitter PAE consumes 437 mW, whereas with 16% PAE the power consumption reduces to 320 mW.

The required transmitted power and optimal number of LNA stages can be read from Figs. 3 and 4 as follows. First, decide on the required range, for example, 150 m. From Fig. 4, a 4-stage LNA is required to maximize η_R, and the transceiver consumes 320 mW. Finally, from Fig. 3, 150 m range requires +15 dBm of transmitted power. For the parameter values given in Table I, the gain and noise figure are expected to be $G_{\rm RX} = 38$ dB and $\rm NF_{RX} = 3.6$ dB.

B. Design for Low Phase Noise

In automotive radar applications, a velocity resolution of at least 1 km/h is required. For a 77 GHz carrier, this demands that the radar sensor detect a 70 Hz frequency shift, which represents 1 ppb sensitivity. Excellent close-in phase noise performance is required of the VCO in such a radar sensor, and therefore the VCO must be designed for minimum phase noise as in [18], making further improvements impossible without pushing the VCO HBTs into breakdown. In automotive applications, range correlation significantly reduces the phase noise at IF [32].

C. Receiver Output and Input Linearity

Receiver input compression can be dominated by power reflected directly from the antenna, or from surfaces placed in front of the antenna. In such systems, circuit topologies which provide high $\rm IP_{1dB}$ have been proposed [7], [33]. Receiver linearity requirements may be eased using separate transmit and receive antennas [17], or pulsed radar, which does not require simultaneous transmit and receive functions [28].

In Fig. 2, the IF amplifier must provide the maximum obtainable output swing to an A/D converter, whatever the target range (i.e. constant IF output power, independent of the RF input power $P_{\rm RX}$). Therefore, variable gain must compensate the full range of $P_{\rm RX}$. The maximum IF output power is given by

$$P_{\rm IF-MAX} = \frac{(V_{\rm DD} - 2V_{\rm CE-SAT})^2}{Z_{\rm OUT}} \tag{6}$$

where $V_{\rm DD}$ is the system supply voltage, $V_{\rm CE-SAT}$ is the collector-emitter saturation voltage, and $Z_{\rm OUT}$ is the IF amplifier output impedance.

At maximum range, the RF input power $(P_{\rm RX})$ is determined from (1), whereas at minimum range the RF input power is given by

$$P_{\rm RX} = 2.3 \times 10^{-2} \frac{P_{\rm TX}}{R_{\rm F}^2 R_{\rm MIN}^2} \tag{7}$$

where $R_{\rm F}$ is the Fraunhofer range. At short range, only a portion of the target lies within the antenna beamwidth, and the far-field assumption which produces the $1/R^4$ factor in (1) is not valid. In this case, evidence suggests that the received power varies as $1/R^2$ [28]. The required total variable gain is determined by dividing (7) by (1), which yields

$$G_{\rm VAR} = \frac{R_{\rm MAX}^4}{R_{\rm F}^2 R_{\rm MIN}^2}. \tag{8}$$

For $R_{\rm F} = 2$ m, $R_{\rm MIN} = 1$ m and $R_{\rm MAX} = 150$ m, 81 dB of total variable gain is required, independent of $Z_{\rm OUT}$. The variable gain must be apportioned as either attenuation or amplification at RF and/or IF, or attenuation of the transmitted power $(P_{\rm TX})$.

The RF input power $(P_{\rm RX})$ must never exceed the receiver $\rm IP_{1dB}$. The conditions under which this requirement is most difficult to satisfy occur at minimum range. The output power of the power amplifier must be adjustable such that

$$\rm IP_{1dB} \geq 2.3 \times 10^{-2} \frac{P_{TX} G_{VAR-PA}}{R_F^2 R_{MIN}^2} \tag{9}$$

is satisfied, where $P_{\rm TX}$ is the maximum transmitted power and $G_{\rm VAR-PA}$ is the required amount of attenuation. For $R_{\rm MIN} =$ 1 m, $P_{\rm TX} = +15$ dBm, and $\rm IP_{1dB} = -35$ dBm, the required value of $G_{\rm VAR-PA}$ is at least 28 dB. The remainder of the variable gain (53 dB) can be implemented at IF.

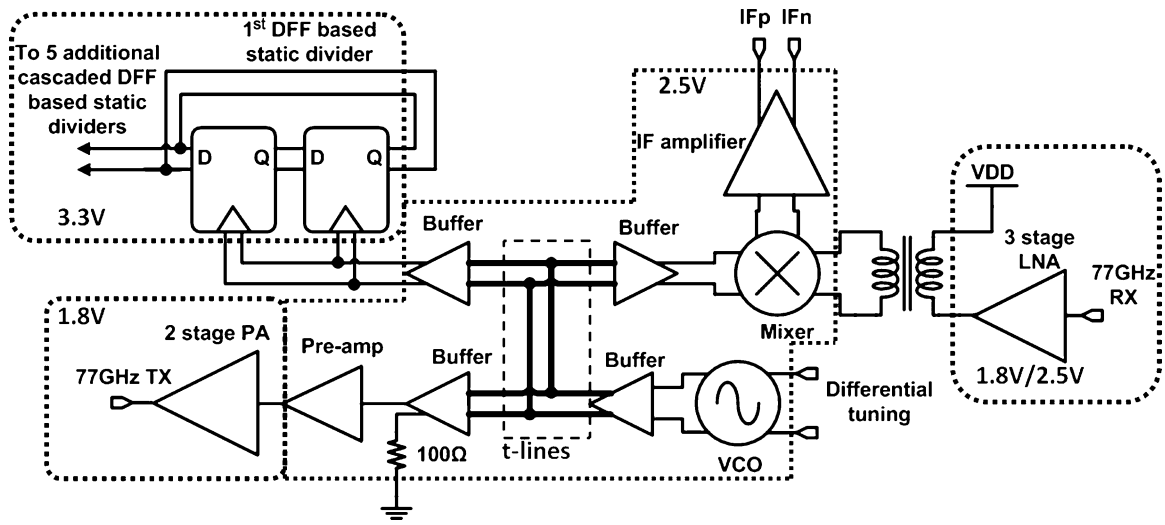

Fig. 5. Full block diagram of the 77 GHz Doppler radar transceiver.

TABLE II
EXPECTED PERFORMANCE OF THE RADAR TRANSCEIVER

Parameter	Value
R_{MAX}	150 m
R_{MIN}	1 m
Max Velocity	250 km/h
Velocity Resolution	< 1 km/h
Modulation linearity	0.1 %
G_{RX}	38 dB
NF_{RX}	3.6 dB
IP_{1dB}	-35 dBm
G_{VAR}	81 dB
$G_{VAR\text{-}PA}$	28 dB
P_{TX}	+15 dBm
PAE	15.7 %
PN @ 100 kHz	-80 dBc/Hz
Isolation	-88 dBm
P_{DC}	320 mW

D. Isolation

To ensure that LO leakage from the transmitter into the receiver is not dominated by on-chip leakage, the on-chip LO leakage should be less than the received power (P_{RX}) for a target at R_{MAX}. Table II summarizes the radar transceiver topology and performance.

III. TRANSCEIVER IMPLEMENTATION

A block diagram of the implemented direct-conversion transceiver is shown in Fig. 5. The received signal is amplified by a 3-stage LNA and converted to a differential signal. Instead of the optimal 4-stage common-emitter LNA design, a cascode is used for the final stage to ease the task of impedance matching between LNA stages, and between the LNA and mixer. A double-balanced Gilbert cell mixer down-converts the RF signal to baseband, and an IF amplifier provides additional current gain to drive 50 Ω off-chip test equipment. The VCO employs the Colpitts architecture designed for minimum phase noise [18]. Differential tuning inputs are provided for the frequency modulation, and a /64 static frequency divider is also included on-chip. A tuned LO distribution network distributes the VCO signal to all circuit blocks. The implementation of all circuit blocks except the LO distribution network is described in [13], [18], [19], and [34]. Variable gain is implemented within the power amplifier by adjusting the bias current in the first two stages. Lumped inductors over substrate are used wherever possible in place of distributed microstrip lines over metal, minimizing die area. Transmission lines remain useful where bias signals must be passed beneath RF signals. Lumped inductors are modeled using ASITIC as described in [22] and [24], and transmission lines over metal are modeled with HFSS, as outlined in [22], and are implemented using the techniques established in [25].

A. LO Distribution Network

The VCO drives a single 20 mA buffer, which drives a network of transmission lines followed by three 10 mA buffers. The 10 mA buffer schematic is shown in Fig. 6. The cascode topology is chosen for its high reverse isolation (low S_{12}), which prevents backward leakage of noise from the PA and frequency divider through the LO distribution network. In Fig. 6, R_1 and R_2 provide the correct DC levels for the load circuitry, and increase the bandwidth of the buffer in case the buffer is not tuned to the VCO center frequency. Emitter degeneration also improves the buffer bandwidth and linearity.

The 10 mA buffer must be matched to several different loads (the mixer, divider, and power amplifier). To minimize the design effort, the sizes of Q_1 and Q_2, and the values of L_C, L_E, and $R_1//R_2$ are fixed, while the ratio R_1/R_2 is chosen to obtain the correct DC level at the output of each buffer. Only L_{INT} and C_1 are chosen to achieve approximate matching to a particular HBT load.

B. Receiver Center Frequency Shifting

To investigate the performance achievable by receivers across the W-band, the 3 dB bandwidth of the 77–85 GHz receiver was shifted to 86–96 GHz. Noise figure measurements from both receivers allow inferences to be drawn about the noise performance of the HBTs which we cannot measure directly in the

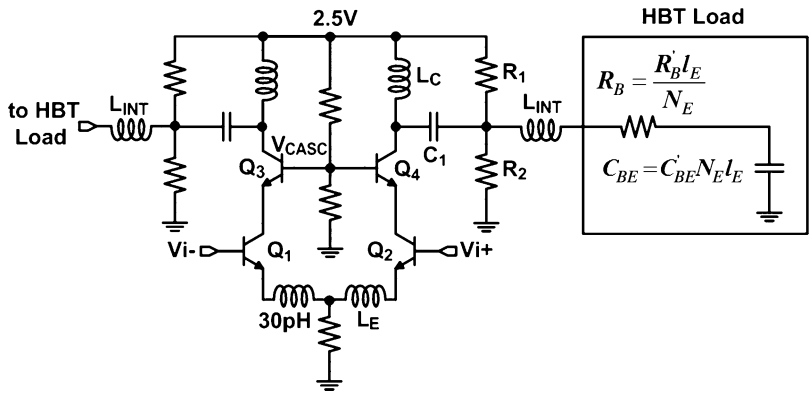

Fig. 6. 77 GHz broadband, tuned LO buffer schematic.

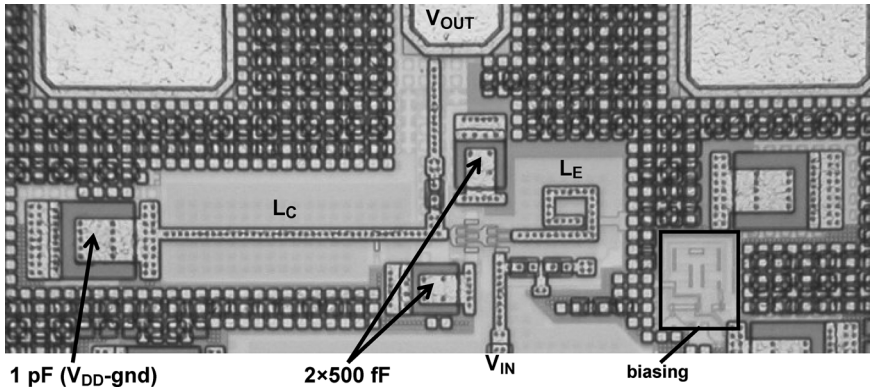

Fig. 7. Layout of a single-ended 77 GHz cascode amplifier.

W-band. Strategies for optimizing the biasing of low noise receivers at different frequencies were also investigated.

IV. Layout Methodology for W-band Transceivers

Aside from the fact that cascading multiple separate circuit blocks at 77 GHz is hampered by the interaction between them, the layout of a full transceiver in which transmission and reception occur simultaneously is complicated by the requirement to satisfy isolation levels exceeding 85 dB in an area smaller than 1 mm^2. This section outlines a systematic layout methodology that addresses isolation and IR drops through the use of decoupling capacitors, bias and power planes, and n-well and p-sub isolation structures.

A. Local Decoupling Capacitors and Isolation Rings

The layout methodology begins at the circuit block level. Decoupling capacitors (1 pF or 500 fF) are placed at the end of every parallel passive component (L, C, or t-line) to provide a low-impedance AC ground. Decoupling capacitors, which must resonate beyond the operation frequency of the transceiver, are also placed directly beside the base of every common-base transistor for the same reason. If necessary, biasing circuitry is moved aside to make space for decoupling capacitors. Circuit blocks are also surrounded by an n-well and p-well isolation ring to prevent noise from entering or leaving. In Fig. 7, a close-up view of the third stage of the 77 GHz LNA layout in [19] is used to demonstrate the placement of decoupling capacitors. Substrate isolation structures are not visible because they are covered by the higher metal layers.

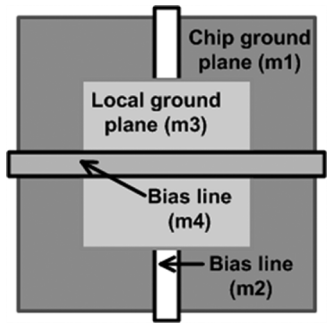

Fig. 8. Local ground planes are used to isolate bias lines.

B. Circuit Block Placement and Sharing Bias Circuitry

The bias signals of large-signal circuits like the VCO or PA must not be shared (or even crossed) with those for sensitive circuits like the LNA. In systems requiring low phase noise, the VCO must be isolated from all other circuits. When bias lines of different circuit blocks must be crossed, a local ground plane was placed between them to minimize their capacitive coupling, as illustrated in Fig. 8. The VCO and the LNA were placed far away from the PA and frequency divider, without unduly increasing the total die area. Substrate isolation structures (discussed later) were placed around the PA and frequency divider to further minimize noise propagation.

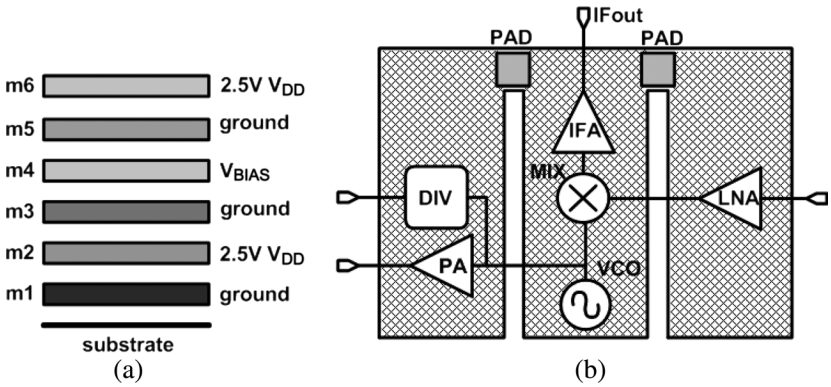

Fig. 9. Interlaced, parallel-connected, and split metal planes for bias and power distribution.

C. Metal Planes for Power and Bias Distribution

Power and bias signals were routed using maximally capacitive, minimally inductive and resistive metal planes, or lines. Minimizing the resistance reduces the IR drop from the pad to the local power supply for each circuit block, and the capacitance of the metal planes contributes further to on-chip decoupling, which prevents the propagation of high frequency noise between adjacent circuit blocks. Fig. 9(a) shows how power, bias, and ground planes are interlaced to increase their capacitance, and Fig. 9(b) shows how metal planes common to all circuits were split to prevent the leakage of noise generated at one point on the plane to sensitive circuits located elsewhere on the same plane.

In the transceivers and receiver presented here, circuit block isolation is further increased through the use of separate power supply domains for the LNA, PA, and digital (divider) circuitry. Moreover, noisy power signals, such as the PA supply, have minimal contact to the substrate. Substrate leakage was also reduced by placing n-well and p-sub contacts between circuit blocks. At mm-wave frequencies, a pattern of small checkered n-well and p-sub regions is preferred over a continuous n-well region because of it provides lower overall capacitance.

D. A Layout Cell for Efficient Creation of Metal Planes

Solid metal planes cannot be created on-chip without causing over-density DRC violations. Slotting or "cheesing" the metal planes manually is time consuming for a large chip, as is forming isolation structures manually around every circuit block. A flexible, time-efficient, and effective method of creating substrate isolation patterns, and stacked metal planes that meet all density rules was developed and is described in this section.

Consider stacking the three shapes shown on the left in Fig. 10 into a single layout cell. Three types of regions (circled in dashed lines on the right) are formed: region A, where the n-wells can be connected to metal-2, region B, where the substrate can be connected to metal-1, and region C where metal-1 and metal-2 can be connected. Any combination of metal layers can therefore be connected or left unconnected, almost arbitrarily.

The density of the two metal layers within the $5\ \mu\text{m} \times 5\ \mu\text{m}$ region was controlled by selecting the distance χ. The maximum allowable metal density is typically 80% in fine-lithography CMOS. Selecting $\chi = 1.87\ \mu$m yields a density of 70%, which allows for some margin of error to prevent over-density.

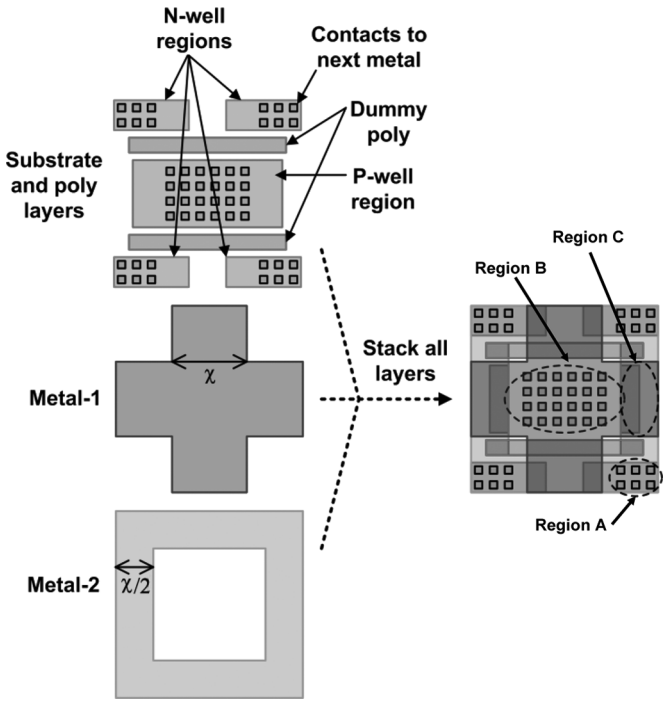

Fig. 10. A $5\ \mu\text{m} \times 5\ \mu$m layout cell for the efficient creation of metal planes and isolation structures.

The density of poly within the cell was similarly controlled. The cell therefore meets all density rules for all layers it contains. The cell was repeated over large areas of the chip to create slotted and interlaced metal planes with the maximum capacitance, minimum resistance, and minimum inductance allowed by the design rules, and a checker pattern of n-well and p-sub regions.

The system just described was extended to include an arbitrary number of metal layers. For example, if metal-3 "plus" shape was placed atop the cell shown in Fig. 10, it could be connected to metal-1 through the center of the cell where metal-2 is absent. By strategically selecting the location of vias and the shape of each metal layer ("plus" or "hollow square"), stacks of parallel-connected metal planes such as that shown in Fig. 9 were quickly created over large areas of the chip, including substrate isolation structures around circuit blocks. A further advantage of this layout system is that it uses a $5\ \mu\text{m} \times 5\ \mu$m grid to create all structures, which simplifies the top level layout.

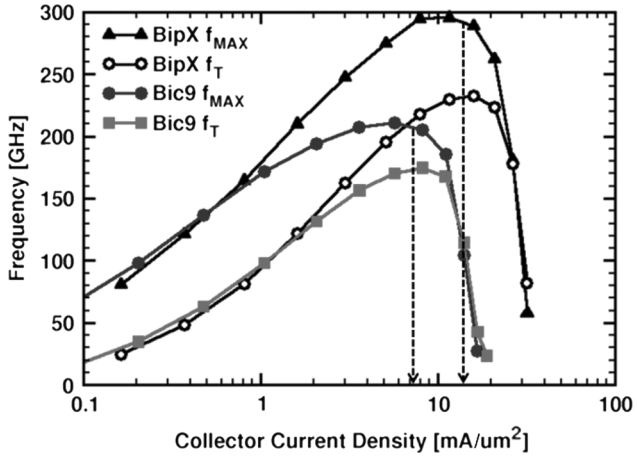

Fig. 11. Measured SiGe HBT f_T and $f_{\rm MAX}$ versus collector current density for two generations of 130 nm technology.

Connection of DC bias pads to the metal planes is also accomplished on the $5\ \mu$m $\times$ $5\ \mu$m grid. The DC bias pads, containing all metal layers connected together with as many vias as possible, are $68\ \mu$m $\times$ $58\ \mu$m in size, which creates a $2\ \mu$m distance between the pad and the surrounding layout cells. The metal layers which should be connected to the pad are then extended over the $2\ \mu$m distance all the way around the pad. Decoupling capacitors are always placed directly beside the pad to minimize the effects of off-chip noise sources.

V. Fabrication

The 77 GHz Doppler radar transceiver was designed and fabricated in a 130 nm SiGe HBT technology with 170 GHz f_T and 200 GHz $f_{\rm MAX}$ (termed "Bic9") and a 6 metal copper back-end. The HBT f_T and $f_{\rm MAX}$ versus collector current density (J_C) are illustrated in Fig. 11 for 1.2 V $V_{\rm CE}$. A 7th aluminum layer is also available, and was sometimes stacked atop metal-6 for even lower interconnect resistance. The transceiver was also fabricated in the next generation SiGe HBT technology with 230 GHz f_T, 300 GHz $f_{\rm MAX}$ (termed "BipX") and identical back-end of line (BEOL). Due to the higher $f_T/f_{\rm MAX}$ of the HBT in the second technology, the center frequency of the transceiver shifted upward from 77 to 82 GHz. The center frequency of this 82 GHz transceiver was then scaled upward to 96 GHz and the power amplifier was eliminated. A layout micro-photograph of the 77 or 82 GHz transceiver is illustrated in Fig. 12.

VI. Measurement Results

A. 77 GHz and 82 GHz Transceivers

As illustrated in Fig. 13, the 77 GHz transceiver fabricated in the 200 GHz $f_{\rm MAX}$ process has 26 dB peak down-conversion gain at 77 GHz and a 3 dB bandwidth of 6 GHz from 74 to 80 GHz. The identical transceiver fabricated in the 300 GHz $f_{\rm MAX}$ process (with identical BEOL) achieves 40 dB peak conversion gain centered at 82 GHz at room temperature, and 31 dB conversion gain at 100 °C. The 3 dB bandwidth of this receiver is 77–85 GHz at room temperature and covers the entire 77–81 GHz automotive radar band up to 100 °C. The frequency divider functions over the entire tuning range of the VCO up to 100 °C. The 82 GHz transceiver consumes 780 mW whereas the 77 GHz transceiver consumes 740 mW. Fig. 14

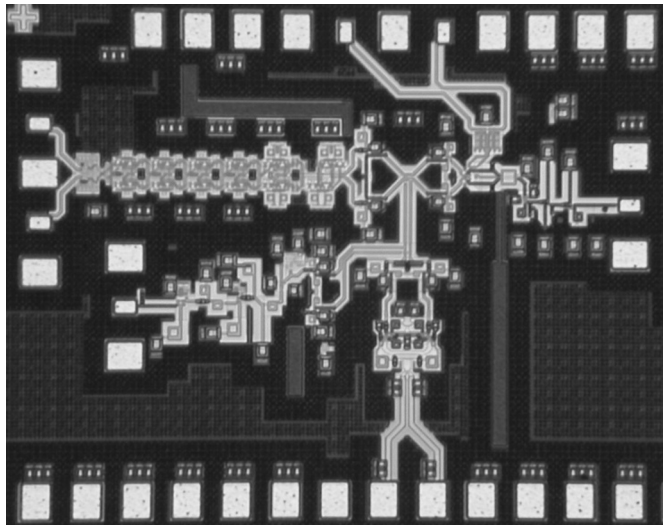

Fig. 12. Microphotograph of the 74–80 GHz (200 GHz $f_{\rm MAX}$ process) or 77–85 GHz transceiver (300 GHz $f_{\rm MAX}$ process).

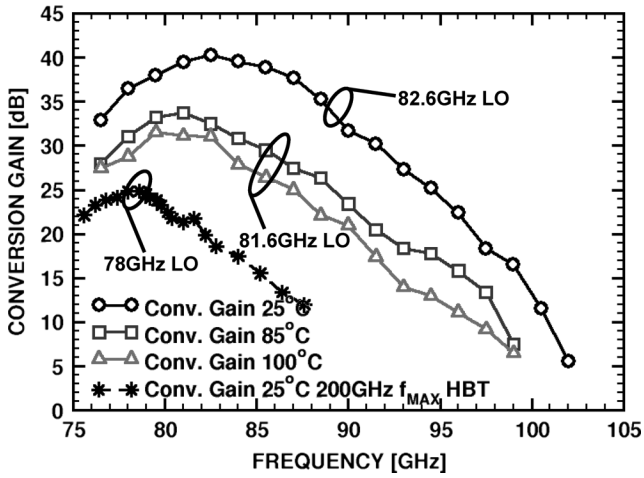

Fig. 13. Measured conversion gain (constant LO) for transceivers in 200 GHz and 300 GHz $f_{\rm MAX}$ SiGe HBT technology.

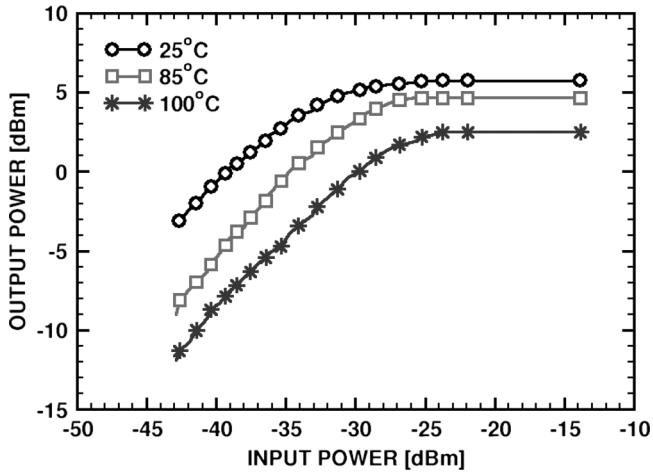

Fig. 14. Measured input and output compression points for the 82 GHz transceiver versus temperature.

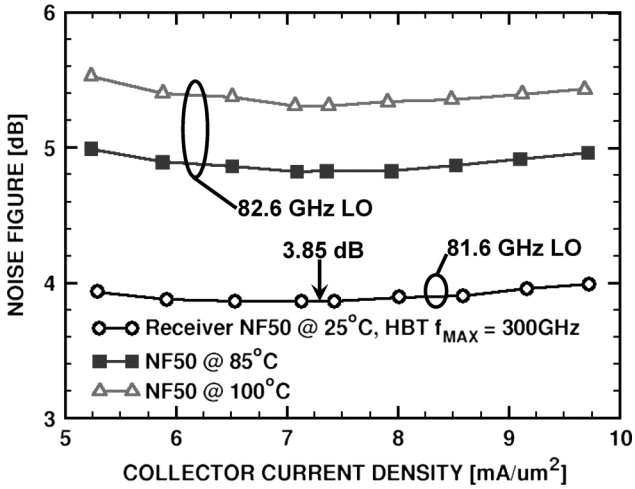

Fig. 15. Measured DSB noise figure (1 GHz IF) of the 82 GHz transceiver versus current density in the LNA and temperature.

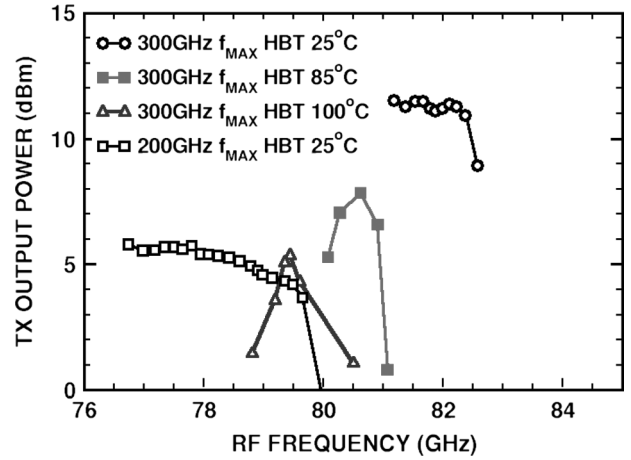

Fig. 16. Measured transmitter output power versus RF frequency and temperature.

illustrates the gain compression characteristics of the 82 GHz transceiver measured at 25 °C, 85 °C, and 100 °C and 1 GHz IF. The $\mathrm{IP}_{1\mathrm{dB}}$ is -35 dBm at 25 °C, and increases to -30 dBm at 100 °C, whereas the $\mathrm{OP}_{1\mathrm{dB}}$ is $+3$ dBm at 25 °C and falls to 0 dBm at 100 °C. The measured DSB noise figure of the 82 GHz transceiver versus collector current density in the LNA is shown in Fig. 15 at 1 GHz IF. The noise figure is 3.85 dB at room temperature and rises to 5.4 dB at 100 °C. To the authors' knowledge, this represents a record receiver noise figure for all SiGe and CMOS receivers operating above 75 GHz. The optimum noise figure current density is 7.1 $\mathrm{mA}/\mu\mathrm{m}^2$, and is constant versus temperature.

The transmitter output power is illustrated in Fig. 16 as a function of the VCO tuning range for the 77 GHz transceiver at 25 °C, and for the 82 GHz transceiver up to 100 °C. The output power of the transceiver is $+11.5$ dBm, however, the output power of the power amplifier alone is adjustable from a maximum of $+14.5$ dBm down to -18.1 dBm, which represents a total of 32.6 dB gain variation. Table III lists the contribution of each circuit block to the power consumption of the 82 GHz transceiver.

TABLE III
MEASURED POWER CONSUMPTION OF CIRCUIT BLOCKS IN THE 77–82 GHz SiGe HBT TRANSCEIVER

Circuit Block	V_{CC} (V)	P_{DC} (mW)
LNA	1.8 & 2.5	53
Mixer	2.5	12
IF amplifier	2.5	50
VCO	2.5	120
PA	1.8 & 2.5	175
6-stage divider	3.3	268
LO tree	2.5	152
TOTAL	**n/a**	**780**

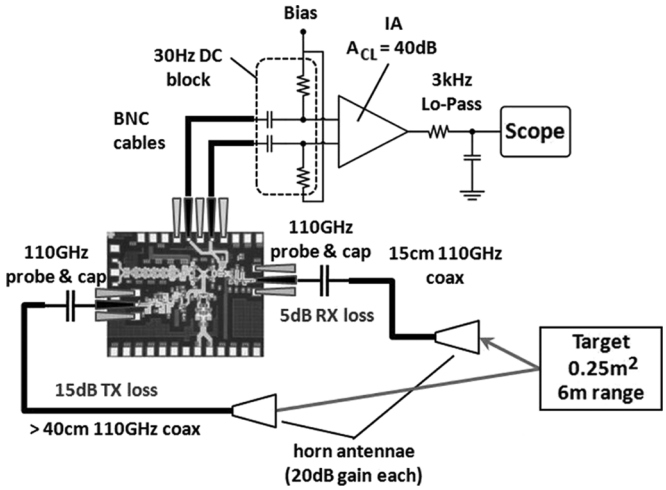

Fig. 17. Experimental setup diagram for measuring the Doppler shift.

B. Detecting the Doppler Shift

To verify the operation of the transceiver as a Doppler radar, the experimental setup shown in Fig. 17 was used. Horn antennas, with 20 dB gain each, are connected to the receiver input and transmitter output using 110 GHz coaxial cables and GGB probes. The continuous-wave signal is reflected off the moving target (a 30 cm $\times$ 40 cm aluminum sheet) 6 m away and into the receiver. An off-chip variable gain instrumentation amplifier with high common-mode rejection ratio amplifies the resulting Doppler signal by 0–40 dB, and converts it to single-ended before it is displayed on the oscilloscope, as in [35]. The total attenuation in the probes and cables is approximately 20 dB.

When the aluminum sheet is moved at a range of 6 m, the Doppler signal in Fig. 18 is generated. The frequency is less than 30 Hz, corresponding to a velocity of less than 0.42 km/h. Note that the signal is clipping at 10 V_{PP}, indicating that the system can detect a much smaller (or more distant) target. The Doppler shift experiment was successfully repeated at 100 °C, albeit with smaller signal amplitude, concomitant with lower conversion gain and reduced transmitted power.

C. Phase Noise at IF

The effect of range correlation on the phase noise spectrum at IF in radar systems is derived in [32]. To measure the phase noise

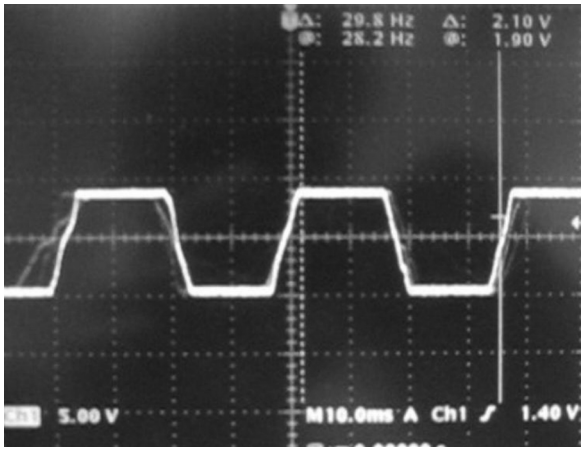

Fig. 18. Doppler signal generated by a 30 cm × 40 cm aluminum sheet at 6 m range.

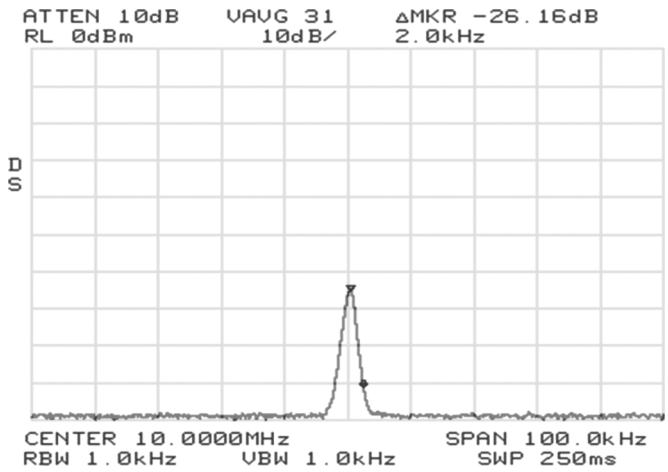

Fig. 19. Down-converted phase noise spectrum at IF generated by the 77 GHz transceiver in the 200 GHz f_{MAX} process.

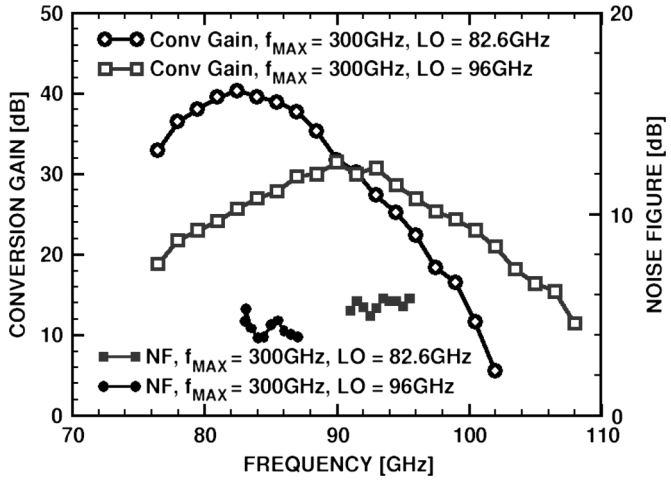

Fig. 20. Meausred conversion gain and noise figure of the 77–82 GHz transceiver and 86–96 GHz receiver at 25 °C.

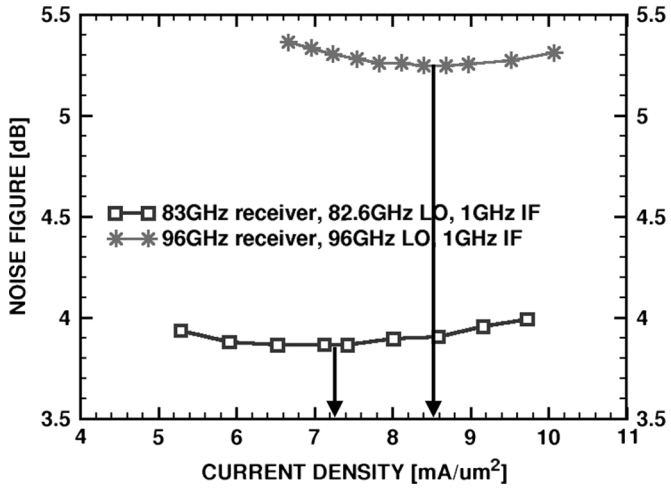

Fig. 21. Measured receiver noise figure versus LNA current density.

performance of the transceiver, narrowband frequency modulation was applied to the VCO tuning inputs, and the phase noise of one of the down-converted IF spurs was measured. The averaged IF spectrum shown in Fig. 19 indicates that the phase noise at IF is −56.12 dBc/Hz at 2 kHz offset, or based on the −20 dB/dec slope seen in [13], −90.12 dBc/Hz at 100 kHz offset. The frequency span shown in Fig. 19 is only 100 kHz, and 31 averaged sweeps are displayed. Such a stable IF spectrum is experimental evidence of range correlation, and suggests that radar sensor architectures not requiring PLLs are viable in automotive applications [10], [17].

D. 96 GHz Receiver

The 96 GHz receiver consumes 700 mW, and achieves 31 dB conversion gain, 5.2 dB noise figure, and a 3 dB bandwidth of 10 GHz extending from 86 GHz to 96 GHz, as illustrated in Fig. 20 for 96 GHz LO. The conversion gain and noise figure of the 82 GHz transceiver are shown on the same plot for comparison.

E. Noise Performance Across the W-band

Illustrated in Fig. 21 are the DSB noise figures of the 82 GHz transceiver and 96 GHz receiver (fabricated in the 230/300 GHz f_T/f_{MAX} technology) measured at 1 GHz IF. In these measurements, the VCOs are tuned to oscillate at exactly 82.6 GHz and 96 GHz, respectively, and the noise figure of each receiver is measured as a function of the current density in the first two stages of the LNA. The resulting optimum noise figure current densities are 7.1 mA/μm^2 at 82.6 GHz LO and 8.4 mA/μm^2 at 96 GHz LO. Finally, Table IV compares the measured performance of these transceiver to that of other state-of-the-art W-band transmitters, receivers, and transceivers.

VII. Conclusion

A single-chip direct-conversion transceiver for 77–81 GHz automotive radar has been presented. A 96 GHz receiver has also been shown. In comparison to previous efforts, they both operate largely from a 2.5 V supply, and contain static frequency dividers and fundamental frequency VCOs. The 77–85 GHz transceiver achieves a DSB noise figure of 3.85 dB, and the 96 GHz receiver achieves a DSB noise figure of 5.2 dB. Both

TABLE IV
STATE-OF-THE-ART 77–94 GHz SIGE HBT, SIGE BICMOS, AND CMOS RECEIVERS, TRANSMITTERS, AND TRANSCEIVERS

Ref.	RF/LO (GHz)	Gain (dB)	BW (GHz, % RF)	IP_{1dB} (dBm)	Rx NF (dB)	PN @ 1MHz (dBc/Hz)	P_{SAT} (dBm)	Divider 1st stage	P_{DC} (mW)	Area (mm^2)	Notes
[15]	77/2×38.5 off-chip LO	5	75–78 3.9%	not given	not given	not given	+9.3	none	not given	10	TX/RX InGaAs HEMT f_{MAX} > 300GHz.
[14]	85/90	12	75–95 22.2%	-18	7	-95	n/a	Static	206	0.66	RX 65nm CMOS
[11]	77/77 off-chip LO	n/a	n/a	n/a	n/a	-95	+16	Miller	2800	3.06	TX SiGe HBT f_{MAX} >200GHz.
[10]	79/79	n/a	n/a	n/a	n/a	not given	+1.5	Miller	4125	1.16	TX SiGe HBT f_{MAX} = 300GHz.
[5]	77/2×38.5	30.5	not given	-22	not given	not given	+12.5	not given	not given	TX 3.8 RX 4.3	Separate TX/RX SiGe HBT f_{MAX} = 300GHz
[7]	80/80 off-chip LO	28	not given	-16	11 (SSB)	not given	n/a	none	1100	1.1	Quadrature RX SiGe HBT f_{MAX} > 200GHz.
[4] RX [3] TX	77/52	35	76-80 5.2%	-27.5	8-10	-95 @ 54GHz	+12.5	52GHz Injection	161 593	2.25 4.25	TX/RX, ×4 SiGe HBT f_{MAX} = 250GHz.
[8]	77/77	30	not given	-26	11.5 (SSB)		n/a	none	440	1.16	RX SiGe HBT f_{MAX} = 330GHz.
[6]	77/77	40	76–78 2.6%	-38	not given	-93	n/a	none	195	1.7	RX SiGe HBT f_{MAX} = 250GHz.
[13]	76/77	24	68–76 10.3%	-22	4.8	-98	n/a	Static	123	0.23	RX SiGe HBT f_{MAX} = 250GHz.
This Work	77/77	**25.6**	**76–81 6.5%**	**-24**	**9**	**-99**	**+5.8**	**Static**	**740**	**1.17**	**TX/RX SiGe HBT f_{MAX} = 200GHz.**
This Work	**82/82**	**40**	**77–85 9.8%**	**-35**	**3.85**	**-99**	**+11.5**	**Static**	**780**	**1.17**	**TX/RX SiGe HBT f_{MAX} = 300GHz.**
This Work	**94/96**	**31**	**85–96 11.4%**	**-30**	**5.2**	**-99**	**n/a**	**Static**	**700**	**1.02**	**TX/RX SiGe HBT f_{MAX} = 300GHz.**

are records for silicon receivers above 75 GHz. Based on the 3.85 dB noise figure, 32 dB of variable gain in the PA up to a maximum of +11.5 dBm, 45 dB of off-chip variable gain at IF, a receiver OP_{1dB} of +3 dBm and IP_{1dB} of −35 dBm, and TX/RX antennas with 25 dB gain each, the usable range of the radar transceiver is 125–0.75 m. The transceiver may thus be employed in a variety of automotive applications such as automatic cruise control, blind-spot monitoring, collision avoidance, pre-collision intelligence, and road surface monitoring. The transceiver is capable of detecting a Doppler shift of only 30 Hz (0.42 km/h), which proves that it has obtained the velocity resolution demanded of automotive radar systems. The power consumption of the entire transceiver is 780 mW, which is low in comparison to the combined power consumption of other transmitters and receivers reported in the literature. Also demonstrated is the strong correlation of the transmitted and received phase noise in a Doppler radar transceiver.

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