Design of Gain Optimized Broadband Low Noise Amplifiers at 120 GHz using SiGe Technology

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***Abstract*— This paper presents the design of single-ended, double stage cascode low noise amplifiers at 120 GHz. A design methodology employing three techniques for gain enhancement of the LNA is presented. The effect of traditional emitter - degeneration technique and its feasibility for simultaneous noise and power matching is evaluated at 120 GHz. The LNAs are designed in a 250 GHz f_T and 300 GHz f_{max} 0.13 µm SiGe:C BiCMOS process. By employing the three design techniques the gain of the LNA is improved by almost 3.5 dB. The two stage gain optimized LNA achieves a gain of 24 dB and a noise figure of 7.2 dB. The circuit works with a supply voltage of 3.3 V and consumes less than 40 mW of power.**

Keywords-; SiGe Heterojunction Bipolar Transistor; Low Noise Amplifier; Broadband; Six-Port; 120 GHz

I. INTRODUCTION

The area of mm-wave circuit design has become increasingly popular in the recent years. Several wireless applications already exist, including wireless communication at 60 GHz, collision-avoidance radar at 77 GHz and mm-wave imaging at 77 and 94 GHz [1] [2]. There has been an increasing demand for high data rate communication in recent years and this increase has led to higher operating frequencies which demands for state-of-art receiver front-ends. Applications like wireless HDTV transmission require a high bandwidth and operating at higher frequencies allows this to be achieved easily. High frequency operation allows transmission of uncompressed data thus enhancing the picture quality. For mm-wave imaging systems high frequency operation provides detailed information about the composition of the materials, electromagnetic absorption rates and enhances the image resolution drastically [3]. The mm-wave frequency band around 120 GHz appears to be a promising candidate due to the availability of a large bandwidth and a relatively lower atmospheric absorption compared to the 60 GHz band.

The advancement in silicon based semiconductor technology has increased the demand for low cost receivers and this need is driving the development of both heterodyne and direct conversion receiver front ends. Stepping into mm-wave frequency regime the direct conversion receivers appears to be an excellent low cost alternative to the heterodyne receivers which requires high quality and expensive IF filters. An example for a receiver architecture which can easily be tailored to work as a direct conversion receiver for wireless communication is a six-port receiver which was till now used in software radio applications and radars [4]. A six port receiver shown in figure 1 eliminates the use of mixers for frequency down conversion and employs the concept of additive mixing and power measurements for signal detection. The low noise amplifier serves as the heart of an advanced receiver front end since it determines the noise performance of the entire receiver. In this paper we first present the design of a two stage cascode LNA in section III-A which achieves a gain of around 20 dB and Noise figure of 7.2 dB dissipating 30 mW of dc power. The effect of emitter degeneration for simultaneous noise and power matching at 120 GHz is discussed in Section III-B. Section III-C presents three techniques that help to improve the gain of the LNA presented in section III-A by almost 3.5 dB.

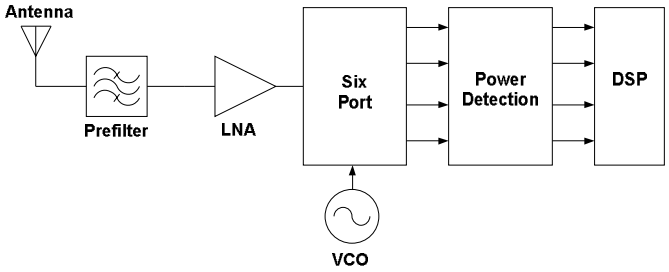

Figure 1. Six-Port Receiver Architecture

II. TECHNOLOGY

The design of the low noise amplifiers discussed in this work are carried out using an advanced 0.13 µm SiGe:C BiCMOS process from IHP. The technology provides SiGe:C HBTs with upto 250 GHz transit frequency and 300 GHz oscillation frequency. The effective emitter width is 0.12 µm and the open base breakdown voltage is 1.7 V. The technology provides five thin aluminium metal layers and two thick top metal layers for signal routing and also provides MIM-capacitors and poly-silicon resistors. Transmission lines are used for the design of the matching networks and implemented with a thick top metal 2 layer over top metal 1 layer. A 4 µm top metal 1 signal layer over top metal 2 ground plane results in a 50 ohm transmission line.

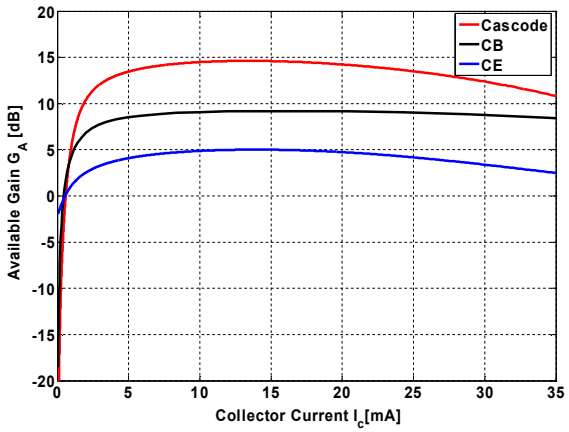

Figure 2. Available Gain of CE, CB and Cascode Amplifiers at 120GHz

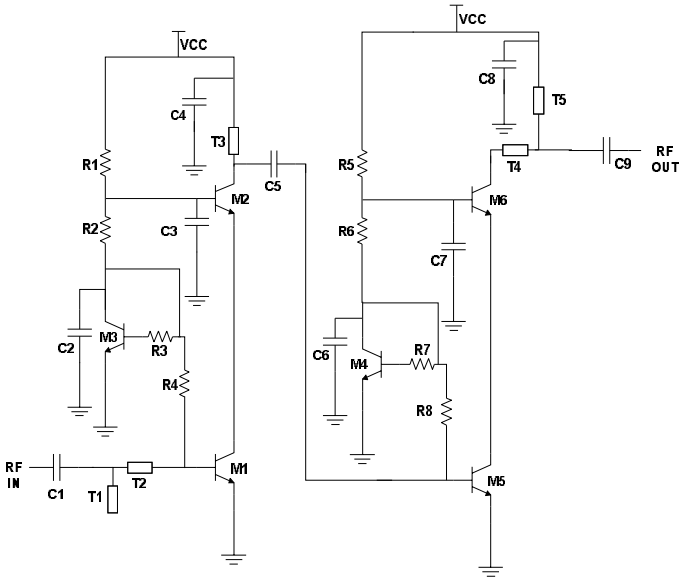

Figure 3. Schematic of the Double Stage Cascode LNA

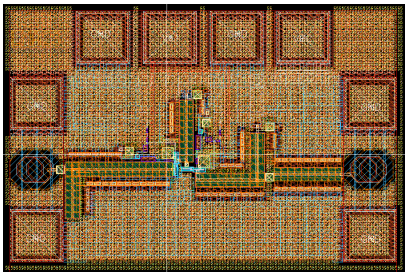

Figure 4. Layout of the Double Stage Cascode LNA

III. CIRCUIT DESIGN

A single ended topology was chosen for the LNA design. A single-ended design provides lower power consumption and prevents degradation of noise performance that would arise in a differential design due to baluns. Three common amplifier configurations were evaluated at 120 GHz and the cascode configuration was selected due to the availability of high gain

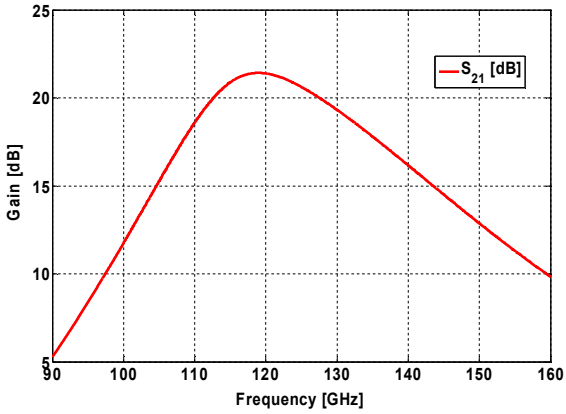

Figure 5. Simulated Gain of the Double Stage LNA

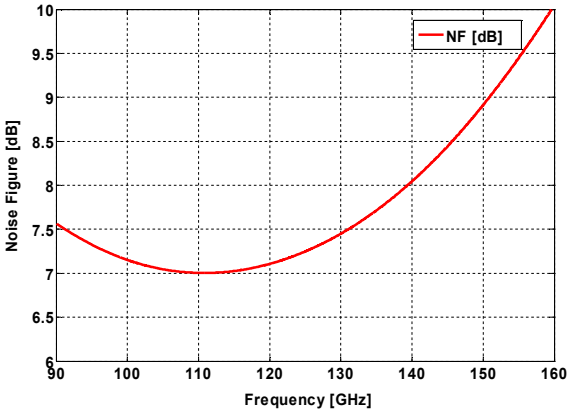

Figure 6. Simulated Noise Figure of the Double Stage LNA

and reverse isolation which improves stability. Figure 2 shows the simulated values of available gain for the Common Emitter (CE), Common Base (CB) and Cascode configurations. It can be seen that for a given bias current the cascode amplifier achieves a higher gain than the others.

A. Double Stage Cascode LNA Design

Figure 3 shows the schematic of the double stage LNA. The amplifier is biased at a higher current than the optimum noise current density to achieve a higher gain with a slight degradation in noise figure. The matching networks are implemented with 50 Ohm transmission lines as described in the previous section. This novel transmission line structure as proposed in [5] provides high quality grounding throughout the chip which is very important for an mm-wave LNA design.

Simulation results showed that matching for maximum power resulted in a noise figure degradation of only 0.5 dB and thus power matching is employed in this design. The transmission lines T1, T2 and T4, T5 form the input and output matching networks respectively. The parasitic pad capacitances of the input and output GSG pads were taken into account during the design of the matching networks and this helped to minimize the length of the transmission lines. A combination of a current mirror circuit and voltage divider circuit was used to bias the cascode stages. The resistors R4 and R8 help to decouple the RF from the DC path which would otherwise lead to degradation in noise figure.

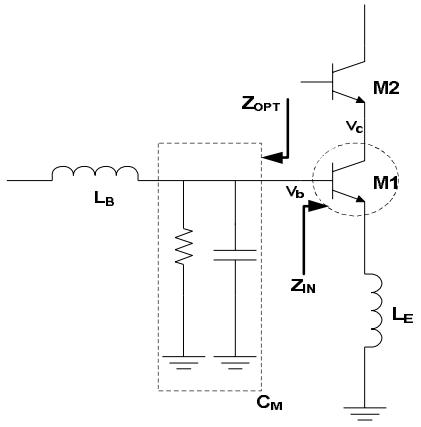

Figure 7. Emitter Degeneration for Simultaneous Noise & Power Matching

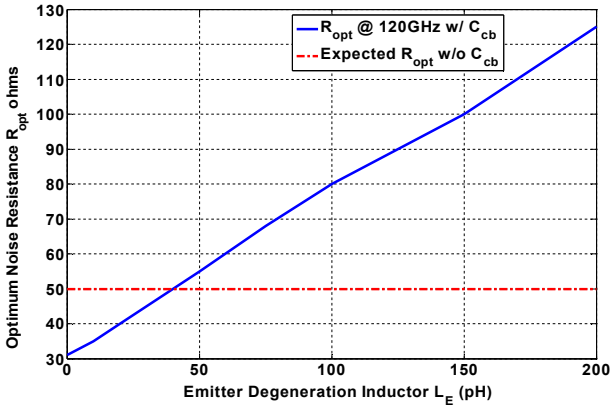

Figure 8. Variation of Optimum Noise Resistance with Emitter Inductor

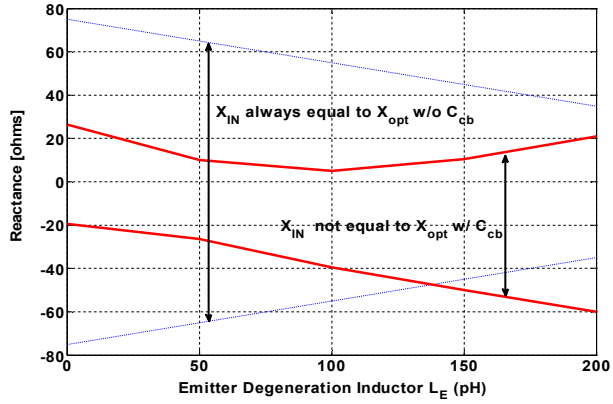

Figure 9. Variation of Reactances with Emitter Inductor

Maximum power transfer between the stages was achieved by using a LC matching network consisting of T3 and C5. This amplifier achieved a gain of 20.6 dB and a noise figure of 7.2 dB as shown in Figure 5 and 6 drawing a current of 9 mA from a dc power supply of 3.3 V. The design was optimized around 125 GHz to take into account process variations. The amplifier shows a 3-dB bandwidth of around 24 GHz. Figure 4 shows the layout of the LNA. On the layout the CE and CB transistors were placed as close as possible to each other and the high frequency grounding capacitors C3 and C7 at the base of the

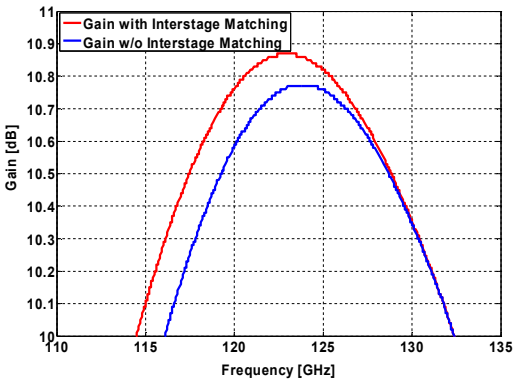

Figure 10. Gain Enhancement with CE-CB Interstage Matching

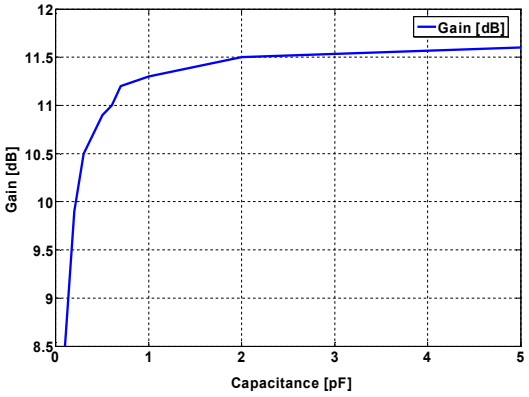

Figure 11. Variation of LNA Gain with Grounding Capacitance

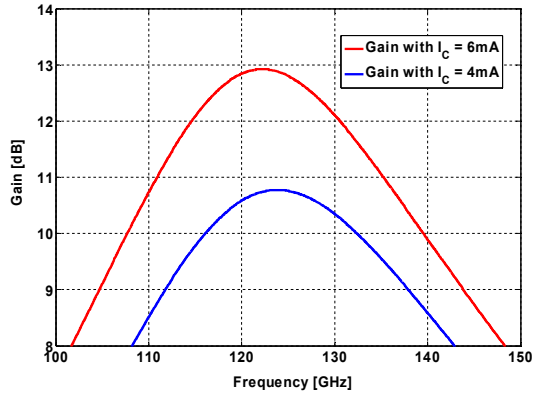

Figure 12. LNA Gain Improvement with a Higher Bias Current

transistors M2 and M6 were placed extremely close to the LNA to minimize any parasitic inductances. Also the presence of a very good ground plane helps to ground the emitter of the CE transistors in a very efficient way. An extra dc pad was provided to control the bias current of the amplifier externally.

B. Effect of Emitter Degeneration at 120 GHz

The method of emitter degeneration as proposed in [6] has been traditionally used to provide a simultaneous noise and power match during an LNA design [7] [8]. Figure 7 shows the emitter degeneration concept. This method makes use of three assumptions for RF circuit Design. 1). The emitter inductor

value (L_E) does not affect the real part of the optimum noise impedance (R_{opt}) and only changes the input impedance Real (Z_{IN}). 2) The optimum Noise reactance (X_{opt}) and the input reactance (X_{IN}) are always the same. They change in the same way with the emitter inductor values and have the same magnitudes always. 3) The minimum noise figure (NF_{min}) of the amplifier is not a function of the emitter length at the optimum current density. However for an LNA design presented at 35 GHz in [9] the violations of the above assumptions were explained. The reason was the pronounced miller effect of the CE transistor (modeled by C_M in Figure 7) caused due to the collector base feedback capacitance (C_{cb}) of the cascode which was negligible at RF frequencies. Figure 8 and 9 shows the impact of emitter degeneration at 120 GHz and it can be observed that the assumptions in [6] fail. The results match closely with the theory presented in [9] and thus the emitter degeneration method could not be used for simultaneous noise and power matching in this design. The pronounced miller effect due to C_{cb} at mm-wave frequencies along with the emitter degeneration inductor causes the input reactance to become more and more capacitive and thus it never equals to the magnitude of the optimum noise reactance which is a major requirement for simultaneous noise and power matching. Also the optimum noise resistance no longer stays constant and equal to 50 ohm as shown in Figure 8.

C. *Design Methodology for Gain Optimization*

The gain of the double stage cascode LNA can be further enhanced by using three additional design techniques without affecting the noise figure. They are 1) Interstage Matching between the CE and CB transistors of the cascode; 2) Increasing the high frequency grounding capacitor at the CB transistors M2 and M6 and 3) Biasing the second stage at a higher current.

Figure 10 shows the impact of introducing the interstage matching between the CE and CB transistors. We can see that the gain of the amplifier can be improved by around 0.2 dB by using this technique. A small transmission line is used to provide a power match between the CE and CB transistors in both the stages of the LNA. Figure 11 shows the gain enhancement obtained by increasing the high frequency ground capacitor value at the common base transistor. Simulated results shows that by using a higher capacitor value the gain of the amplifier can be improved by almost 1 dB. Figure 12 shows the impact of increasing the bias current for the second stage. The values of the resistors R5 and R6 were changed in the schematic to bias the second stage at a higher current of 6 mA. This led to almost 2 dB gain enhancement. From theory if the gain of the first stage of cascade is high enough, the noise contributions from all the other stages can be eliminated and thus the noise figure of the LNA presented here does not degrade even when the second stage is biased at a higher noise figure. All the above three techniques were combined and the design was modified. Figure 13 shows the gain of the modified LNA. It can be observed that almost 3.5 dB improvement in the gain of the LNA could be achieved. The simulated 1-dB Compression point of the LNA is -19 dBm and the IIP3 is -10 dBm. The gain enhancement procedure shows no major impact on the linearity performance of the LNA.

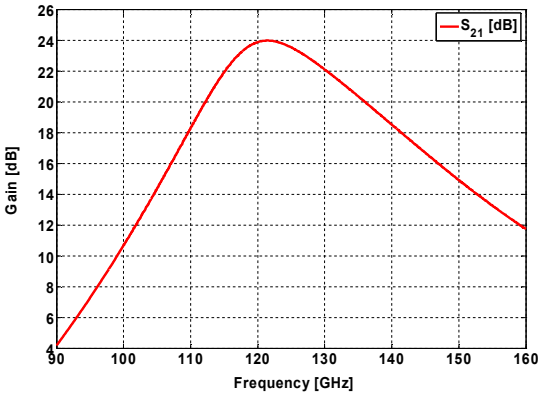

Figure 13. Gain of the Optimized LNA

IV. CONCLUSION

Design of a double stage cascode LNA at 120 GHz is presented using a 0.13 µm SiGe BiCMOS process. The impact of emitter degeneration at 120 GHz is studied and it is found that at mm-wave frequencies the traditional emitter degeneration method does not work any more for simultaneous noise and power matching. Three design techniques are presented that helps to improve the gain of the low noise amplifiers considerably. Following the design methodology presented in this work we are able to achieve an LNA with a gain of 24 dB and noise figure of 7.2 dB at 120 GHz with a 3-dB bandwidth of approximately 24 GHz.

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