A 130nm SiGe BiCMOS technology for mm-wave applications featuring HBT with f_T/f_{MAX} of 260/320 GHz

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***Abstract* — A manufacturable 130nm SiGe BiCMOS RF technology for high-performance mm-wave analog applications having a high-speed SiGe Heterojunction Bipolar Transistor (HBT) integrated into a full-featured RFCMOS is presented. The technology features a high performance (HP) SiGe HBT with f_T/f_{MAX} of 260/320 GHz, a high breakdown (HB) HBT with BV_{CEO} of 3.5V, 130nm RF CMOS, and a full suite of passive devices. Specific device results pertaining to this BiCMOS8XP technology are discussed in this paper.**

***Index Terms* — SiGe; BiCMOS; 130nm; mm-wave; HBT.**

I. Introduction

A high performance SiGe BiCMOS technology is essential to enable high speed digital logic, mixed signal circuits and millimeter-wave (mm-wave) analog ICs for applications in E-band backhaul, 60-100 gbps wireless telecommunication network, instrumentation, automotive radars, and mm-wave sensing and imaging [1]. In this article, BiCMOS8XP technology (8XP) is presented featuring a high-performance SiGe HBT demonstrating f_T/f_{MAX} > 260/320 GHz, a high-breakdown HBT with BV_{CEO}=3.5V and a rich menu of passive devices integrated with RFCMOS from IBM's 130nm RF CMOS technology CMRF8SF (8SF) [2].

8XP technology has been developed based on IBM's current BiCMOS8HP (8HP) technology [3]. The HBT integration flow is essentially unchanged with lateral and vertical scaling applied to meet bipolar performance requirements while preserving manufacturing compatibility with 130nm RF CMOS. A self-aligned emitter contact scheme further enhances performance.

In this paper, Section II discusses the 8XP technology overview. The HBT integration approach to achieve the performance targets is then described in section III. Finally, device results are presented in section IV.

II. Technology Overview

The 8XP technology is optimized to support mm-wave analog applications including high speed wireless and wireline telecommunication and imaging. These applications also incorporate increased amount of control circuitry, digital signal processing, built-in test functions and CMOS-based analog functions which require increased levels of CMOS density to remain affordable. IBM's 130nm RF CMOS technology was chosen as the base due to its rich and proven RF features and balance between integration density and process complexity/cost. Table I shows the device menu being developed as part of 8XP technology.

Table I. Device Description in 8XP Technology

Device	Nominal Values
Bipolar	
HP HBT ($f_T/f_{MAX}/BV_{CEO}$)	260/320 GHz / 1.7V
HB HBT ($f_T/f_{MAX}/BV_{CEO}$)	65/200 GHz / 3.5V
VPNP ($f_T/f_{MAX}/BV_{CEO}$)	17/22 GHz / 6.5V
FET	
Thin FET V_{DD}	1.2V
Thick FET V_{DD}	2.5V
FET Isolation	True Triple Well allowing NFET/PFET in an isolation
Passives	
N diffusion resistor	9 Ω/□
N+ diffusion resistor	77 Ω/□
P+ poly resistor	340 Ω/□
High R poly resistor	1700 Ω/□
TaN resistor	61 Ω/□
Thin/Thick Mos varactor	11/2 fF/μm^2
HA junction varactor	2 fF/μm^2
Single MIM	1 fF/μm^2
Dual MIM	3 fF/μm^2
Dual Metal Inductors	Standard / Symmetrical
Millimeter-wave passives	Single & Coupled microstrip / Co-planar transmission lines
Distributed passives	corners, bends, stubs, etc

Two bipolar transistors provide flexibility in meeting frequency and voltage tolerance requirements for several circuit applications. A selection of FET pairs provide flexibility in meeting digital performance and power

requirements in supporting multiple input/output (I/O) voltages and in implementing FET-based analog functions. Resistors, varactors, capacitors, and inductors comprise a rich menu of passive devices supporting design of analog circuits and transceiver blocks. Transmission lines and distributed passive devices support mm-wave design. Design of digital functions is facilitated through development of a standard-cell library, memory compilers and IO cells.

III. HBT Integration

8XP technology integrates SiGe HBTs with the 130nm CMOS process while maintaining the electrical characteristics of the CMOS devices. The integration scheme and the HBT structure employed in 8HP [3] were used as a starting point, with incremental changes and device scaling to improve HBT performance. Fig. 1 illustrates the base after gate BiCMOS integration scheme employed in 8XP [1]. Deep-trench isolation and buried subcollector are first formed, followed by the CMOS devices through gate formation. The CMOS devices are then protected, the HBTs are formed, followed by the source/drain junctions and the final anneal to activate the dopants. Modifications to the details of spacer formation and implant conditions are necessary to adjust the FET characteristics to match those of the 130nm low-power CMOS technology.

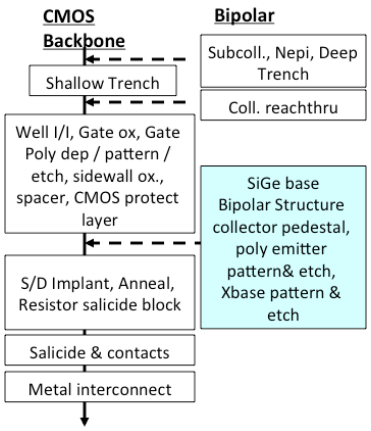

Fig. 1. Flow chart diagram depicting the BiCMOS scheme employed in 8HP and 8XP technologies.

Technology Computer-Aided Design (TCAD) was used to optimize the emitter polysilicon, SiGe base and collector doping profiles of the HBT. The TCAD methodology entailed the development of a calibrated model set to the relevant hardware data for the 8HP technology which features a 200/260GHz f_T/f_{MAX} NPN. The calibrated model set features close structural, diffused dopant profile and electrical data matches to electron micrographs, secondary-ion mass spectroscopy, scanning capacitance probe and DC/AC measurements. The calibration was subsequently utilized as the baseline for scaling the HBT to a higher AC performance level. An analysis of the simulated emitter-collector transit delay shows that the base transit time (T_b) and base-collector space charge region transit time (T_{bc}) were the major contributors to total delay in the 8HP HBT. Thus, these regions were the focus of device scaling to improve performance. Fig. 2a illustrates the changes which were made to the intrinsic device dopant profiles to achieve improved performance. These changes included reduction in the intrinsic base layer thickness, an increase in the Ge grade across the neutral base and an increase in the collector doping level. The simulated components of the transit time for 200GHz and 260GHz f_T performance level are shown in Fig. 2b. As mentioned earlier, an improvement in f_T was obtained by reducing the carrier transit times - T_b and T_{bc} .f_{MAX} was improved through reduction in parasitic base resistance by employing a self-aligned emitter-base contact scheme. Fig. 3 shows a schematic representation of the 8HP HBT structure and some of the focus areas for transistor scaling.

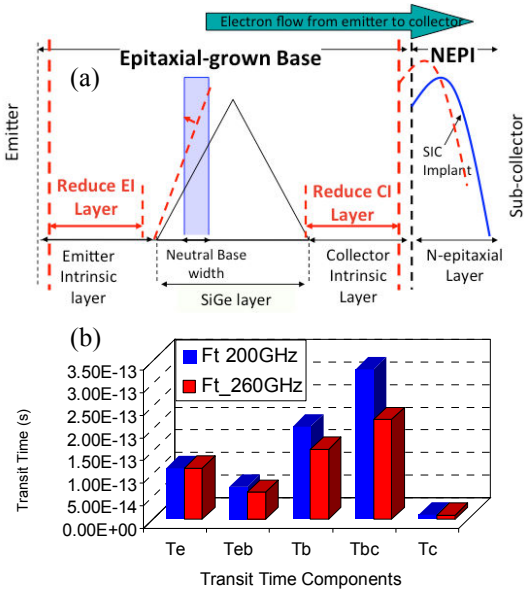

Fig. 2. Summary of TCAD simulations: (a) modulation in intrinsic dopant profile (b) simulated result of transit time components for 200 and 260GHz f_T

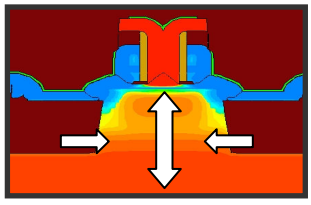

Fig 3. Highlights of the initial structural and device design changes to the HBT migrating from 8HP to 8XP technology.

IV. Device Characterization

A. HP and HB HBTs

Gummel plot of a typical HP HBT having emitter area of 0.12x2.5 μm^2 is shown in Fig. 4. Extracted f_T/f_{MAX} as a function of collector current at V_{CB}=0.3V is shown in Fig. 5. Peak f_T/f_{MAX} of 265/350GHz was obtained at a collector current density of 16mA/μm^2. f_T and f_{MAX} were extracted using extrapolations from -20dB/dec fit to the measured current gain H_{21} and Mason's Unilateral gain U with open-short de-embedding of the parasitic impedances associated with the pads and wiring. HP HBTs have a BV_{CEO} of ~1.7V and BV_{CBO} of 5.6V. Compared to 8HP, noise figure of HBTs in 8XP is lower by ~0.3dB due to improved base resistance (Fig. 6). This technology also co-integrates a HB HBT having BV_{CEO} of 3.5V, BV_{CBO} of 11.5V and f_T/f_{MAX} ~65/200GHz (at V_{CB}=1V).

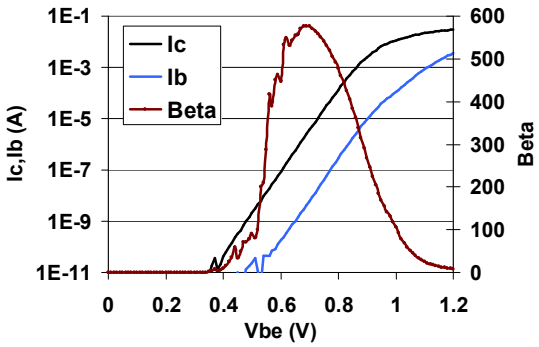

Fig. 4. Gummel plot and device beta for a typical HP HBT having emitter area ~0.12x2.5 μm^2 at V_{CB}=0V

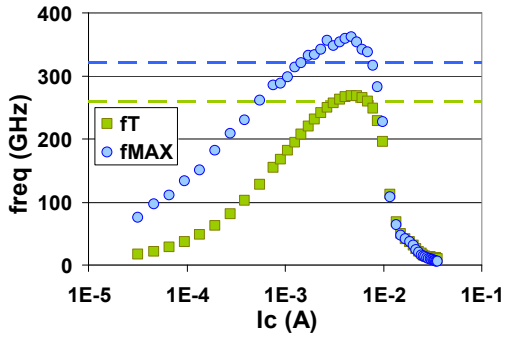

Fig. 5. Extracted f_T amd f_{MAX} at V_{CB}=0.3V for a typical HP HBT having emitter area ~0.12x2.5 μm^2. Peak f_T/f_{MAX} achieved is ~ 265/350 GHz for a target of ~260/320 GHz (dash lines)

B. CMOS

The CMOS base devices were selected considering both digital and RF performance. CMOS devices offered in this technology are based on IBM's foundry-compatible 130nm generation 8SF technology. Integration of SiGe HBT causes little to no FET parameter shift. The base CMOS is 1.2V with 0.12 μm drawn gate lengths. These FETs can optionally be coupled with either 2.5V I/O FETs using a dual gate oxidation process. Fig. 7 depicts equivalent I_{DSAT} vs. L_{EFF} of 1.2V NFET CMOS in 8XP and 8SF. This base device equivalent allows design IP migration from base CMOS technology. Triple well isolation can be used for floating logic relative to substrate improving noise isolation and device stacking for higher voltage signal handling.

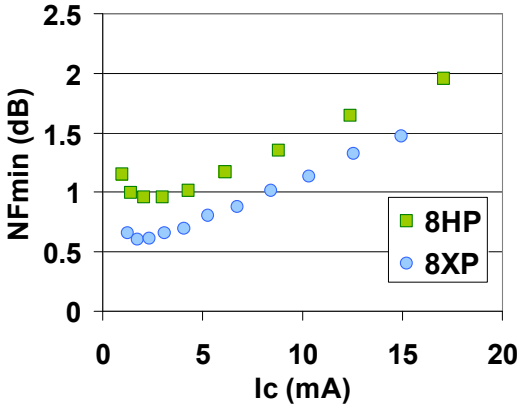

Fig. 6. Measured noise figure for a 18 μm long HP HBT showing a reduction in NF_{min} for 8XP compared to 8HP HBT. Data was taken at freq = 12GHz and V_{CE} = 1.35V

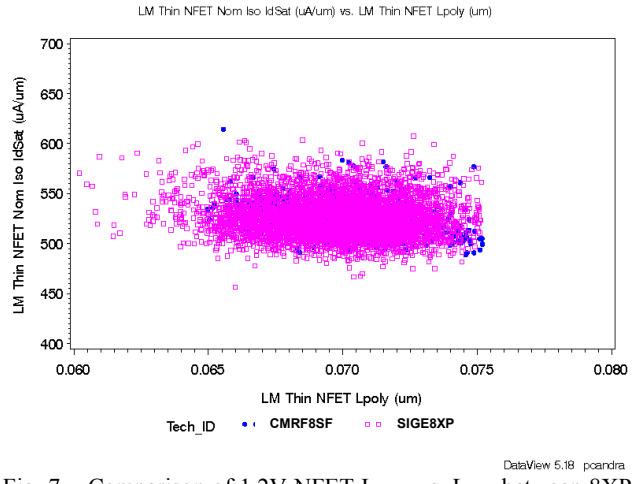

Fig. 7. Comparison of 1.2V NFET I_{DSAT} vs. L_{EFF} between 8XP and 8SF technologies

C. Millimeter-Wave elements

In order to facilitate mm-wave design, transmission lines and distributed passive devices are also supported in 8XP. This allows mm-wave designers to reduce the need for electromagnetic simulations. Fig. 8 shows a collection of transmission-line discontinuities that are modeled as discrete devices. Such elements have been used to design

complex mm-wave transceivers in 8HP [5] and are being implemented in 8XP. A Wilkinson power divider, combining a thin-film resistor, transmission lines, bends and tees is shown as an example. A 94GHz Wilkinson power divider was demonstrated in 8HP [6]. Measured versus simulated results are shown in Fig. 9.

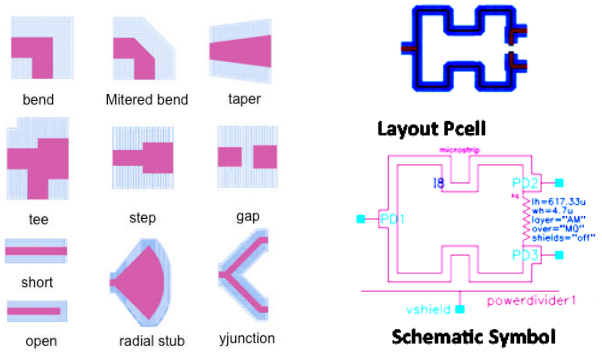

Fig 8. Layout views of selected primitive passive devices on left and the pcell and schematic symbol for the Wilkinson power divider hierarchical device.

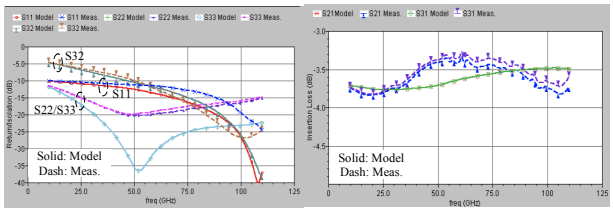

Fig. 9. Measured and simulated S- parameters of a 94GHz Wilkinson power divider implemented in 8HP. Top: Return loss and isolation, bottom: insertion loss

D. Through Silicon Via

To improve power amplifiers performance in SiGe BiCMOS technology, a grounded TSV is introduced in 8XP to reduce ground lead inductance in analog and mixed signal technologies [7]. The TSV is formed through the entire wafer and shorted on the back with a blanket wafer backside metallization as shown in Fig. 10.

V. Conclusion

A high performance SiGe HBT having f_T/f_{MAX} ~ 260/320GHz has been successfully integrated into IBM's 0.13µm RF CMOS to enable SiGe BiCMOS8XP technology. This technology also supports a high breakdown HBT with f_T/BV_{CEO} = 65GHz/3.5V and a rich menu of passive devices to enable high performance mm-wave designs targeted towards high speed wireless and wireline telecommunication and imaging applications.

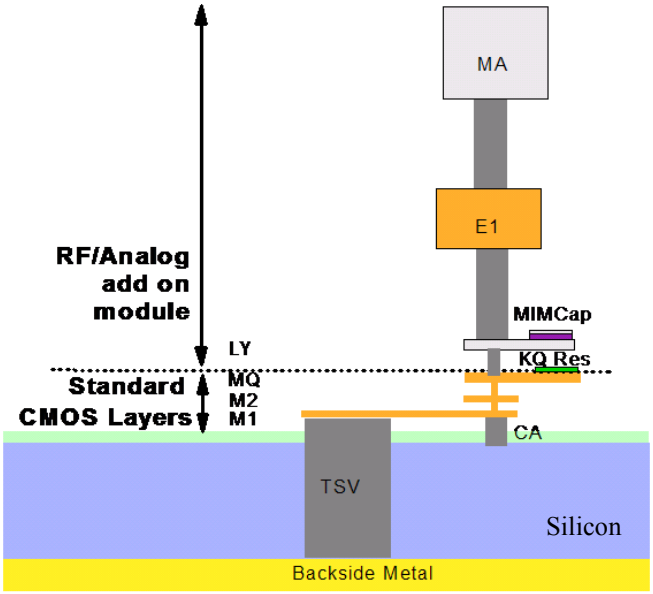

Fig. 10. Schematic cross-section of a TSV formed through the entire wafer and shorted on the back with a blanket wafer backside metallization

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