A 65 GHz LNA/Phase Shifter With 4.3 dB NF Using 45 nm CMOS SOI

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***Abstract*—This letter presents the first 45 nm CMOS SOI LNA/phase shifter for 60 GHz applications. The 3 b phase shifter is designed using a switched-LC approach and results in only 6 dB loss at 65 GHz. The LNA/phase shifter front-end results in a gain of 6.5 dB, a noise figure of 4.3 dB, and an input $P_{1\,\mathrm{dB}}$ of -13.5 dBm (limited by the amplifier) with a power consumption of 15 mW. This work shows that advanced CMOS processes are essential for low power, medium linearity 60 GHz phased arrays.**

***Index Terms*—45 nm CMOS, low noise amplifier (LNA), millimeter-wave, phase shifter.**

I. Introduction

SILICON-based 60 GHz phased array systems using the all-RF architecture have been investigated for short-range Gbps communication links [1], [2]. They have also been demonstrated at 35–85 GHz for satellite communications and automotive radars [3]. Two main designs have emerged for the phase shifter: The vector modulator [4] and switched-LC networks [5]. The vector modulator allows for design flexibility, but results in increased power consumption for high linearity and a high NF (larger than 12 dB) since it uses two amplifiers and a lossy I/Q network. On the other hand, the switched-LC approach suffers from high loss and NF due to the non-ideal CMOS switches in the 130 nm or 90 nm CMOS nodes, but has a power handling of 7–12 dBm depending on the CMOS node. Therefore, high-gain amplifiers are used in front of both phase shifter types, which results in either an input $P_{1\,\mathrm{dB}}$ of -30 to -20 dBm (for low power operation) or high power consumption for an input $P_{1\,\mathrm{dB}}$ of -15 to -10 dBm.

Recently, 45 nm CMOS SOI amplifiers, doublers and switches have been demonstrated with excellent performance up to 200 GHz [6], [7]. This letter presents a 65 GHz CMOS SOI switched-LC phase shifter with low insertion loss, and shows that 65 GHz phased array front-ends can be designed with low power consumption and high linearity.

II. Design

The LNA and phase shifter are designed using the IBM 45 nm CMOS SOI process (Fig. 1). The inductors are implemented using G-CPW transmission lines except the 175 pH spiral inductor in the LNA, and the capacitors are standard IBM-library vertically stacked interdigitated metal finger caps (MFCs). The G-S-G RF pads, LNA and each phase shifter bit are designed with 50 Ω input and output impedances. A full-wave EM solver, Sonnet [8], is used to simulate all the transmission lines, interconnections and pads.

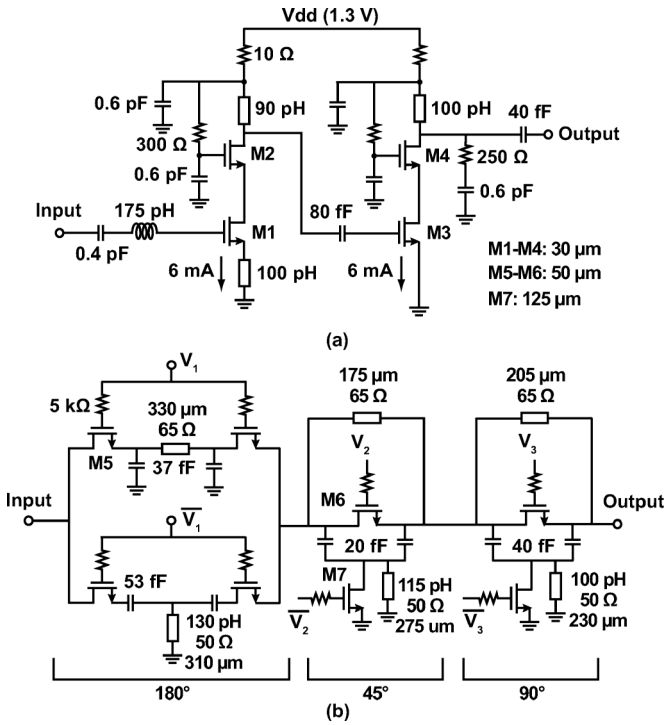

Fig. 1. Schematic of the V-band (a) LNA and (b) 3 b phase shifter.

The LNA is a two-stage cascode amplifier with emitter degeneration for simultaneous noise and power matching [Fig. 1(a)]. 30 μm wide floating-body transistors with 1 μm finger width are used. 10 Ω resistors are placed at the Vdd node for stability considerations, and do not affect the LNA, except the 60 mV voltage drop. A resistor of 250 Ω is used to result in a wide-band output impedance match. The measured LNA peak gain is 12.5 dB with a NF of 4.0 dB at 65 GHz [9]. The measured output 1 dB power compression point ($OP_{1\,\mathrm{dB}}$) is -2 dBm.

The 3 b phase shifter consists of cascaded 180°, 45° and 90° phase shifting elements (Fig. 1(b)). The 180° phase shifter is designed using switched high-pass/low-pass networks [2]. The high-pass T-network results in a 90° phase lead, and consists of two series capacitors (53 fF) and a shunt transmission line (130 pH), whereas the low-pass π-network results in a 90° phase lag and consists of an inductive transmission line ($Z_0 = 65\ \Omega$, $l = 330\ \mu$m) and two shunt capacitors (37 fF). The 90° and

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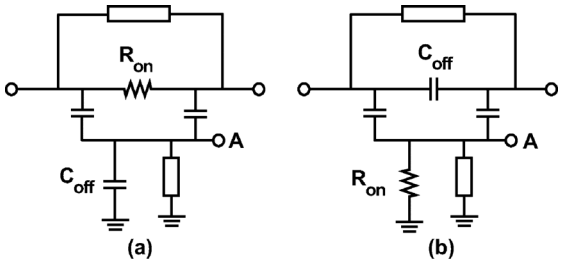

Fig. 2. Equivalent circuit model of the 45°/90° phase shifters in the (a) bypass and (b) phase-delay states.

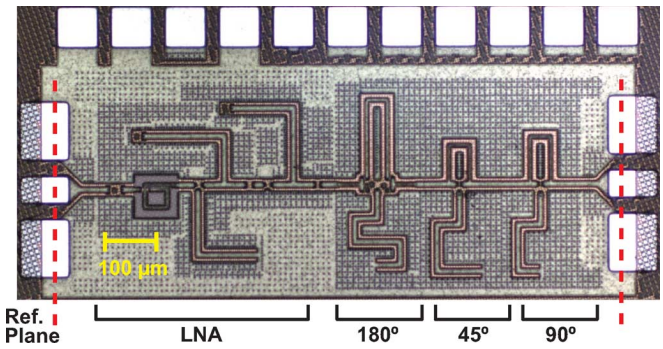

Fig. 3. Microphotograph of the LNA/phase shifter.

45° phase shifters employ low-pass π-networks, and are based on switching between a phase delay and a bypass state. When M6 is on and M7 is off, the M7 off-state capacitance (C_{off}) resonates with the shunt transmission line and creates an open-circuit at node A (Fig. 2). The M6 on-resistance (R_{on}) therefore results in a bypass state. When M6 is off and M7 is on, the series transmission line together with the two shunt capacitors form a low-pass network, which results in a phase delay. Gate bias resistors of 5 kΩ are used for all switches in order to prevent the RF signal leakage through the gate bias lines.

A low R_{on} is desired for the shunt switch (M7) so that the CLC π-network in the phase-delay state results in low loss and accurate phase delay. At the same time, the impedance at node A needs to be high in the bypass state, and this is achieved by resonating M7 C_{off} with an inductor. A shunt switch transistor width of 125 μm (50 $\times$2.5 μm, $R_{on} = 2.8\,\Omega$ and $C_{off} = 62$ fF) is therefore chosen in this design. For the 90° and 45° phase shifters, the inductor values are 100 pH ($X = 38\,\Omega$) and 115 pH ($X = 43\,\Omega$) respectively, with a Q of 13 at 60 GHz. The loss in the 90° and 45° phase delay states is mostly determined by the transmission-line Q and two shunt capacitors, and is typically 1–1.5 dB at 60 GHz. In the bypass state, the loss is determined by the series switch loss, and is 2–3 dB at 60 GHz in a bulk CMOS technology. This creates a gain error between the bypass and phase delay states. However, in an advanced SOI CMOS process, the gain error could be minimized by choosing a wide series switch transistor without incurring a large substrate capacitance. Therefore, a transistor width of 50 μm (20 $\times$2.5 μm, $R_{on} = 7\,\Omega$ and $C_{off} = 25$ fF) is chosen for the series switch (M6) which results in a loss of 1–1.5 dB for the 45° and 90° phase states.

Fig. 3 presents the LNA/phase shifter chip photograph (0.55 $\times$ 1.2 mm^2 including the pads).

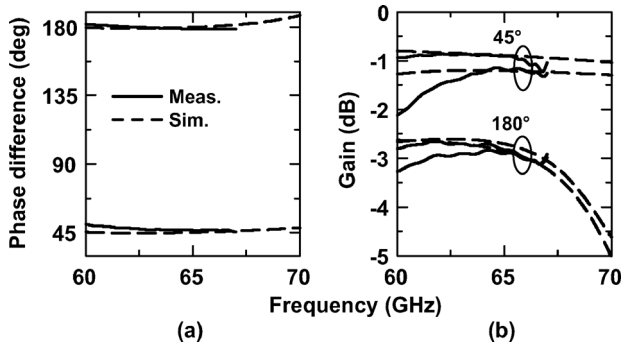

Fig. 4. Measured and simulated (a) phase difference and (b) gain of 180° and 45° phase shifter test-cells.

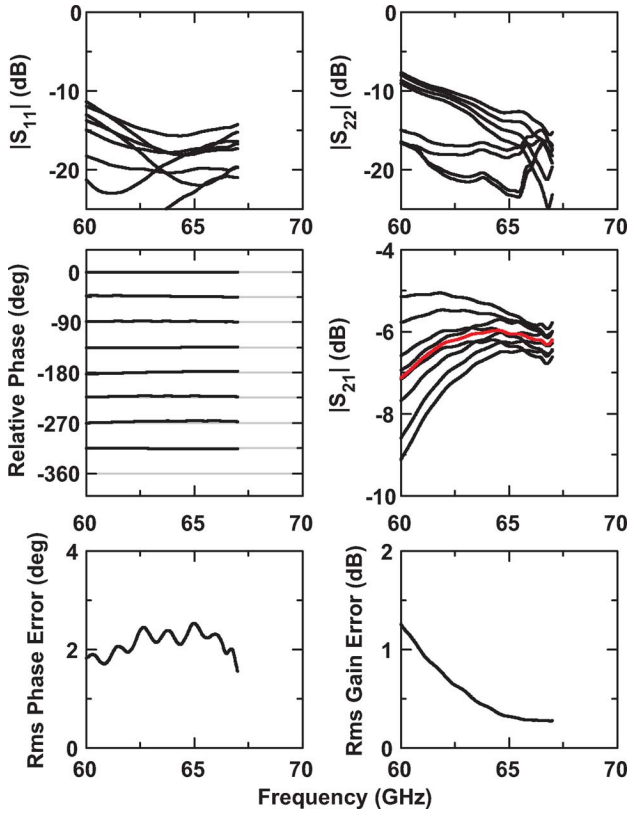

Fig. 5. Measured S_{11}, S_{22}, S_{21}, relative phase, rms phase error and rms gain error of the 3 b phase shifter.

III. Measurements

The 3 b phase shifter was measured on-chip with an Agilent E8361 67 GHz PNA using SOLT calibration to the probe tips. Fig. 4 presents the simulated and measured phase difference and the insertion loss of individual 180° and 45° phase shifting cells. The measured insertion loss of the 45° and 180° phase shifters are 0.9–1.2 dB and 2.8–2.9 dB, respectively, at 65 GHz.

Fig. 5 presents the measured 3 b phase shifter. The input return loss is less than -10 dB at $60 - 67^{+}$ GHz, and the output return loss is less than -8 dB at $60 - 67^{+}$ GHz. The measured loss of the 3 b phase shifter is 6.0 ± 0.5 dB at 65 GHz, and the average loss is 6.0 dB (red curve in Fig. 5). The measured RMS gain error is 0.3 dB at 65 GHz and is less than 1.3 dB at $60 - 67^{+}$ GHz. The measured RMS phase error is less than 2.5° at $60 - 67^{+}$ GHz. The measured input $P_{1\,\mathrm{dB}}$ is about 6 dBm, and is relatively constant versus frequency and phase state (Fig. 6).

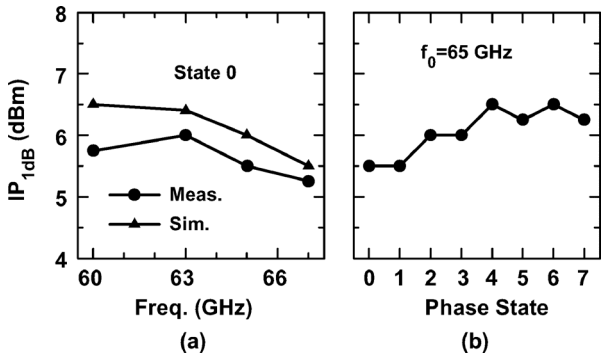

Fig. 6. Measured and simulated input $P_{1\,\mathrm{dB}}$ of the 3 b phase shifter versus (a) frequency and (b) phase state.

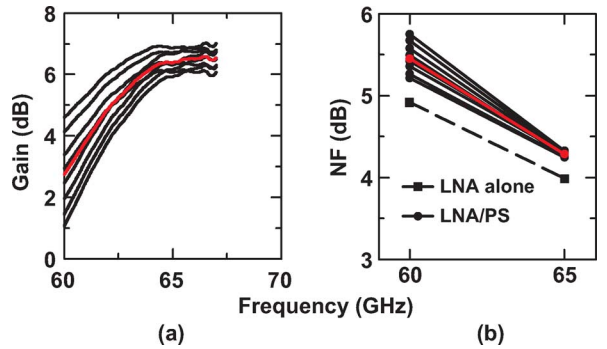

Fig. 7. Measured (a) gain and (b) noise figure of the LNA/phase shifter for different phase states. The red curve is the average of all phase states.

TABLE I
LNA/PHASE SHIFTER COMPARISON

	This Work	[4]	[1]*	[10]*
Technology Node	45-nm CMOS	90-nm CMOS	65-nm CMOS	65-nm CMOS
Frequency (GHz)	60–67$^+$	53–65	57–62	58–64
Rms gain error (dB)	$<$1.3	N/A	$<$1.7	$<$1.3
Rms phase error (degrees)	$<$3	N/A	$<$12	$<$8
Peak Gain (dB)	6.5	12.5	25	12
NF (dB)	$<$5.5	$<$7.5	N/A	$<$8.5
IP_{1dB} (dBm)	–13.5	–13.3	–21.5	–16
Power Consumption (mW)	15	60	45	78
Phase Shifter Topology	3b passive	5b active	4b passive	4b active

*1-element of the receiver phased array.

The input $P_{1\,\mathrm{dB}}$ of the phase shifter is high enough so as not to limit the overall $P_{1\,\mathrm{dB}}$ when preceded by an LNA.

The measured average gain and NF of the LNA/phase shifter is 6.5 dB and 4.3 dB, respectively at 65 GHz (Fig. 7). The cascaded NF is only degraded by 0.3 dB since the phase shifter has low loss. The measured 3 dB bandwidth of the LNA/phase shifter is 59.5–61.6 (about 60.6) to 67$^+$ GHz for different phase states. The overall input $P_{1\,\mathrm{dB}}$ is limited by the LNA, and is -13.5 dBm at 65 GHz.

The LNA and phase shifter were designed at 60 GHz, but the measured results show that the center frequency shifted to 65 GHz for both designs. Although parasitic RC extraction and full electromagnetic simulations were employed, this 8% frequency shift could be due to inaccurate transistor models since the CMOS models are mostly for digital designs. The results at 65 GHz are still state-of-the-art and show the validity of the design. Table I summarizes this work and compares the results with other LNA/phase shifter designs [10].

IV. CONCLUSION

A 65 GHz 3 b phase shifter with an integrated LNA is presented. The LNA/phase shifter achieves a gain of 6.5 dB, a noise figure of 4.3 dB and an input $P_{1\,\mathrm{dB}}$ of -13.5 dBm at 65 GHz with only 15 mW dc power consumption. The RMS phase and gain error is less than 2.5° and 1.3 dB at $60-67^+$ GHz.

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