A 65 nm CMOS 4-Element Sub-34 mW/Element 60 GHz Phased-Array Transceiver

Maryam Tabesh, *Student Member, IEEE*, Jiashu Chen, Cristian Marcu, *Student Member, IEEE*, Lingkai Kong, *Student Member, IEEE*, Shinwon Kang, *Student Member, IEEE*, Ali M. Niknejad, *Senior Member, IEEE*, and Elad Alon, *Member, IEEE*

***Abstract*—This paper describes a low power and element-scalable 60 GHz 4-element phased array transceiver implemented in a standard 65 nm CMOS process. Using a 1.2 V supply, the array consumes <34 mW/element including LO synthesis and distribution. Energy and area efficiency are achieved by utilizing a baseband phase shifting architecture, holistic impedance optimization, and lumped-element based design. Each receiver (RX) element provides 24 dB of gain with an average noise figure (NF) of 6.8 dB while the total saturated output power of the transmitter (TX) is 4.5 dBm. The array achieves 360° of phase shifting range with a worst-case measured phase resolution of 6 bits (TX)/ 5 bits (RX) while maintaining amplitude variations less than ±0.5 dB.**

***Index Terms*—Baseband phase shifting, beam steering, CMOS, energy efficient array, low noise amplifier (LNA), low power, millimeter wave integrated circuits, phase-locked loop (PLL), phased-array, power amplifier (PA), 60 GHz transceiver.**

I. Introduction

DUE to the availability of 7 GHz of unlicensed bandwidth, the 60 GHz band provides an attractive solution for multi-Gb/s short range communication [1]–[6]. Commercial solutions in silicon for wall-powered applications are now available [7]. Portable devices, e.g., mobile phones and tablets, are much more sensitive to system cost and energy efficiency compared to non-mobile devices. This represents an important challenge in the realization of an integrated 60 GHz solution suitable for such low power mobile applications.

Energy and area efficient phased array transceivers are key to enabling such multi Gb/s communications in mobile devices at 60 GHz. Phased arrays enable beam-steering, which provides an agile means of overcoming path-loss, fading, and security issues, as well as allowing spatial power combining in order to ease the design of the power amplifier at mm-wave frequencies [8]–[12]. An N element phased array solution (on both the transmitter and the receiver) improves the link budget by a factor of N^2 on the transmitter due to coherent spatial combining and by a factor of N on the receiver due to improved signal to noise ratio. This overall N^3 improvement in the budget is critical in overcoming the large inherent path loss at the 60 GHz carrier frequency.

Despite the low gain of CMOS at mm-wave frequencies, lower manufacturing costs and higher integration can be achieved compared to other semiconductor processes. Integrating the RF with baseband (BB) and Built-In-Self-Test (BIST) circuitry significantly reduces assembly and testing costs, which at mm-wave can dominate the overall costs of the final system.

Although significant progress has been made in the design of silicon based phased arrays, current implementations at mm-wave frequencies have not yet simultaneously achieved sufficient performance and area/power efficiency. For example, in [8] and [10] an integrated 16 element phased array transmitter and receiver were implemented in a 0.12 μm SiGe process with excellent performance, but the power consumption of these designs (which were targeted to support video streaming with the wirelessHD standard) is too high for portable devices. As another example, [9] demonstrated the lowest power CMOS phased array transceiver to date using an RF phase shifting architecture. However, this low power consumption was obtained at the expense of somewhat reduced per-element performance (e.g., gain, noise figure, and output power).

In this paper we therefore describe a scalable, integrated 4 element BB-phase shifting transceiver implemented in a 65 nm standard CMOS process that achieves high level of performance per-element while maintaining low area and power consumption. By utilizing essentially the entire available bandwidth (BW) at 60 GHz as a single channel, this transceiver was designed to allow 10 Gbps communication using QPSK modulation. The transceiver consumes 137 mW in both transmit and receive modes. In Section II we review the tradeoffs leading to the choice of a baseband phase shifting architecture for the array. Section III describes the techniques used in the transmitter to achieve high energy efficiency in both the baseband and RF domains. Section IV discusses the design of the mm-wave receiver and proposes impedance scaling for improved power consumption. Section V describes the challenges and proposed solutions for low-power LO generation and distribution given the baseband phase-shifting architecture. Finally, measured results for the entire transceiver are presented in Section VI, followed by concluding remarks in Section VII.

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M. Tabesh, J. Chen, L. Kong, S. Kang, A. M. Niknejad, and E. Alon are with the University of California, Berkeley, CA 94704-1302 USA (e-mail: tabesh@eecs.berkeley.edu; jiashuc@berkeley.edu; konglk@eecs.berkeley.edu; shinwon@eecs.berkeley.edu; niknejad@eecs.berkeley.edu; elad@eecs.berkeley.edu).

C. Marcu is with Qualcomm Atheros, San Jose, CA 95110 USA (e-mail: cmarcu@gmail.com).

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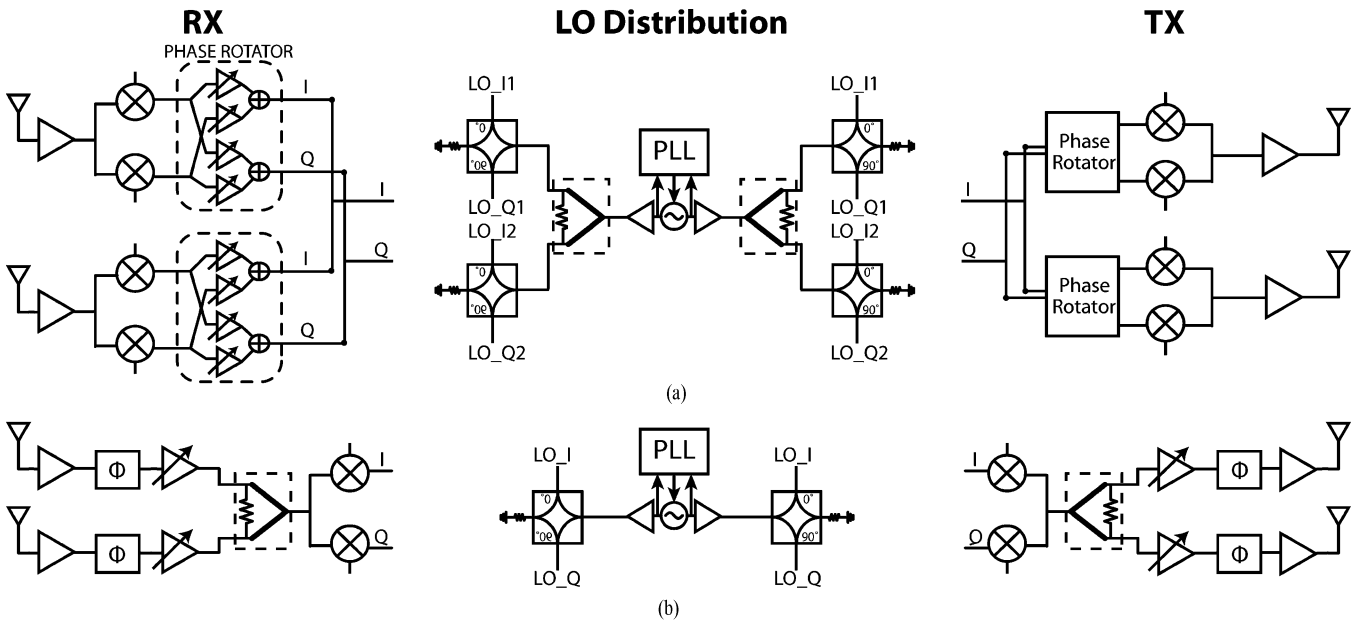

Fig. 1. Block diagram of 2-element RX, LO distribution, and TX for (a) BB phase shifting and (b) RF phase shifting architectures.

II. MM-Wave Phased-Array Architectural Choices

Multiple architecture choices are available for the implementation of integrated phased arrays. The two main choices considered in this section are RF and BB phase-shifting architectures (Fig. 1(a) and (b)). Both topologies require some form of phase-shifting as well as mm-wave combining or splitting. Phase shifters at RF tend to be large and can introduce substantial losses on RF signal paths, leading to lower output power at the TX and higher NF in the RX. Besides lower losses [13], phase shifting at baseband can achieve improved phase resolution, leading to better control over null placement and depth [14], [15] as well as the ability to perform more precise calibration in order to correct for various impairments.

In an RF architecture, splitting and combining happens at the carrier frequency on the signal path, whereas the baseband architecture has mm-wave splitters on the LO path and IF frequency combiners/splitters. The loss and variation of this mm-wave combining and splitting network are generally easier to tolerate in the LO distribution due to the lower bandwidth of the signal as well as the observation that the overall performance of the transceiver is less sensitive to the amplitude on the LO path as compared to the signal path (as long as the LO amplitude is sufficiently large).

On the transmitter side (as shown in Fig. 1), the power amplifiers (PA) themselves are equivalent in both architectures. However, all else held fixed, the PAs in the RF phase shifting architecture are provided with lower input power (and hence lower equivalent isotropically radiated power (EIRP) for fixed PA gain) due to the loss of the phase shifters preceding the PA. Also, for a similar power delivered to the PA, the splitter in the RF architecture necessitates larger mixers to deliver more power to the RF network. In the BB architecture, the mixer sizes can be down-scaled proportionally to achieve the same RF power per element.

Besides the means by which phase shifting is achieved, the other architectural decision on the transmitter is related to the choice of the number of elements for a required EIRP. The required EIRP and the effective transmitter efficiency are given by

$$EIRP_{required} = N^2 P_{out/El} \tag{1}$$

$$\eta_{overall} = \frac{N^2 P_{out/El}}{N P_{DC/El}} = N\eta_{El} \tag{2}$$

where N is the number of elements and η_{El} is the efficiency per element.

For the same EIRP, we can either scale up the number of elements (smaller $P_{out/El}$) or the output power of each PA. Given that due to spatial power combining, the TX EIRP improves by N^2 while the DC power only scales with N, it is often beneficial to use a larger number of elements for better overall efficiency (2). However, increasing the number of TX elements is generally limited by one of the following factors: footprint limitations on using larger antenna arrays, the overhead power in the TX path eventually dominating the overall power as the output power of each PA is reduced, and finally the degraded efficiency of each PA as the output power is reduced to the level where the losses from the impedance transformation network (required to interface the high impedance levels of a low-power PA to 50 Ω antennas) dominate.

Returning to the choice of phase shifting implementation, a similar argument holds for the comparison of the two architectures on the receiver. As shown in Fig. 1, similar low noise amplifiers (LNA) are used, but the mixers in the BB architecture can be scaled in device size since they are working with smaller (desired) signal power levels. We will also assume that the RF VGA and BB phase rotators will have similar power consumption and limitations. The noise figure of a single path in the RF

architecture can be described by:

$$F_{RF} = F_{LNA} + \frac{L_\phi^{-1} - 1}{G_{LNA}} + \frac{F_{VGA} - 1}{G_{LNA} L_\phi} + \frac{F_{mixer} - 1}{G_{LNA} \underbrace{L_\phi G_{VGA}}_{\approx 1}}. \quad (3)$$

While the same path in the BB architecture has a noise figure of:

$$F_{IF} = F_{LNA} + \frac{F_{mixer} - 1}{G_{LNA}} + \frac{F_{rot} - 1}{G_{LNA} G_{mixer}}. \quad (4)$$

In the calculations it should be noted that the noise of the mixer in the RF architecture directly adds to the RF paths when input referred and is not divided by the number of elements. This is due to the uncorrelated noise signals at the input of the Wilkinson power combiner.[1] The analysis shows that the noise figures of the two topologies are similar, with the BB topology perhaps being slightly better. While the RF architecture suffers from higher noise due to lossy phase shifters and the compensating VGA (the second and third terms in (3)), the mixer noise component is larger in the BB topology due to reduced device sizes.

Finally, in the receiver, the RF power *combiner* of the RF architecture is replaced by an RF *splitter* on the LO path. The splitter requires extra buffers to overcome power split loss in addition to power consumption from large signal drive of the splitting network. Therefore, to get the full advantages of using the BB architecture, the design of a low power LO distribution network including quadrature phase generation is critical. In Section V we show that this network can be designed to meet these requirements.

One of the perceived advantages of the RF phase shifting architecture is superior linearity. Since spatial power combining occurs in the RF domain, the mixer is relieved from handling large signal blockers that generally originate from different spatial directions. Nevertheless, due to the losses of the passive RF phase shifters, maintaining low noise figure requires that buffer amplifiers be placed after the LNA, and these buffer amplifiers will therefore limit the linearity. Similarly, if an active RF phase shifter is used, the variable-gain amplifiers within the active phase shifter will determine the linearity of the front-end. In a BB phase shifting architecture, the mixers in each element can be decomposed into an active block and a passive current (or voltage) commutating block. The active block plays a similar role as the buffers or VGAs in the RF phase shifters, so that the overall linearity is roughly comparable in both architectures.

It should be noted that an LO phase shifting mm-wave phased-array architecture is also possible [11]. While this architecture eliminates phase shifters in the signal path, high frequency phase shifters (or phase rotators) and an LO distribution network are still needed. Furthermore, it also requires quadrature downconversion mixers per path (just like BB phase shifting) and overall this architecture does not offer a substantial advantage over the alternatives for low power phased-array design.

[1]Note that Wilkinson power combiners are used since typical voltage or current summation structures will lead to significant coupling and interactions between the elements, making such an approach unattractive from a scalability standpoint.

Given that at a high level a BB phase shifting architecture can achieve performance and power comparable to that of the more traditional RF phase shifting architecture, the transceiver described in this paper utilizes BB phase shifting in order to leverage its improved phase control and accuracy. A block diagram of the demonstrated phased-array transceiver – which includes 4 RX elements, 4 TX elements, integrated BB phase rotators, VCO/PLL, and LO distribution network – is shown in Fig. 2. In the following sections we describe each of the major sections of the transceiver in further detail.

III. Transmitter

Fig. 3 shows a block diagram of each transmitter element. It consists of a 7-bit resolution baseband phase rotator, a double-balanced quadrature Gilbert mixer, and a zero-voltage-switching power amplifier. In a relatively low output power transmitter, the overall efficiency is often not dominated by the PA, but rather by the other required blocks in the transmitter chain that can each contribute to a significant portion of the total power consumption. Therefore, optimizing the efficiency of every block in the transmitter is critical to achieving low total per-element power; the techniques we have utilized to achieve this goal are described in the following subsections.

A. Phase-Rotating Quadrature Mixer

Maximizing the current efficiency of the mixer is critical not only in reducing the mixer power, but also in maximizing the impedance at the LO ports in order to reduce the required LO buffer current swing. Combining the baseband phase rotator and the quadrature mixer into a single structure is attractive since the bias current can be reused.

In such a combined rotator/mixer structure, the conventional means to achieve phase rotation functionality is to current sum the weighted initial I and Q signals, as illustrated in Fig. 4(a). Unfortunately however, this architecture suffers from relatively low efficiency. To gain insight into the root cause of this poor efficiency, consider the current efficiency of the phase rotator, which is defined as the ratio of the effective differential output current magnitude to the total DC current:

$$\eta_{old} = \frac{\sqrt{I'^2 + Q'^2}}{2(\cos(\theta) + \sin(\theta))} = \frac{\sqrt{I^2 + Q^2}}{2(\cos(\theta) + \sin(\theta))} = \frac{1}{\sqrt{2}(\cos(\theta) + \sin(\theta))} \quad (5)$$

where the final equality is due to the fact that $\mathrm{I/Q}$ values are either 1 or -1 for QPSK modulation. Note that the efficiency falls between 50% to 71% depending on phase rotation angle θ, which significantly limits the overall efficiency of the complete mixer/rotator structure.

The low efficiency of traditional phase rotation is further explained by an example shown in Fig. 4(b). At 45° phase rotation angle (where both initial $\mathrm{I/Q}$ inputs are equal to 1), one pair of the cosine and sine current appears at the output as common-mode signals to achieve an effective I magnitude of zero. In other words, half of the total current is wasted due to the current-mode subtraction inherent in this structure.

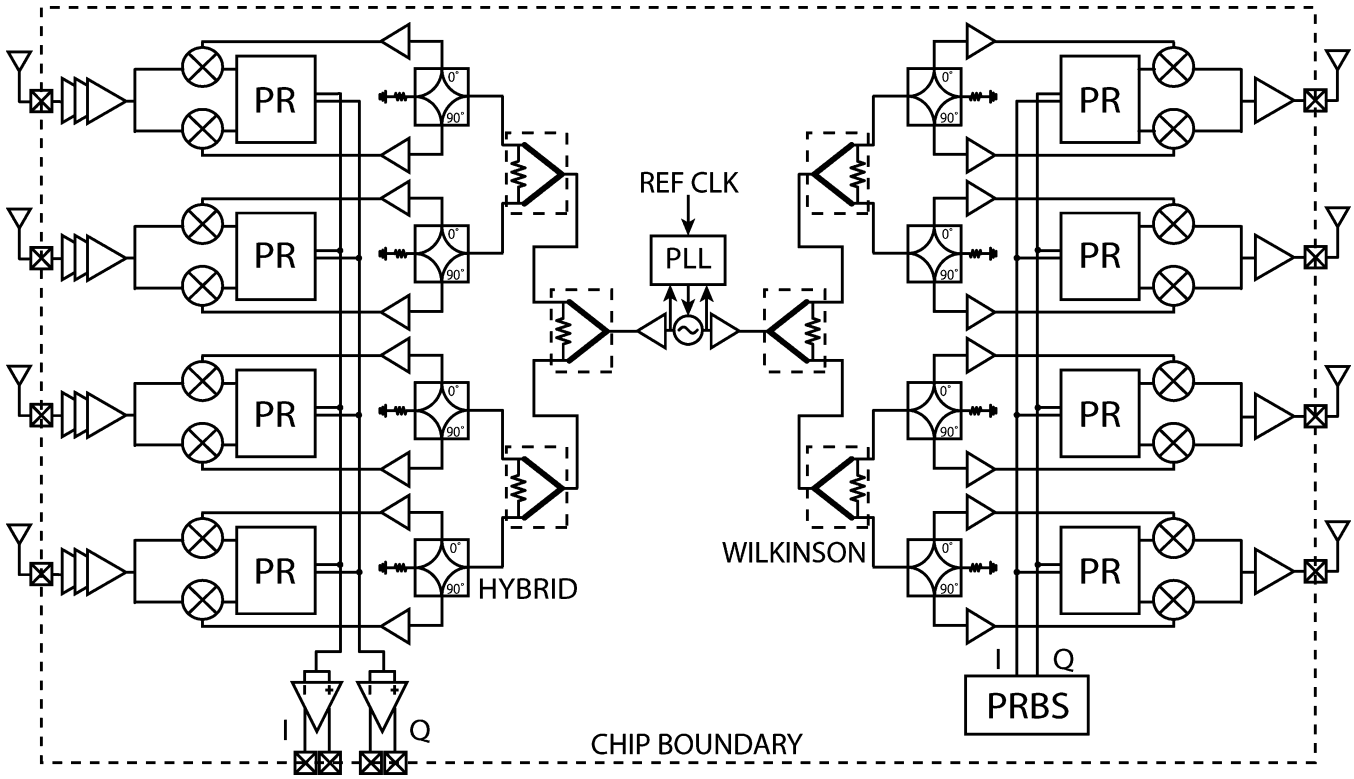

Fig. 2. Block diagram of the 4-element BB phased-array transceiver.

To increase the current efficiency, an improved baseband phase rotator architecture is proposed in Fig. 5. In the proposed architecture, only two current sources are used. Instead of carrying $\cos(\theta)$ and $\sin(\theta)$ weightings, these current sources carry $\cos(\theta + 45^\circ)$ and $\sin(\theta + 45^\circ)$ weightings, representing the magnitude of the phase-rotated $\mathrm{I/Q}$ signals. Depending on which quadrant the final phase-rotated data lands, the $\cos(\theta + 45^\circ)$ weighting will represent either the I' signal or the Q' signal. Since the final modulated RF signal's quadrant depends on both the baseband data quadrant and the phase rotation angle, eight current distribution switches are used to dynamically distribute the two current sources to the appropriate $\mathrm{I/Q}$ output ports.

The proposed design reduces the DC current compared to a conventional design, resulting in a new current efficiency of:

$$\begin{aligned}\eta_{new} &= \frac{\sqrt{I'^2 + Q'^2}}{\cos(\theta + 45^\circ) + \sin(\theta + 45^\circ)} \\ &= \frac{\sqrt{\cos^2(\theta + 45^\circ) + \sin^2(\theta + 45^\circ)}}{\cos(\theta + 45^\circ) + \sin(\theta + 45^\circ)} \\ &= \frac{1}{\cos(\theta + 45^\circ) + \sin(\theta + 45^\circ)}. \end{aligned} \tag{6}$$

Note that the new efficiency falls between 71% and 100%, a significant improvement compared to the conventional approach. Fig. 6 plots the efficiency comparison for different phase rotation angles; the new architecture is superior to the conventional one at all angles, with an average improvement of roughly 40%.

As previously mentioned, the quadrant of the output RF signal depends upon both the baseband data quadrant and the phase rotation angle. The current distribution switches S1-S8 are therefore controlled by the baseband input quadrant information (Quad1 to Quad4), which are computed from the original $\mathrm{I/Q}$ signals, and the sign bits of the 7-bit phase rotation control, as illustrated in Fig. 3. The truth table of the quadrant signals and the correspondence between the two sign bits and the phase rotation region are shown in Tables I and II. At each clock sampling point, only one of the four switches (S1 to S4) connected to the I mixer is turned on while the others remain off. The same principle applies to the four switches (S5 to S8) connected to the Q mixer. The current sources are implemented using 5-bit DACs with the upper 4 bits thermometer encoded.

The phase rotated baseband signals are fed into two double-balanced mixers for quadrature upconversion. Since the sizes of the Gilbert quad switches set the driving requirement for the LO buffers, smaller size transistors are preferred to increase the input impedance and reduce the buffer power consumption. Due to reduced phase rotator current, 10 μm transistors are used, resulting in a small-signal differential input impedance of 1.2 $\mathrm{k}\Omega$. With a differential input swing of 600 mV (peak voltage), the required LO input power is kept below -8 dBm. The outputs of the two double-balanced mixers are current combined before feeding to the transformer used for coupling the PA and the mixer. The power consumption of the phase rotator/mixer varies between 6–8.75 mA depending on the phase rotation setting.

B. Zero-Voltage-Switching PA

Since QPSK modulation has relatively small peak-to-average power ratio (PAPR), this enables the use of a zero-voltage-switching (ZVS) amplifier for improved efficiency. The most popular switching class for relatively high

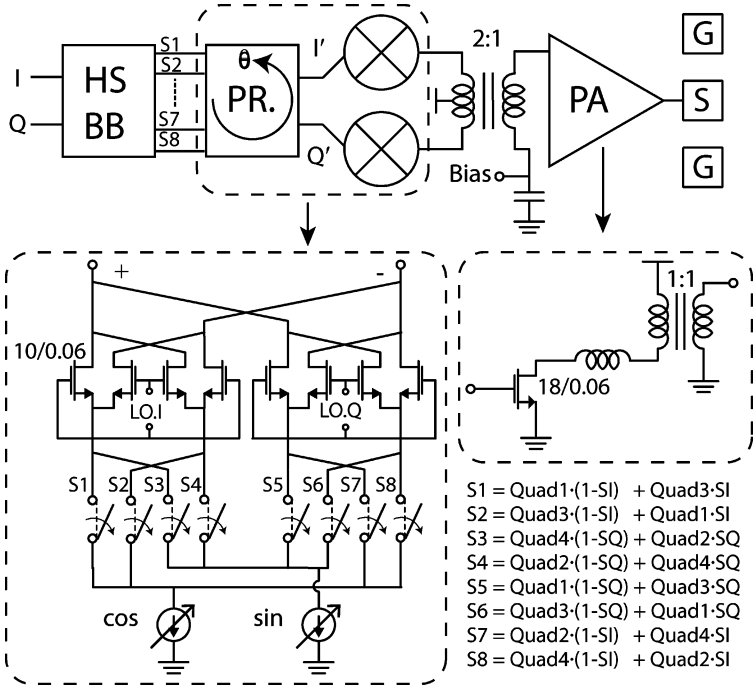

Fig. 3. Schematic of one transmitter element.

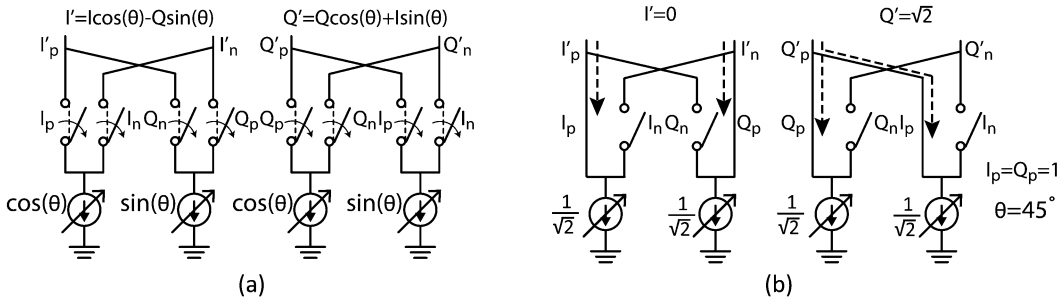

Fig. 4. Schematic of the conventional BB phase rotator architecture.

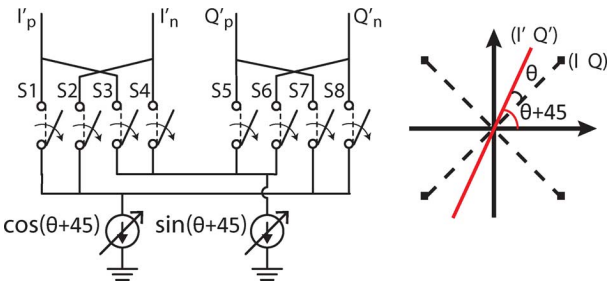

Fig. 5. Schematic of the proposed BB phase rotator architecture.

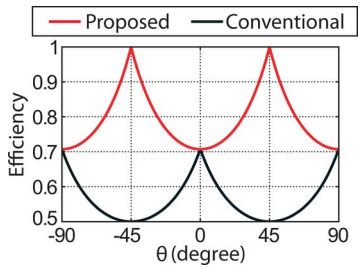

Fig. 6. Efficiency comparison of the conventional and proposed phase rotator.

frequency modulation is Class-E since the topology can absorb the transistor drain parasitic capacitance as part of its output tuning network. Although abundant work has been done on Class-E amplifiers, adopting this class for mm-wave designs is extremely challenging. This is mainly because the capacitance tolerance of Class-E amplifiers reduces linearly with frequency. With the same output power level, much smaller transistors are allowed at high frequency, therefore resulting in increased on-resistance loss.

One way to increase the capacitance tolerance and improve the efficiency is to utilize harmonic tuning [16]. Adding higher harmonics beyond the second has diminishing returns in efficiency improvement but results in more complexity (and hence additional passive loss) in implementing the on-chip tuning network, and therefore this design only involves second harmonic tuning.

Fig. 7 shows the simulated V-I waveform of the PA as well as the predicted drain efficiency, power gain, and power added efficiency (PAE) of the core PA as a function of the normalized

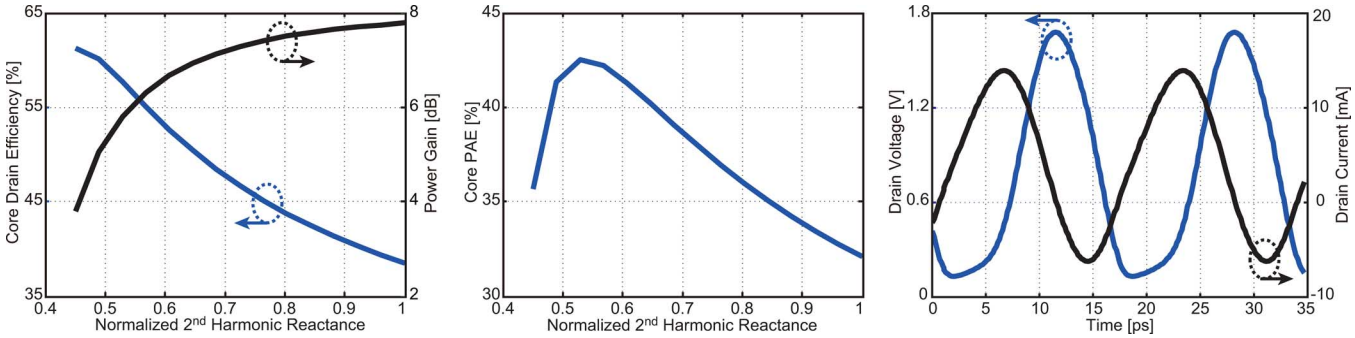

Fig. 7. Predicted PA core drain efficiency, power gain, PAE, and simulated V-I waveforms.

TABLE I
TRUTH TABLE OF THE QUADRANT SIGNALS

Input (I, Q)	Quad1	Quad2	Quad3	Quad4
(1,1)	1	0	0	0
(-1,1)	0	1	0	0
(-1,-1)	0	0	1	0
(1,-1)	0	0	0	1

TABLE II
PHASE ROTATION REGION AND ITS CORRESPONDING CONTROL SIGN BITS

SI,SQ (Sign bits of the phase rotation control)	Phase rotation region in radians
(0,0)	0 to $\pi/2$
(1,0)	$\pi/2$ to π
(1,1)	π to $3\pi/2$
(0,1)	$3\pi/2$ to 2π

second harmonic reactance (normalized to the reactance of the transistor capacitance at the fundamental frequency) presented to the transistor. As evident in the figure, decreasing the second harmonic reactance improves the capacitance tolerance of the ZVS topology and allows a larger switch to be used. As a result, the drain efficiency can be significantly improved. However, larger switches also require larger input power and therefore the power gain decreases. Since the PAE is a function of both drain efficiency and power gain, an optimal normalized second harmonic reactance exists, with a value of approximately 0.52 for this design.

The tuning network for this design is implemented by a 1-to-1 wide trace broadside coupled transformer with a diameter of 42 μm and a series inductor of 100 pH. This passive network up-converts 50 Ω to 150 Ω at the fundamental frequency for optimal power delivery while providing 40 pH of inductance at the second harmonic. The output transformer has a trace width of 12 μm and provides inherent electrostatic discharge (ESD) protection. The ZVS amplifier operates from a 0.8 V supply (for reliability), draws 4.4 mA, and has a simulated power gain of 5 dB. The simulated core drain efficiency is 54% and the overall drain efficiency including the tuning network loss and the pad loss is 34%.

As the target output power is 0 dBm for each element, a single-ended PA is used instead of a differential one since the differential PA requires an additional 4 $\times$ impedance upconversion and would hence suffer from excessive loss. A 2-to-1 transformer is used to achieve the differential to single-ended conversion as well as to perform the required impedance matching between the mixer and the PA. To improve the common-mode rejection of the transformer balun, primary and secondary windings are implemented in two different top metal layers such that the capacitive coupling can be minimized. In addition, a 600 fF de-coupling capacitor is added to the center-tap of the primary winding in order to resonate with the common-mode winding inductance. In order to capture the lead inductance of the current summing structure at the output of the quadrature mixer, an 8-port input structure is attached with the transformer primary in the EM simulation. The combined structure has an insertion loss of 3 dB.

IV. RECEIVER

A block diagram of each receiver element is shown in Fig. 8. Each receiver path consists of an ESD protection structure, a three-stage LNA, a single-balanced quadrature down-conversion mixer, and a BB phase rotator. The most effective technique applied to reduce power consumption at the receiver is to down scale device sizes and hence up scale the operating impedance levels. At the receiver's input, the antenna interface limits the impedance to 50 Ω, but increasing internal impedances is nonetheless an effective means of reducing power consumption.

In the LNA, device and current scaling were performed under given noise figure and bandwidth constraints, resulting in a three stage, inductively degenerated cascode LNA with integrated ESD protection as part of the input matching network (Fig. 8). Cascode devices are used for their higher MSG and unconditional stability at mm-wave frequencies and also to make the LNA less sensitive to process variations.

The first stage of the LNA is optimized for noise and power matching. The input transformer serves both as a part of the input impedance transformation and also as the ESD protection. At low frequencies (transient ESD frequency), the primary winding of the transformer will short the ESD currents to ground. Due to very low magnetic coupling of the 60 GHz transformer at these low frequencies, the secondary side will not see the voltage or current spike. The only consideration then is the current handling capacity of the metal traces. The 9 μm width

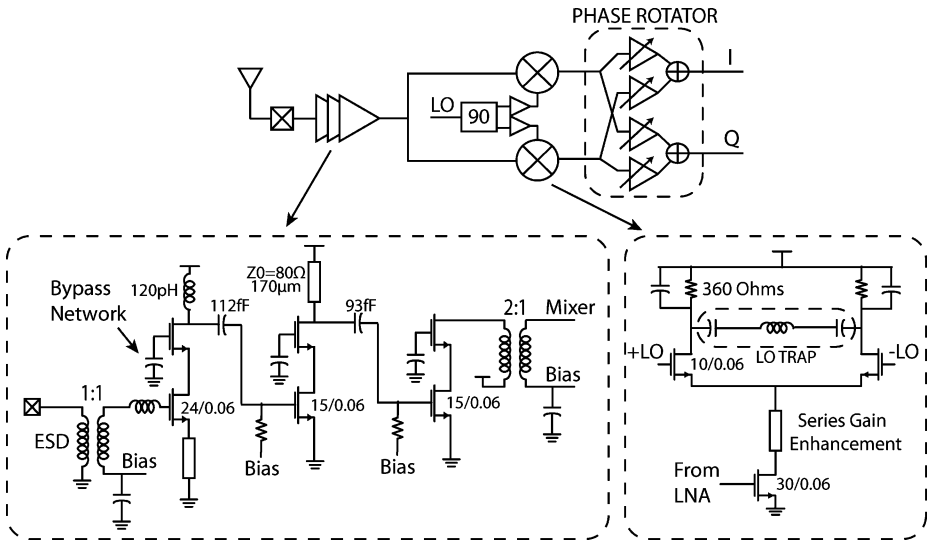

Fig. 8. Schematic of one receiver element.

chosen in this design was previously shown to be adequate for protection against 400 V machine model events [4].

A 2-to-1 transformer is used to achieve the required impedance matching between the LNA and the g_m stage of the quadrature mixer. The LNA is designed to provide 15 dB of power gain (23 dB of voltage gain), 6 dB of NF, and -23 dBm of input referred 1 dB compression point (high-gain mode) and has a measured power consumption of 10 mW (8.2 mA from a 1.2 V supply) under nominal bias settings. It is also designed to provide gain tunability of 9 dB (by utilizing 4-bit programmable bias DACs on each of the three stages) with less than 1 dB increase in NF.

Impedance and device scaling is also applied to the mixer stage. On the mixer switch devices, this downscaling is ultimately limited by the quality factor and self-resonant frequency (SRF) of the matching network on the LO side, since progressively smaller switch sizes require larger inductors for matching at the LO port. In addition, further reduction in switch size will result in a higher required overdrive and hence larger LO power for the same gain. To break this limiting tradeoff on device size and LO power, a single balanced mixer with 10 μm transistors was chosen, which is shown in Fig. 8. This choice will however lead to LO leakage into the mixer output. Therefore, a series LC LO trap has been implemented using a 2-turn inductor in order to reduce the LO feedthrough on the IF side by 25 dB. The mixer requires -5 dBm of LO power to provide 700 mV of differential input swing at the switching transistor gates, which is provided by the mixer buffers in the LO distribution network.

Another effect of device and current scaling is the increase in the impedance of the internal mixer node. A series gain enhancement tuning network was therefore implemented with 120 μm of 80 Ω Coplanar Waveguide (CPW) transmission line in order to prevent loss on the high-frequency signal [17]. Each I/Q mixer can provide a simulated voltage gain of 6 dB, and the total measured power consumption of the quadrature mixer is 5 mW (2.1 mA from a 1.2 V supply for each of the I and Q mixers). The mixer has a simulated input voltage at 1 dB compression point and NF (referenced to 50 Ω input impedance) of 123 mV and 9.5 dB, respectively.

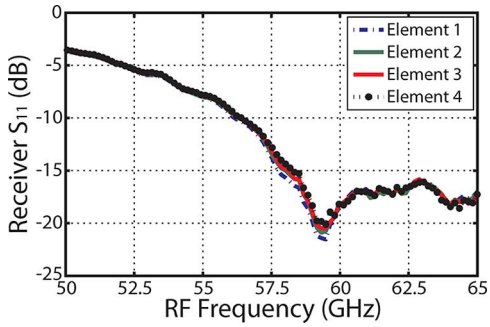

Fig. 9. Measured S_{11} of 4-element receiver.

The baseband phase shifter consists of a bank of current-summed g_m stages whose polarities and input sources are controlled digitally. The relative gains of the I and Q channels are controlled in steps of 1/8. Combined with the polarity controls to set the phase quadrant, this leads to 11° of phase resolution. To reduce power consumption, a partial I/Q sharing structure [4] is implemented here, resulting in 12 g_m cells in each phase shifter. The output current from different elements are summed in the current domain at the center of the chip and then converted to voltage through load resistors. The combined signal is then fed into a baseband buffer to drive the outputs off chip. Each phase rotator achieves a simulated bandwidth of 3.5 GHz while consuming 3 mW of power. The input referred noise density and input voltage at 1 dB compression point of the phase rotator are 4 nV/$\sqrt{\text{Hz}}$ and 220 mV, respectively.

The measured gain, average noise figure, and input referred 1 dB compression point ($IP_{-1\text{ dB}}$) of each receiver path are 24 dB, 6.8 dB, and -29 dBm, respectively, when consuming 27 mW under nominal settings (including the mixer buffers) from a 1.2 V supply. Because of the use of a transformer at the input, the matching is wideband and S_{11} remains better than -10 dB from 56 GHz to 65 GHz. Measured S_{11} for all four elements is shown in Fig. 9.

V. LO Generation and Distribution

The 60 GHz LO for both the TX and RX is generated by a fully integrated, integer-N, charge pump based phased locked

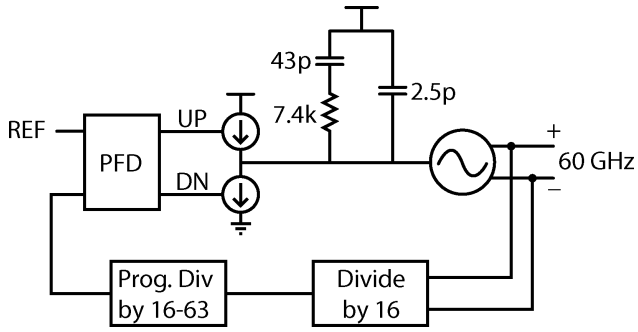

Fig. 10. Integer-N phase locked loop block diagram.

loop (PLL) that has been optimized for minimum integrated output phase noise. The core of this type-II 3rd order integer-N PLL (Fig. 10) consists of a fundamental mode VCO with directly coupled buffers to drive the LO distribution chain (Fig. 11). The VCO was chosen to be a fundamental mode design since it provides significantly higher output power than a push-push or higher order harmonic multiplier [18], easing the gain requirements in the distribution chain. Since the LO must be distributed to many elements, splitting losses will reduce the LO power, and using a high output power VCO significantly reduces the overall power consumption in a phased array transceiver. This can only be achieved by the design of a low power 60 GHz VCO and 60 GHz divider. As demonstrated next, the overall power consumption of this PLL is lower than the power consumed by a harmonic design.

In order to achieve a low-power and robust 60 GHz VCO design, a cross-coupled topology was selected for the core with a single turn 125 pH octagonal inductor. Our previous work has shown that single-turn inductors are nearly optimal for low loss resonators [19]. To achieve high tuning range while maintaining a low $\mathrm{K_{VCO}}$ for reduced noise sensitivity, a 3-bit switched varactor bank is used in parallel with an analog varactor $2\times$ the size of the bank LSB, ensuring 50% overlap between tuning bands. Non-minimum channel length ($0.18\ \mu\mathrm{m}$) was used for all varactors; optimized to achieve high on-off ratio with good quality factor. The final design achieves 12.4% tuning range with approximately 1.9 GHz/V $\mathrm{K_{VCO}}$ per band while consuming only 9 mW from a 1 V supply. The VCO has a simulated free running phase noise of $-115\ \mathrm{dBc/Hz}$ at 10 MHz offset.

The use of a fundamental mode oscillator requires a low power 60 GHz divider, making an injection locked design desirable [20]. Since the phase noise is set by the injected signal, coverage of 3 VCO bands can be ensured by adding a parallel resistor $\mathrm{R_L}$ to de-Q the tank (Fig. 12) without affecting the output phase noise. The total locking range is extended to cover the rest of the VCO's tuning range by using a 2-bit switched varactor bank (which could be tied to the MSBs of the VCO control bits), also maintaining 50% overlap between divider bands. The rest of the divider chain includes two current-mode-logic (CML) dividers and a TSPC divider followed by a 16 to 63 programmable counter. The injection locked divider consumes 3.6 mW from the 1.2 V global supply while the rest of the dividers consume a total of 5 mW.

The differential VCO outputs each drive a single-ended distribution network for the RX and TX, respectively, through independent single-ended LO buffers. To maintain high impedance in the VCO tank for low power consumption, both the first divider and the LO buffers are capacitively coupled to the VCO core. The buffers – whose outputs are matched to the distribution network impedance with transmission lines (for compactness) – also provide gain and isolation from the distribution network. Each buffer consumes 3.6 mW from the 1.2 V global supply.

The phase comparison path consists of a flip-flop based Phase Frequency Detector (PFD) followed by a charge pump and an on-chip 2nd order loop filter. The charge pump topology is based on the design presented in [21]. The selection of charge pump current and loop filter components was optimized to minimize overall output phase noise for the PLL. The charge pump current is programmable from 250 μA to 2 mA with a nominal value of 1 mA. The loop bandwidth can be programmed using the charge pump current to 1–6 MHz.

The LO distribution network (Fig. 11) was designed to minimize power consumption while maintaining scalability for larger phased-arrays. Maintaining a constant impedance with transmission lines and matched power splitters allowed arbitrary routing of the LO signal, which scales well for larger arrays. In this design, in-phase splitting is performed by Wilkinson dividers to each of the 4 elements, followed by local hybrids to generate the quadrature LO. The Wilkinson dividers utilize meandered 71 Ω CPW transmission lines to reduce the area required. The simulated insertion loss of this splitter is only 0.7 dB. The hybrid is a transformer-based lumped design that requires very little area by comparison (area is only $0.002\lambda^2$) while still achieving only 0.7 dB of insertion loss in simulation. Finally, at each mixer, a local buffer is required to drive the mixer LO port impedance and to provide gain. This buffer is always required to ensure sufficient LO swing at the mixer for high conversion gain. Due to the large LO swing required at the mixers, a 2:1 transformer is used at the output of each LO buffer to reduce the voltage swing requirement from the buffer. This transformer also performs single-ended to differential conversion and provides impedance matching. The size of the buffer is chosen for maximum drain efficiency while providing the required power level to the transformer. The gain of each buffer provides approximately 2 dB of margin ensuring sufficient LO swing over process variations. For a small number of elements, the gain of this buffer easily offsets the loss of the distribution network. However, for larger arrays, further buffering would be required within the distribution network by, for example, using active signal splitters [8]. Nevertheless, on a per element basis, the power consumption is dominated by the mixer buffers which consume less than 3 mW each.

VI. Experimental Results

The transceiver was realized in a 65 nm standard CMOS process with no special RF options. The die photo of the 4-element phased array transceiver including on-chip PLL and LO distribution is shown in Fig. 13. Due to the use of lumped-element based design, the area of each TX and RX element is $0.3\ \mathrm{mm^2}$ (TX)/$0.416\ \mathrm{mm^2}$ (RX) (including mixer buffers and hybrids), and the overall TRX occupies an area of 2.5 mm by 3.5 mm. All measurements were performed by direct on-chip probing of mm-wave signals in a chip-on-board assembly which

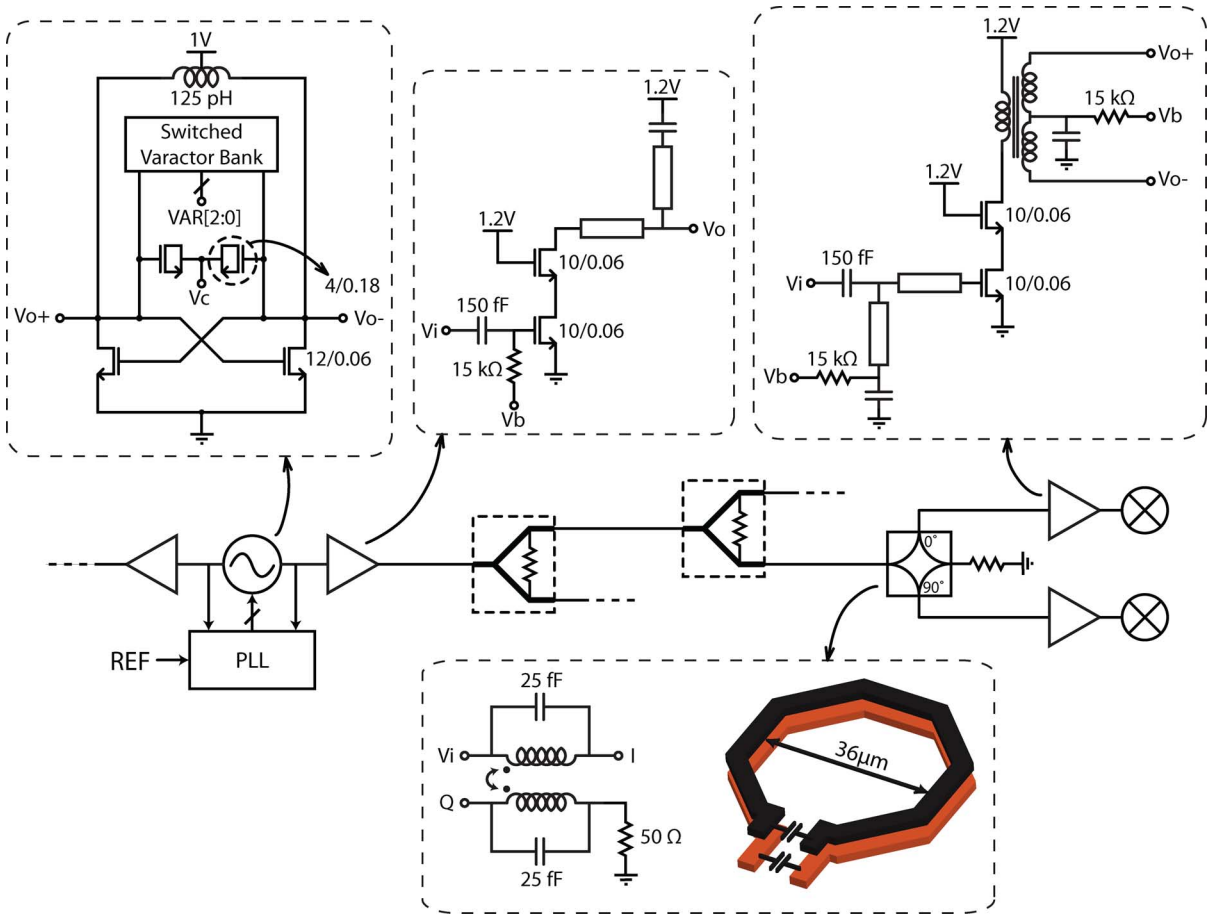

Fig. 11. Schematic of VCO, LO buffers, and LO distribution chain including Wilkinson power splitters and transformer coupled lumped quadrature hybrid.

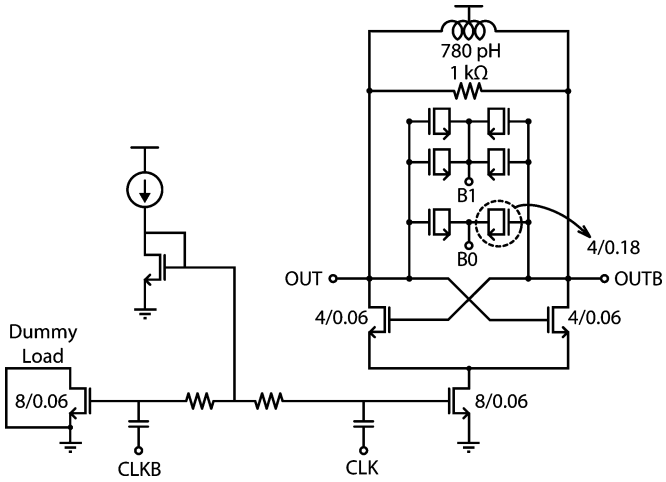

Fig. 12. Schematic of injection locked divider.

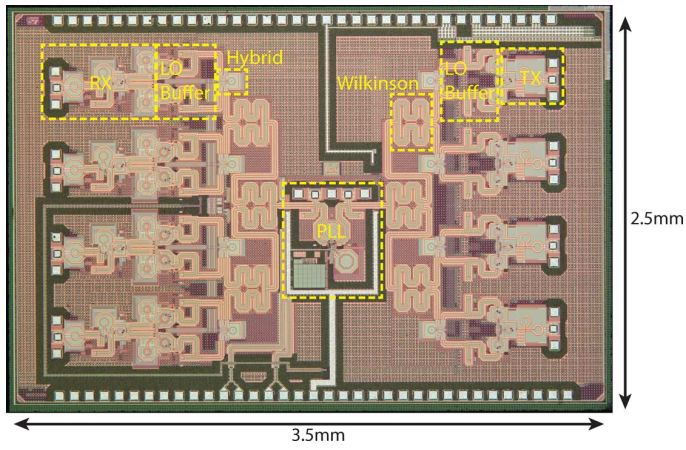

Fig. 13. Transceiver die photo (left side: RX, center: LO generation and distribution, right: TX).

allowed DC and IF signals to be bonded out to connectors on a PCB.

Fig. 14 shows the measured output power of each transmitter element. The measured peak output power and PA drain efficiency is −1.5 dBm and 20% respectively with 3-dB bandwidth of more than 8 GHz. The output power difference between elements is less than 0.5 dB. The measured power is lower than the simulation results, but within the expected range for process variations.

Each transmitter element was tested using QPSK modulated signals mapped from PRBS sequences generated on-chip. The 60 GHz output was down-converted using an external harmonic mixer. Fig. 15 shows the measured eye-diagram when transmitting 5 Gb/s data on the I-channel. The transmitter consumes a

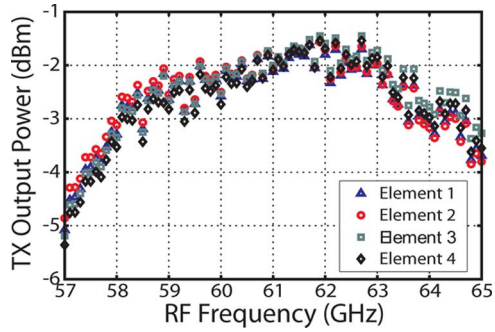

Fig. 14. Measured output power of four transmitter elements.

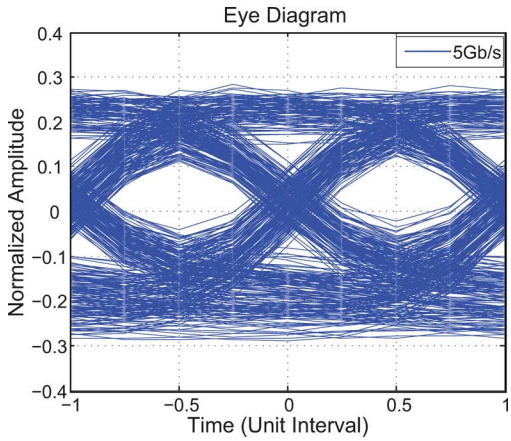

Fig. 15. Measured eye-diagram of the I-channel while transmitting 5 Gb/s QPSK data.

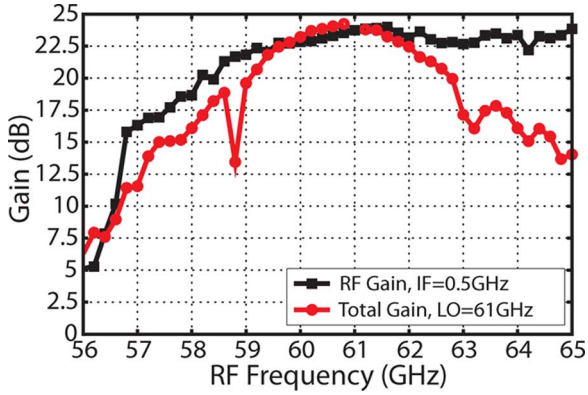

Fig. 16. Single-element RX measured gain and BW: Overall BW (red) and RF front end BW (black).

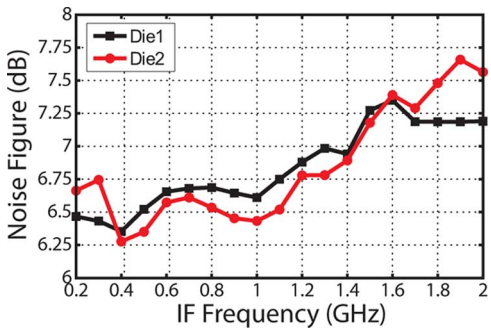

Fig. 17. Measured receiver noise figure.

total worst-case (45° phase shift) power of 27 mW/element (including LO distribution).

The RX gain and bandwidth measurements were performed by using a 60 GHz signal generator and a 25 GHz spectrum analyzer. The overall bandwidth was measured by maintaining a fixed LO frequency of 61 GHz and sweeping the RF frequency. The overall gain and bandwidth of a single-element receiver were 24 dB and 1.8 GHz respectively. In addition, the RF bandwidth was measured separately by sweeping the LO and RF signals together at a constant offset of 500 MHz resulting in a constant 500 MHz IF frequency. As shown in Fig. 16, the RF 3-dB bandwidth is higher than 6.5 GHz and is limited on the high side at 65 GHz by the instrument capabilities (VNA). Given the as-expected high RF bandwidth and our simulations of the bandwidth of the baseband chain, we believe that the limitation on the overall bandwidth is most likely due to filtering from bond wires and PCB routing of the baseband signals. These limitations would of course be removed if the baseband were integrated onto the same die as the RF transceiver.

Measurement of a single-element receiver's NF vs. IF frequency is illustrated in Fig. 17. The NF measurement was performed using a 60 GHz noise source and an Agilent N8974A noise figure meter. An average noise figure of 6.8 dB was measured over 2 GHz of IF bandwidth, with a minimum NF as low as 6.3 dB.

The measured TX and RX phase constellations of the four elements are shown in Fig. 18(a) and (b). In the TX, the VNA is used to measure the phase rotation angle. An external LO signal is fed from Port 1 of the VNA to the distribution tree while taking the output from the PA to Port 2 and observing the relative phase shift (S21). In the RX, due to the ability to control the I and Q phase shifters independently, direct measurement of I and Q phase and amplitude is performed. The TX and RX achieve 360° of phase shifting range with worst-case phase steps of 5° and 11° respectively. The gain variation across all phase settings and all elements is less than ± 0.5 dB.

The two-element phased array normalized gain is shown in Fig. 19 as a function of phase shifter rotation angle. This two-element measurement was performed by using dual GSG probes and off-chip power splitters/combiners allowing simultaneous probing of both elements. The phase setting of one element was held constant while the phase shift on the other element was swept over its entire range. Due to the high phase resolution and low gain mismatch, the measured peak-to-null ratio on the TX and RX are 40 dB and 29 dB respectively. This confirms that the on-chip isolation between elements is sufficient to obtain a good peak-to-null ratio.

As a further characterization of the performance of the array, 4-element synthesized TX and RX patterns were constructed (Fig. 20). These patterns are based on measurements of each of the 4 elements phase and gain characteristics and assume a $\lambda/2$ uniform array. In such array patterns, the peak gain is not as sensitive as the nulls to the mismatch in gain and phase between elements. Thus, the close matching between ideal and synthesized array patterns shown in Fig. 20 further confirms the high resolution and accuracy of the proposed transceiver design.

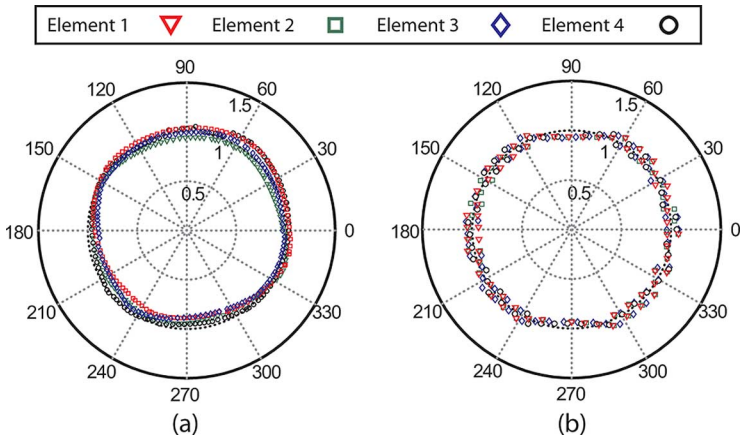

Fig. 18. Measured phase constellations for all four elements: (a) TX, (b) RX.

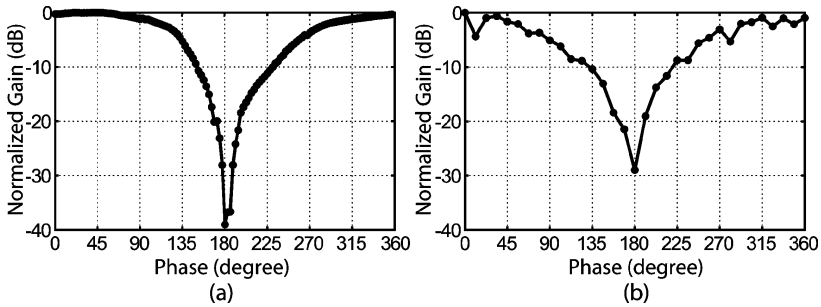

Fig. 19. Measured two-element pattern: (a) TX, (b) RX.

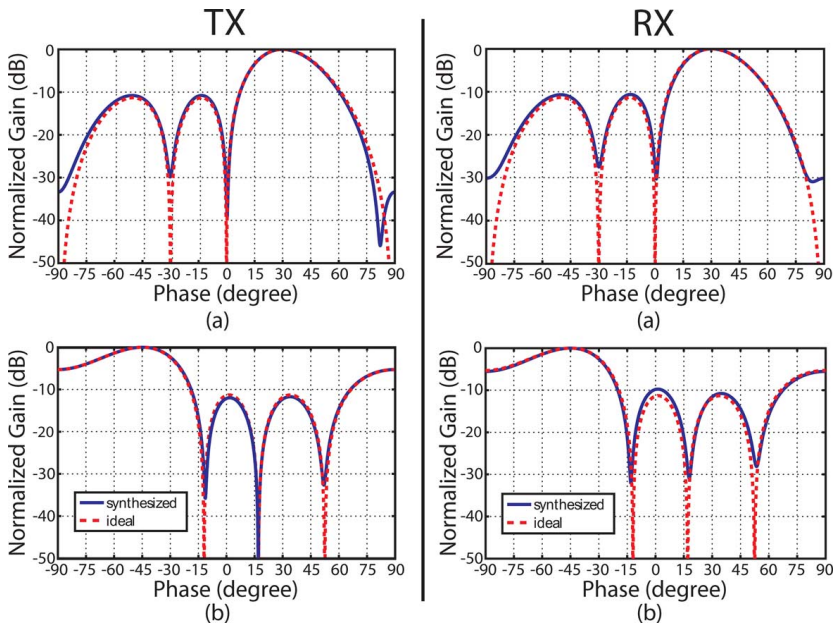

Fig. 20. Synthesized array patterns with array steered to: (a) 30° angle, (b) −45° angle.

The PLL output was directly probed on-chip to allow measurement and characterization. The measured VCO tuning range over all 8 tuning bands is 57.9–65.6 GHz (Fig. 21), equivalent to a tuning range of 12.4%. The VCO has a measured free running phase noise of $-112\,\mathrm{dBc/Hz}$ at 10 MHz offset. The phase noise variation of the VCO (due to varactor non-linearity) was approximately ± 1 dB across each discrete band. The measured output power from one LO buffer is -1.8 dBm, for a total differential power of $+1.2$ dBm. The locked PLL spectrum (Fig. 22) and phase noise (Fig. 23) were measured using an external down-conversion mixer to bring the LO in range of an Agilent E4440A Spectrum Analyzer. Note that since the measured response for both the TX and RX is centered around 61 GHz, the PLL reference for these tests was 119 MHz with the programmable di-

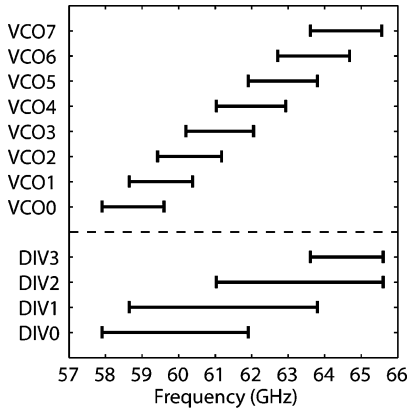

Fig. 21. Measured VCO and injection locked divider tuning range. (Measurement of divider tuning range limited by VCO).

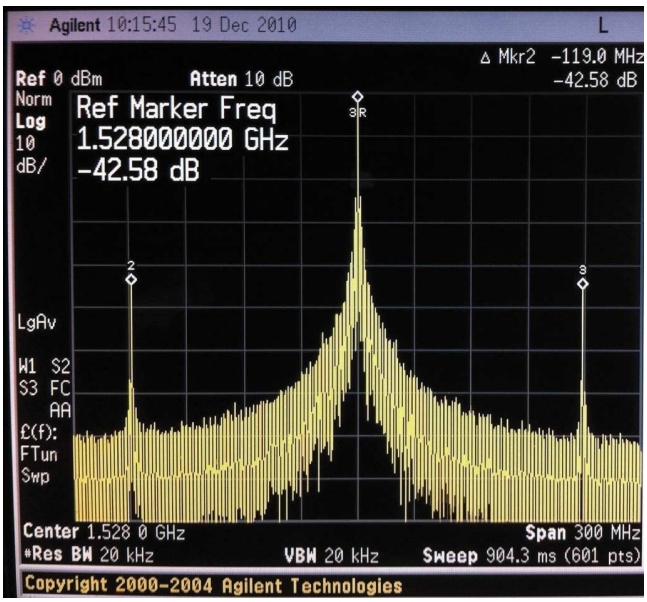

Fig. 22. Spectrum of locked PLL at 61 GHz downconverted with external mixer to allow measurement with Agilent E4440A Spectrum Analyzer. Reference spurs are less than −40 dBc.

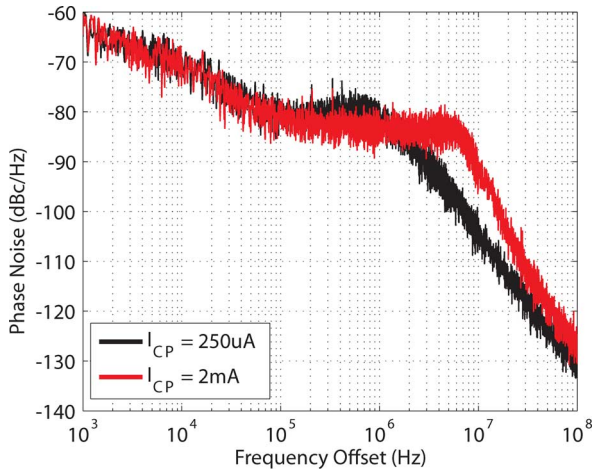

Fig. 23. Measured phase noise at 61 GHz for two loop bandwidth settings, measured using Agilent E4440A Spectrum Analyzer.

TABLE III
PLL PERFORMANCE SUMMARY AND COMPARISON

	[22]	[18]	[23]	**This Work**
Technology	CMOS 65nm	CMOS 0.18µm	CMOS 65nm	**CMOS 65nm**
Freq. (GHz) (Tune Range)	42.1-53 (22.9%)	53-58 (9%)	55.4-60.3 (8.5%)	**57.9-65.6 (12.5%)**
Power (mW)	72	35.7	46	**29**
Reference Spur (dBc)	-	-40	-35	**-42**
Output Power (dBm)	-	-37.85	-7	**+1.2**
PLL Phase Noise (dBc/Hz)	-81 (in-band) -84.5 @ 1MHz*	-85.2 (in-band) -90.9 @ 10MHz	-65 (in-band) -87 @ 1MHz	**-82 (in-band) -107 @ 10MHz**
VCO FOM (dBc/Hz)	-179	-157.5	-175.3	**-178.3**
VCO FOM_T (dBc/Hz)	-186.2	-156.6	-173.9	**-180.2**

* from phase noise plot of PLL locked to 51.84GHz

vider set to 32 for an LO at 61 GHz. For standards compliance, a 135 MHz reference would be used to allow tuning to the four standard channels by varying the programmable divider; well within the capabilities of this system.

Measurements show reference spurs to be lower than -40 dBc, while PLL phase noise is -82 dBc/Hz in-band and -107 dBc/Hz at 10 MHz offset. Due to incorrect sizing of the final divider stage and the buffer at the output of the divider chain, the divider chain output noise is dominated by these two stages and is much higher than expected. Since divider noise is indistinguishable from reference noise, this effect appears as excess reference noise in measurements of the PLL output noise. In simulation with an appropriately sized divider and buffer (which would only have consumed an additional 1 mW of power), the in-band PLL output noise is approximately 12 dB lower. The entire PLL, including LO buffers, consumes only 29 mW while achieving high tuning range and similar noise performance to previously reported low-power PLLs (Table III), making it a competitive solution for 60 GHz phased array transceivers.

VII. CONCLUSION

This paper describes the design and characterization of a low-power, scalable, fully-integrated 60 GHz 4-element 65 nm CMOS phased array transceiver consuming <34 mW/element including LO synthesis and distribution. The transceiver operates from a 1.2 V supply and consumes 137 mW in either transmit or receive mode. Energy and area efficient phased array transceivers are key to enabling multi Gb/s communication in mobile devices at 60 GHz, and hence are the principal focus in this design. Holistic impedance optimization in a BB phase shifting architecture is used in order to achieve high energy efficiency. In addition, the BB phase shifting architecture has the advantage of allowing high and accurate phase resolution.

In the transmitter, a current-reuse architecture for the phase rotator/mixer and switching PA enables substantial improvement in the current-efficiency of this block as well as the en-

TABLE IV
TRX PERFORMANCE SUMMARY AND COMPARISON

	[This work] TRX	[9] TRX	[8] TX	[10] RX
Technology	**65nm CMOS**	90nm CMOS	0.12µm SiGe	0.12µm SiGe
Array Size	**4**	32	16	16
RX Gain/Element	**24dB**	12.5dB	-	50dB (w/ BB VGA)
RX NF/Element	**6.8dB**	11dB	-	7.4-7.9dB
Phase Resolution	**TX: 6 bits*** **RX: 5 bits***	2 bits	6 bits	5 bits
3dB BW	**RX: >±1.8GHz** **TX: 8GHz pwr. BW**	-	±1GHz	>±1GHz
IP_{1dB} @ RX Gain (/El.)	**-29dBm** **@24dB**	-17dBm @12.5dB	-	-40dBm @24 dB
Tot TX o/p Power TX o/p /El.	**4.5dBm** **-1.5dBm**	8dBm -7dBm	21dBm 9dBm	N/A
Total Power	**137mW(TX/RX)**	507mW	3.8W	1.8W
Synthesizer	**29mW**	Not Included	-	-
Pdc/El. (no synth.)	**27mW**	16mW	156mW	59mW
TX Efficiency: P_{out}/P_{DC} (/El.)	**2.58%**	1.25%	5.1%	-
RX Noise FOM: $1/(F.P_{DC})$ (/El.)	**7.75**	4.975	-	2.915

* Measured ENOB

tire transmitter element. On the receiver, down-scaling device sizes and up scaling impedance levels similarly results in significant power savings. Finally, the LO distribution network is designed to minimize power consumption while maintaining scalability for larger phased arrays by utilizing a constant impedance with transmission lines and matched power splitters along with power optimized LO buffers.

Table IV shows the comparison of this design with state of the art 60 GHz phased arrays in silicon. While a direct comparison between the works is difficult due to the wide range of specifications, the proposed architecture and implementation techniques enable high performance (comparable to that of designs not targeted for mobile applications) while retaining low overall power consumption.

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Maryam Tabesh (S'05) received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2005, and the M.S. degree from the San Jose State University, San Jose, CA, in 2007. She is currently working toward the Ph.D. degree at the University of California at Berkeley.

She is an active member of the Berkeley Wireless Research Center (BWRC). Her research interests are in energy-efficient mm-wave phased-array systems, passive RFID circuits and ultra-low-power electronics for sensor applications. She spent summer 2007 with HMicro Inc. in Los Altos, CA, and summer 2010 at the Corporate R&D division of Qualcomm in San Diego, CA.

Ms. Tabesh was the recipient of the Qualcomm Innovation Fellowship 2010–2011, the 2006–2007 Society of Women Engineers (SWE) Scholarship, and the 2007 Alfred Dixon Memorial Scholarship.

Jiashu Chen received the B.E. degree in electronic engineering with First Class Honors from City University of Hong Kong, Hong Kong, China, in 2007. As an undergraduate student, he also studied at Fudan University in Shanghai and Carnegie Mellon University in Pittsburgh, PA. He is currently working towards the Ph.D. degree at the University of California, Berkeley.

He is a member of the Berkeley Wireless Research Center (BWRC). His research focuses on power amplifiers in silicon technologies, mm-wave beamforming transceiver arrays and efficient mm-wave transmitter architectures. He held an internship position at Maxim Integrated Products, Inc. in 2010.

Mr. Chen is a recipient of the prestigious 2007 International Fulbright Science and Technology Fellowship, which is awarded by the U.S. Department of State to 27 international Ph.D. students out of 110 nominations from 70 countries. He is also a recipient of many other awards including the Best Student Paper Award at the 2010 Radio Frequency Integrated Circuits Symposium, Analog Devices Outstanding Student Designer Award in 2011, MTT-S Undergraduate/Pre-graduate Fellowship in 2007 and the Scholarship for Outstanding Chinese Mainland Students from the Hong Kong University Grants Committee in 2004.

Cristian Marcu (S'01) received the B.S.E.E. degree from the University of California, Irvine, in 2005 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 2008 and 2011, respectively.

In 2007, he interned with Qualcomm Inc., Campbell, CA, working on cellular receivers. In 2009 and 2010, he interned with Qualcomm, Santa Clara, CA, where he worked on ultra-low-power mixed-signal design and WLAN power amplifiers, respectively. In 2011 he joined Qualcomm Atheros, San Jose, CA, where he is working on radio-frequency integrated circuits for wireless applications. His research interests included CMOS mm-wave circuit design, and low power frequency synthesis for mm-wave applications.

Lingkai Kong (S'07) received the B.S. degree in mathematics and physics from Tsinghua University, Beijing, China, in 2007. He is currently working towards the Ph.D. degree in electrical engineering at the University of California, Berkeley.

During the summer of 2008, he was a design engineer intern at Inphi Corp., Westlake Village, CA, where he was involved with a 10 Gb/s laser driver design. He was also a design engineer intern during summer 2010 at Rambus Inc., Los Altos, CA, where he worked on a 60 GHz phased-array front-end. In 2011 summer, he was with Xilinx, San Jose, CA, developing a voltage-mode transmitter for high-speed serial link applications.

Mr. Kong is the recipient of 2011 Analog Devices Outstanding Designer Award.

Shinwon Kang (S'09) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2004. Since 2008, he has been pursuing the Ph.D. degree in electrical engineering at the University of California, Berkeley.

From 2004 to 2007, he worked at Xeline, Seoul, Korea, where he was involved with the design and implementation of powerline communication chips and modems. In summer 2011, he interned with Qualcomm Inc., Santa Clara, CA. He is currently with the Berkeley Wireless Research Center (BWRC). His research interests include RF/microwave and millimeter-wave integrated circuits and systems.

Mr. Kang was a recipient of the GE Foundation Scholar-Leaders Program in 2003–2004 and the Qualcomm Scholarship Program from Qualcomm Korea Ltd. in 2004. He was a co-recipient of the IEEE ISSCC 2010 Jack Kilby Award for Outstanding Student Paper. Since 2008, he has held the Samsung Scholarship for graduate studies.

Ali M. Niknejad (S'10) received the B.S.E.E. degree from the University of California, Los Angeles, in 1994, and the Master and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1997 and 2000. During his graduate studies, he authored *ASITIC*, a CAD tool that aids in the simulation and design of passive circuit elements such as inductors into silicon integrated circuits.

After graduation from Berkeley, he worked in industry focusing on the design and research of analog RF integrated circuits and devices for wireless communication applications. He is currently an Associate Professor in the EECS Department at UC Berkeley and co-director of the Berkeley Wireless Research Center and the BSIM Research Group. His research interests lie within the area of wireless and broadband communications (RF, mm-wave, and sub-THz), including the implementation of integrated communication systems in silicon using CMOS, SiGe, and BiCMOS processes. His focus areas of his research

include analog and RF circuits, device physics and modeling, and numerical techniques in electromagnetics.

Prof. Niknejad served as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and on the TPC for the IEEE ISSCC and CICC. He is currently a SSCS Distinguished Lecturer. He was a co-recipient of the Outstanding Technology Directions Paper at ISSCC 2004 for co-developing a modeling approach for devices up to 65 GHz. He is also a co-recipient of the 2010 Jack Kilby Award for Outstanding Student Paper for his work on a 90 GHz pulser with 30 GHz of bandwidth for medical imaging. His students have also been awarded the RFIC best paper awards in 2005, 2007, 2008, and 2009. He is a co-founder of HealthMicro and inventor of the REACH™ technology, which has the potential to deliver robust wireless solutions to the healthcare industry.

Elad Alon (S'02–M'06) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2001, 2002, and 2006, respectively.

In 2007, he joined the University of California, Berkeley, as an Assistant Professor of electrical engineering and computer sciences, where he is now a co-director of the Berkeley Wireless Research Center (BWRC). He has held visiting positions at Xilinx, Oracle, Sun Labs, Intel, AMD, Rambus, Hewlett-Packard, and IBM Research, where he worked on digital, analog, and mixed-signal integrated circuits for computing, test and measurement, and high-speed communications. His research focuses on energy-efficient integrated systems, including the circuit, device, communications, and optimization techniques used to design them.

Dr. Alon received the IBM Faculty Award in 2008, the 2009 Hellman Family Faculty Fund Award, the 2010 UC Berkeley Electrical Engineering Outstanding Teaching Award, and the 2010 ISSCC Jack Raper Award for Outstanding Technology Directions Paper.