A 60-GHz Band 2×2 Phased-Array Transmitter in 65-nm CMOS

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***Abstract*—A 60-GHz band 2×2 phased-array transmitter implemented in 65-nm bulk CMOS is described. Two-dimensional beam steering in the azimuthal and elevation planes is implemented via LO phase shifting in a transmitter that also supports direct or IF up-conversion. Full current bleeding in the final upconversion mixer suppresses flicker noise, and dynamic LO biasing suppresses carrier feedthrough. The 2.9×1.4 mm^2 chip consumes a total of 590 mW from a 1-V supply when driving all four channels at a maximum saturated output power of 11 dBm, with 20 dB gain per transmitter. Carrier leakage varies between -20.5 dBc ± 0.5 dB and sideband rejection is 25 to 28 dBc among the four transmitters when measured on the same die. The measured phase noise is 1.7 ± 1 dB higher than the theoretical 21.6 dB increase in the phase noise due to $12\times$ frequency multiplication of the injected LO. Maximum power-added efficiency of the transmit amplifier is greater than 16%, and gain is above 17 dB from 54 to 61 GHz.**

***Index Terms*—Active inductor, carrier feedthrough, CMOS, frequency multiplier, I/Q generator, low voltage, millimeter wave, phased array, phase shifter, power amplifier, sideband suppression, transformer coupling, transmitter, tripler.**

I. Introduction

POINT-TO-POINT wireless communication at gigabit per second data rates over short distances operating in the 57 GHz–64 GHz band [1]–[3] may soon be realized using silicon-based integrated circuit technologies, given the recent approval of the IEEE 802.15.3c-2009 standard [4]. The European Computer Manufacturers Association International (ECMA) outlines similar requirements in the ECMA-387 standard [5]. Also, the WirelessHD consortium specification (version 1.0a [6]) for the transmission of high-definition video resides in this unlicensed band. Apart from wireless communication, other potential mm-wave applications for silicon ICs include: long-range collision avoidance radar at 77–79 GHz for automobiles [7], and radio imaging at 94 GHz (and above) for security, medical screening and medical diagnoses [8], [9].

Phased-array systems are well-suited to mm-wave applications [10]–[12] because spatial directivity of the transmit signal emitted from the phased-array antenna may be used to compensate for directionality of propagation that occurs with increasing frequency. Also, the gain of a phased-array antenna offsets the path loss that constrains the span of communication link in the 60-GHz band. Multiple transmitters increase the effective isotropic radiated power (EIRP) by a factor of $10\log_{10}\mathrm{N}$ dB over that of a single transmitter due to the spatial summation of power, where N is the number of elements in the array. The EIRP will increase by another $10\log_{10}\mathrm{N}$ dB due to the gain of the phased-array [13]. Other ways of increasing the transmitter power output, such as raising the supply voltage (which compromises active device reliability [14]), or implementing on-chip passive power combiners (which incur relatively high losses in the interconnect metals and silicon substrate [15], [16]), are less attractive alternatives. In particular, implementation of a 60-GHz band phased-array transceiver in silicon CMOS is preferred because it is amenable to co-integration of RF and baseband circuitry, with the potential for low cost per unit in volume production.

This paper describes a 60-GHz band fully-differential phased-array transmitter IC for steering the radiated beam of a 2×2 antenna array in both azimuthal and elevation planes. The testchip is implemented in a production 65-nm bulk CMOS process with (simulated) $\mathrm{f_T}$ and $\mathrm{f_{max}}$ of approximately 200 GHz [17]. The 2.9×1.4 mm^2 test chip provides four single-ended RF channels with up to 11 dBm (saturated) RF power available from each transmit output. Phase tuning via LO phase shifting is applied in each up-conversion transmitter. Flicker noise and carrier feedthrough are suppressed in the up-converter by full current bleeding and dynamic LO biasing in the mixer. LO phase shifting was selected because the low transconductance of CMOS transistors renders phase shifting in the RF domain less desirable, as the high losses of active phase shifters (e.g., 4.9 dB loss from 50–56 GHz, while consuming 23 mW in 90-nm CMOS [18]) requires more amplification and therefore greater power consumption. Linearity of phase shifters placed in the RF path is also important, as they may distort the transmitter outputs. A third alternative is baseband or IF phase-shifting performed at a lower frequency. This is less sensitive to impairments caused by circuit parasitics, but requires extensive calibrations to remove phase and amplitude errors [19]. The large-signal LO is applied to the input of a transmit mixer, rendering the RF outputs relatively insensitive to amplitude differences caused by on-chip mismatches between the differential LO signals used in each up-converter. However, both LO and IF phase-shifting schemes require the mixers to have a wider dynamic range than in the RF phase-shifting topology. This is not a disadvantage in a transmitter application, because the dynamic range of the baseband signal is known and defined by the modulation scheme.

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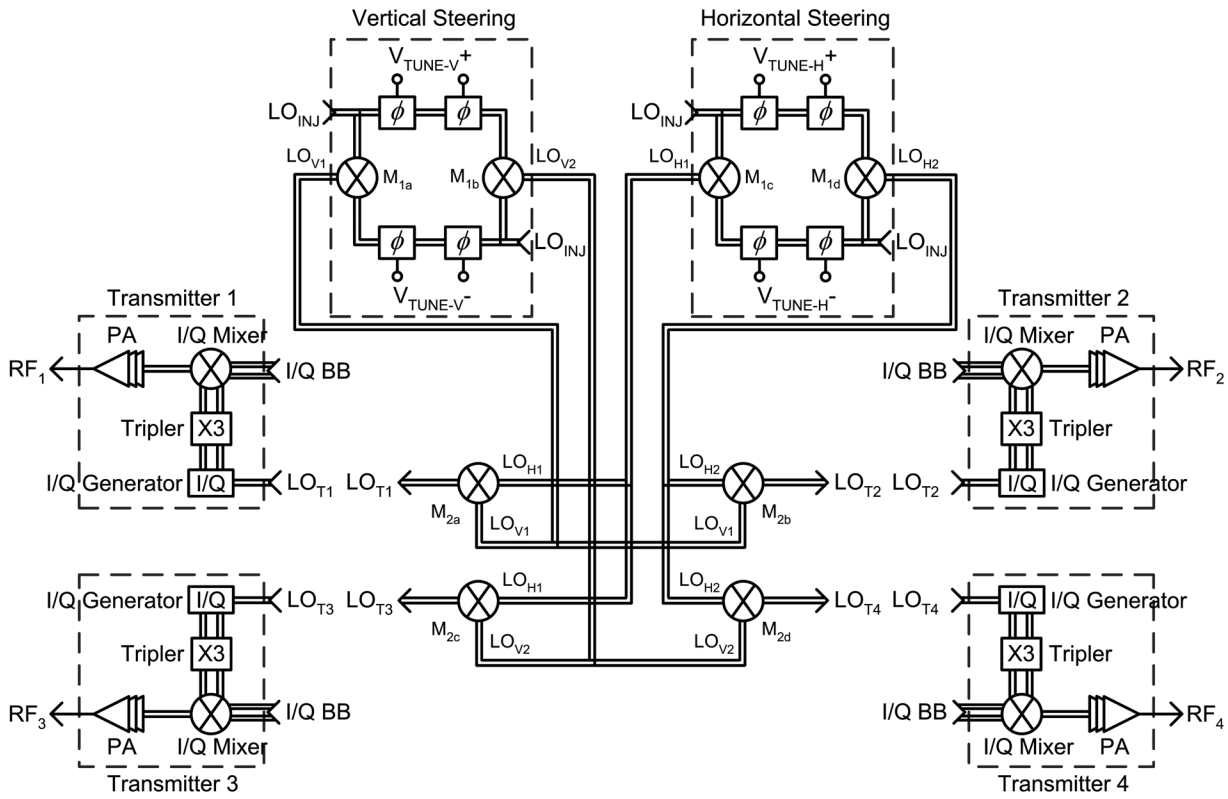

Fig. 2. Phased-array transmitter architecture.

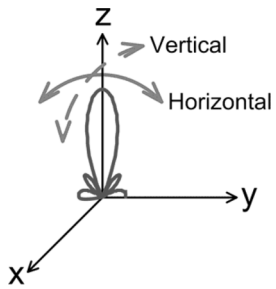

Fig. 1. Beam steering.

Section II of this paper examines the architecture of the 2 × 2 phased-array transmitter, and discusses the merits of such implementation. Section III describes the schematic implementation of the various building blocks, while the experimental setup and measurement results of this array test chip are presented in Section IV.

II. Phased-Array Transmitter Architecture

A 2 × 2 phased-array transmitter can effectively steer the energy radiated by the four antennas in any direction above the plane of the array, as illustrated in Fig. 1. By varying the transmit signal phase between antenna pairs, the antenna beam may be steered either vertically (i.e., elevation plane) or horizontally (i.e., azimuthal plane). Fig. 2 shows the transmitter architecture implemented in this work. This design is capable of independent steering of the beam produced by a 2 × 2 antenna array in both vertical and horizontal planes, as LO phase-shifting facilitates phase adjustment of all four (identical) transmitter outputs. The topology is fully-differential (differential signal paths are indicated by closely-spaced parallel lines connecting the circuit blocks in Fig. 2), which improves the rejection of common-mode interference (e.g., supply noise). At mm-wave frequencies, the balanced signal path in differential circuits also minimizes the deleterious effects of interconnect and ground inductances, thereby reducing parasitic degeneration and eliminating a source of potential instability in the power (and other) amplifier stages.

The injected LO at 1/12th of the desired carrier frequency ($\mathrm{LO_{INJ}}$ at ∼5 GHz) drives two sets of cascaded phase shifters and mixers that control both vertical and horizontal beam steering in the 2 × 2 antenna array. The phase shifters are cascaded to increase the tuneable phase range. Multipliers $\mathrm{M_{1a}}$–$\mathrm{M_{1d}}$ double the input frequency (while summing the input phases) to give four, phase-adjustable outputs at $1/6$th of the desired RF carrier (∼10 GHz). Differences in the output phases between $\mathrm{LO_{V1}}$ and $\mathrm{LO_{V2}}$, and $\mathrm{LO_{H1}}$ and $\mathrm{LO_{H2}}$ are controlled independently by differential tuning of $\mathrm{V_{TUNE-V}}$ ($\mathrm{V_{TUNE-V}} + -\mathrm{V_{TUNE-V}}-$) and $\mathrm{V_{TUNE-H}}$ ($\mathrm{V_{TUNE-H}} + -\mathrm{V_{TUNE-H}}-$), respectively. When $\mathrm{V_{TUNE-V}}$ and $\mathrm{V_{TUNE-H}}$ are at their nominal bias voltages, $\mathrm{LO_{V1}}$, $\mathrm{LO_{V2}}$, and $\mathrm{LO_{H1}}$, $\mathrm{LO_{H2}}$ are all in phase (since they are at the same frequency).

The outputs from the first LO up-conversion stages drive four mixers ($\mathrm{M_{2a}}$–$\mathrm{M_{2d}}$) in the second up-conversion stage that generate subharmonics $\mathrm{LO_{T1}}$-$\mathrm{LO_{T4}}$ at $1/3$rd of the RF frequency (∼20 GHz). Simultaneous tuning of $\mathrm{V_{TUNE-V}}$ and $\mathrm{V_{TUNE-H}}$ introduce phase differences among $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$, as the phases of the inputs to mixers $\mathrm{M_{2a}}$–$\mathrm{M_{2d}}$ ($\mathrm{LO_{V1}}$, $\mathrm{LO_{V2}}$, and $\mathrm{LO_{H1}}$, $\mathrm{LO_{H2}}$) are summed at the mixer outputs.

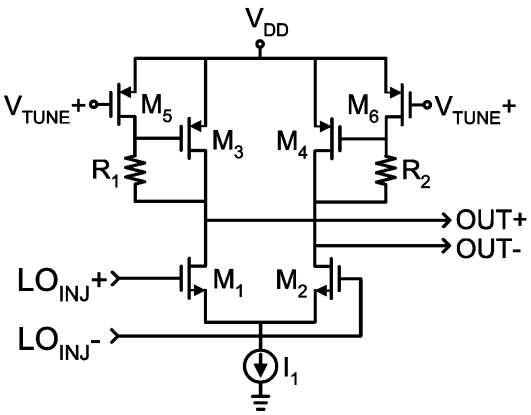

Fig. 3. Schematic of the phase shifter subcircuit.

The differential $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$ outputs drive a quadrature (I/Q) signal generator within each of the four transmitters ($\mathrm{TX_1}$–$\mathrm{TX_4}$), respectively. The quadrature signal generator outputs injection-lock a frequency tripler in each transmitter that generates the 60 GHz-band carrier used to directly up-convert the (I/Q) baseband inputs to RF. The up-converted RF signal then drives a three-stage power amplifier (PA) with an integrated output balun to produce single-ended transmit signals $\mathrm{RF_1}$–$\mathrm{RF_4}$, respectively. The phase shift seen at each transmitter output is three times larger than the phase shift at its respective LO input (e.g., LO_{T1} for output $\mathrm{RF_1}$) due to frequency tripling of $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$. Thus, $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$ are required to be tuneable only over a $\pm 60^\circ$ range as the tripler increases the input phase range by $3\times$ (i.e., to the $\pm 180^\circ$ required for full beam steering).

Each transmitter performs a single up-conversion, and is suitable for zero-IF, low-IF, or GHz-IF use. Since it is a single sideband up-conversion, no IF image-reject filtering is required. Moreover, the 60-GHz-band quadrature carrier that is generated through injection-locking of the tripler helps refine both phase and amplitude of the 20-GHz driving signal produced by the I/Q generator, giving smaller output phase and amplitude errors compared to direct generation of a quadrature LO at 60 GHz due to component mismatches. LO pulling by the PA is also minimized as the injected LO (i.e., inputs to the phase shifters at $\sim$5 GHz) is well-below the RF transmit signal. Isolation of greater than 40 dB between the input and output of each PA is maintained to reduce LO pulling. Furthermore, the power supply nodes of the injection-locked tripler and PA are connected together off-chip to a large de-coupling capacitor to reduce pulling. Carrier feedthrough arises mainly due to asymmetry between the differential waveforms, and is minimized in this design by introducing a small DC offset between the two LO bias voltages (dynamic LO biasing). Flicker noise of the mixer is suppressed by full current bleeding (i.e., no DC bias current flows through the switching quad transistors).

III. Circuit Design and Implementation

This section describes the circuits used to implement the phased-array transmitter in 65-nm bulk CMOS. All circuit blocks use differential signaling.

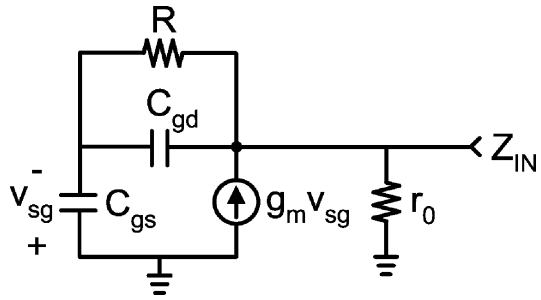

Fig. 4. Simplified small-signal equivalent circuit of the active inductor used in the phase shifter of Fig. 3.

A. Phase Shifter

Fig. 3 shows a simplified schematic of the phase shifter. Two active inductors formed by $\mathrm{M_3}, R_1$ and $\mathrm{M_4}, R_2$ load differential pair $\mathrm{M_1}, \mathrm{M_2}$, which is driven by differential LO input $\mathrm{LO_{INJ}}+$, $\mathrm{LO_{INJ}}-$. Current source $\mathrm{I_1}$ controls the total current flowing through this cell, thus, the gate bias ($\mathrm{V_{TUNE}}+$) on $\mathrm{M_5}$ and $\mathrm{M_6}$ determines the fraction of the total bias current that is shared between tuneable inductances $\mathrm{M_3}, \mathrm{M_5}$ and $\mathrm{M_4}, \mathrm{M_6}$. Any change in the load inductance varies the phase of $\mathrm{OUT}+$ and $\mathrm{OUT}-$ in response to $\mathrm{V_{TUNE}}+$ with only a small amplitude variation of the output swing as the phase shifter draws a constant current.

The small-signal equivalent half-circuit of the active inductor is shown in Fig. 4. The impedance seen looking into the drain of a pMOS transistor with a resistor connected between its gate and drain terminals is derived in the Appendix. It is approximately given by

$$Z_{\mathrm{IN}}(s) \approx \frac{1}{\left(g_m + \frac{1}{r_0}\right)} + sC_{gs}\frac{(g_m R - 1)}{\left(g_m + \frac{1}{r_0}\right)^2} \tag{1}$$

where g_m is the transconductance of transistor $\mathrm{M_3}$ or $\mathrm{M_4}$ in Fig. 3, C_{gs} is the gate to source capacitance, r_0 is the transistor output resistance, and R is the load resistance (either R_1 or R_2 in Fig. 3).

The active inductance in (1) is

$$L_{\mathrm{active}} \approx \frac{C_{gs}(g_m R - 1)}{\left(g_m + \frac{1}{r_0}\right)^2} \tag{2}$$

and its associated Q-factor is

$$Q_{\mathrm{active}} \approx \frac{\omega C_{gs}(g_m R - 1)}{\left(g_m + \frac{1}{r_0}\right)}. \tag{3}$$

The small-signal input impedance of the circuit in Fig. 4 is inductive as long as $g_m R$ is greater than unity. Moreover, (1) reveals two other characteristics. The real part of $Z_{\mathrm{IN}}(s)$ is relatively large, as g_m of the MOS transistor is typically a few milli-Siemens and r_0 of a 65-nm MOS transistor is a few kilo-Ohms in the low-GHz region. Note that the real part of the transistor output resistance decreases with increasing frequency due to the drain-to-bulk parasitic capacitance, which is neglected in Fig. 4. The $Re(Z_{\mathrm{IN}}(s))$ may be reduced by raising the transconductance (g_m) of the transistor by either increasing its aspect ratio

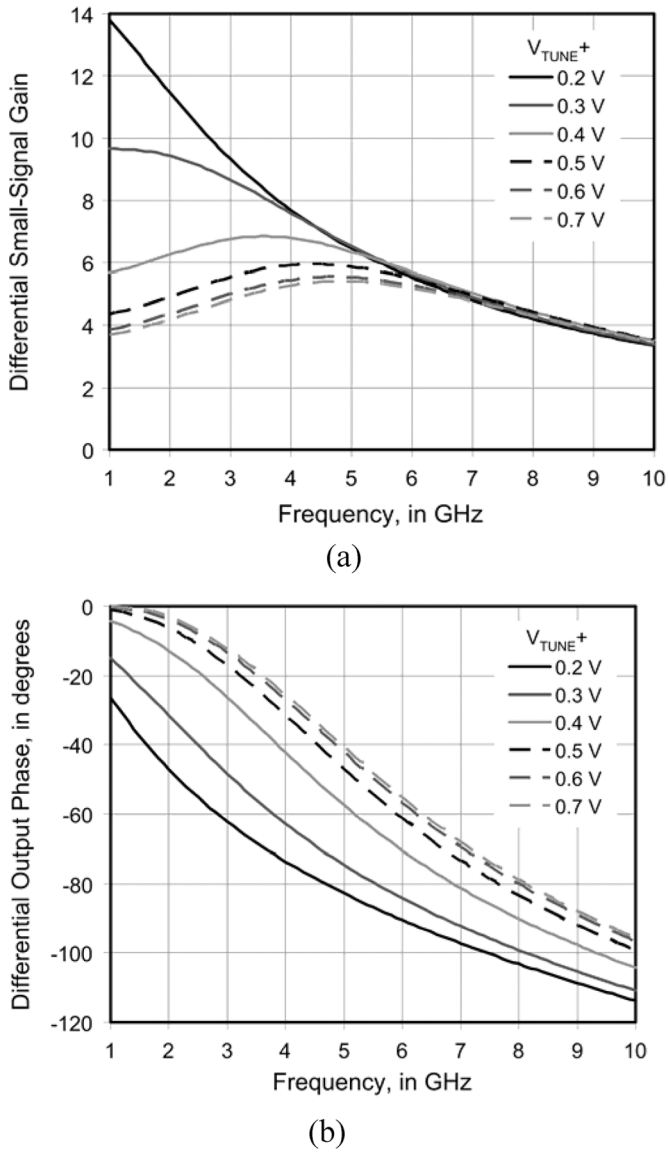

Fig. 5. Simulated performance of the phase shifter versus frequency for different $\mathrm{V_{TUNE}}+$: (a) small-signal gain, (b) output phase.

(i.e., W/L) or its current consumption. Given the high dissipation, the Q-factor of the active inductor (see (3)) is poor. Nevertheless, an inductance in the nano-Henry range is possible due to the multiplication of C_{gs} (typically tens of fF) by a factor of 10^5 (i.e., due to r_0^2). Moreover, the chip area required by this circuit is two orders of magnitude smaller than an on-chip passive inductor of the same inductance. The inductance of (2) is tuned by varying the bias current, and hence g_m of the transistor.

The simulated differential small-signal gain of the phase shifter including extracted parasitics with a resistively-loaded output buffer for varying $\mathrm{V_{TUNE}}+$ is plotted in Fig. 5(a). Minimum gate length transistors $\mathrm{M_3}$ and $\mathrm{M_4}$ are 30 μm wide, and R_1 and R_2 are 800 Ω. The total power consumption is 2 mW from a 1-V supply. It can be seen from the plots that the gain variation for different $\mathrm{V_{TUNE}}+$ decreases with increasing frequency. At 5 GHz, the gain changes from 5.4 to 6.5 as $\mathrm{V_{TUNE}}+$ is varied between 0.2 V and 0.7 V. Fig. 5(b) shows the corresponding differential output phase simulated for different $\mathrm{V_{TUNE}}+$. The phase variation also decreases with increasing frequency. At 5 GHz, the output phase changes from $-83°$ to $-40.6°$, giving 42.4° phase range in total. Monte Carlo simulation over 100 runs predicts that the phase range varies between 38.1° and 45°. Thus, two phase shifters in cascade provide more than 60° phase shift for $\mathrm{LO_{INJ}}$ (note that frequency tripling in each transmitter increases this phase range by 3x, to $>180°$), which also provides margin under process, voltage and temperature (PVT) variations. The small-signal range of the phase shifter decreases by just 25% (from simulation) when the circuit is used to phase shift a large-signal, such as the injected LO. It should be noted that the two sets of phase shifters give $\pm 180°$ phase shift at the RF output.

B. First LO Up-Conversion Mixer

Mixers $\mathrm{M_{1a}}$–$\mathrm{M_{1d}}$ in Fig. 2 up-convert the injected LO and phase shifter outputs. Fig. 6(a) depicts the functional diagram of this mixer, which consists of three identical combiner blocks [20]. Fig. 6(b) presents the schematic of each combiner. Differential inputs $\mathrm{V_A}(\mathrm{V_A}+, \mathrm{V_A}-)$ and $\mathrm{V_B}(\mathrm{V_B}+, \mathrm{V_B}-)$ are loaded equally in order to minimize any phase and amplitude errors between them. The voltage inputs are first converted to currents by $\mathrm{M_1}, \mathrm{M_2}$ and $\mathrm{M_3}, \mathrm{M_4}$, and then summed before driving a differential active inductor load realized by $\mathrm{M_5}, \mathrm{M_6}$ and R_1, R_2. The active inductor in this mixer has a bandpass response centered at twice the input frequency, which amplifies the desired up-converted outputs $\mathrm{V_{OUT}}+, \mathrm{V_{OUT}}-$ and attenuates any feedthrough from inputs $\mathrm{V_A}$ and $\mathrm{V_B}$. This differs from the implementation in [20], where resistors are used as loads in each combiner for frequency down-conversion.

The differential active inductor load in Fig. 6(b) offers common-mode rejection, unlike the single-ended phase shifter of Fig. 3. Fig. 7 shows the small-signal equivalent circuit. The differential input impedance looking into the source terminals of the two active devices (see the Appendix for derivation) is approximately

$$Z_{\mathrm{IN}}(s) \approx 2\left[\frac{1}{g_m} - (R//r_0)\right] + s\left\{\frac{2C_{gs}}{g_m}\left[2(R//r_0) - \frac{1}{g_m}\right] + 8C_{gd}(R//r_0)^2\right\} \quad (4)$$

where g_m is the transconductance of the transistor ($\mathrm{M_5}$ or $\mathrm{M_6}$ in Fig. 6), C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, respectively, r_0 is the transistor output resistance, and R is the load resistance (i.e., R_1 or R_2).

The active inductance is given by

$$L \approx \frac{2C_{gs}}{g_m}\left[2(R//r_0) - \frac{1}{g_m}\right] + 8C_{gd}(R//r_0)^2 \quad (5)$$

and its Q-factor is

$$Q_{\mathrm{active}} \approx \frac{C_{gs}\left[2(R//r_0) - \frac{1}{g_m}\right] + 4g_m C_{gd}(R//r_0)^2}{[1 - g_m(R//r_0)]}. \quad (6)$$

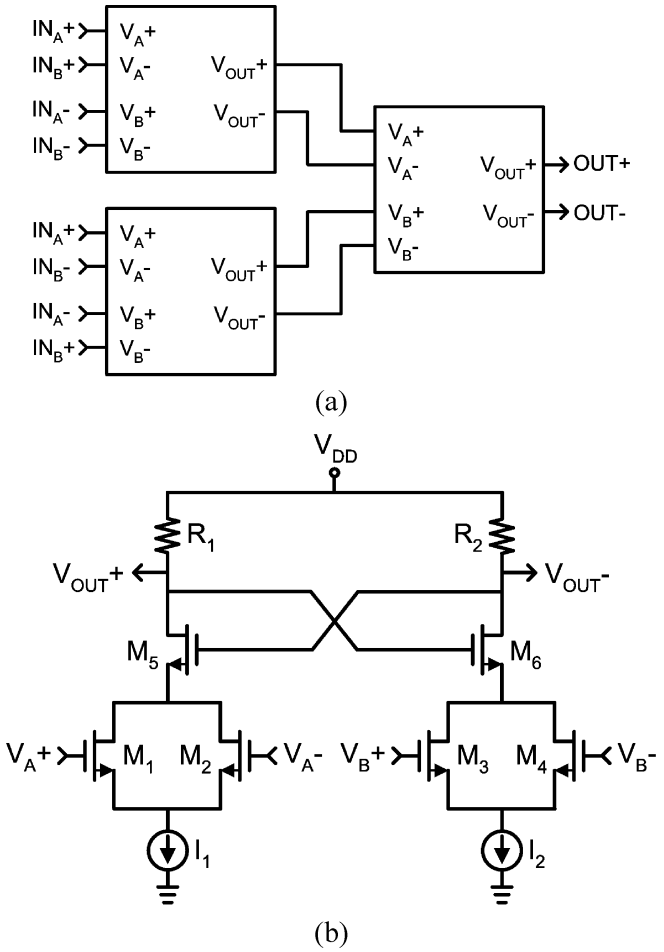

Fig. 6. First LO up-conversion mixer: (a) functional diagram, (b) schematic of the combiner subcircuit.

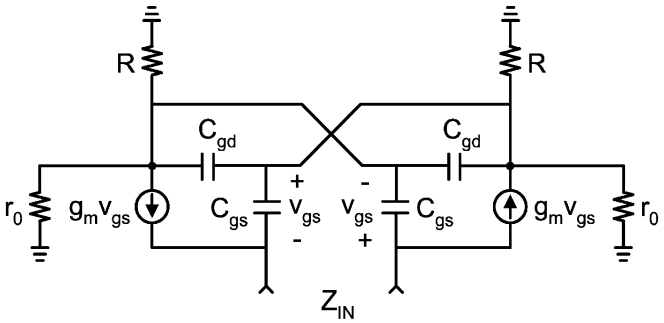

Fig. 7. Small-signal equivalent circuit of the differential active inductor used in the combiner of Fig. 6.

The inductance (5) is largely determined by $8C_{gd}(R//r_0)^2$, which gives a few nano-Henrys of inductance due to the multiplication of C_{gd} (in the tens of fF) by a factor of 10^5 (i.e., due to $(R//r_0)^2$). In contrast to the single-ended active inductor analyzed previously, changing transconductance g_m (which dominates in (2)) does not vary the inductance significantly. The real part of input impedance given by (4) is negative when $g_m(R//r_0) < 1$. Therefore, the transistor transconductance can be chosen to give a small net positive resistance in order to achieve a high Q factor as seen from the denominator of (6) $(g_m(R//r_0) \rightarrow 1)$.

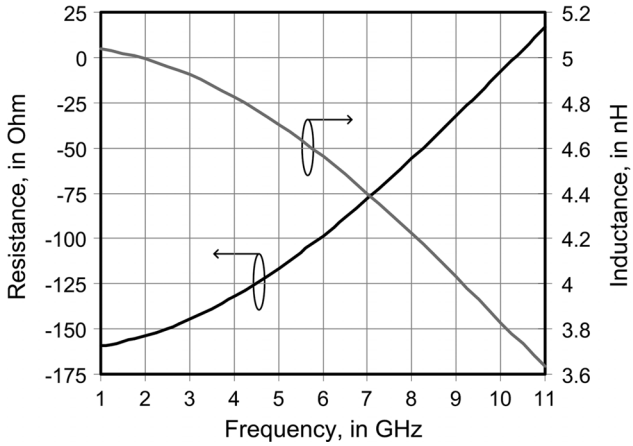

Fig. 8. Simulated resistance and inductance of a differential active inductor across frequency.

Fig. 8 illustrates the simulated resistance and inductance, including extracted parasitics, of the differential active inductor used in each combiner. Minimum gate length transistors M_5 and M_6 are 16 μm wide, and R_1 and R_2 are 250 Ω. The negative resistance decreases with increasing frequency as the transistor output resistance becomes smaller due to the drain–bulk parasitic capacitance (not included in the small-signal circuit of Fig. 7). Note that the resistance becomes positive beyond 10.4 GHz. The inductance also decreases with increasing frequency due to the same effect. At 10 GHz (i.e., twice the operating frequency of the phase shifters), the differential active inductor provides 3.8 nH inductance to tune out the capacitive loading of the two current summers ($\mathrm{M}_1, \mathrm{M}_2$ and $\mathrm{M}_3, \mathrm{M}_4$). This minimizes the loss of the combiner, thus giving a larger output signal swing for a given power consumption. The mixer with its output buffer provides approximately 700 mV differential swing at 10 GHz with a power consumption of 6 mW from a 1-V supply.

C. Second LO Up-Conversion Mixer

Resistively-loaded differential buffers increase the output swing from the first up-conversion stage ($\mathrm{LO_{V1}}$, $\mathrm{LO_{V2}}$ and $\mathrm{LO_{H1}}$, $\mathrm{LO_{H2}}$ in Fig. 2) in order to drive the second stage of frequency translation (mixers $\mathrm{M_{2a}}$–$\mathrm{M_{2d}}$). This up-conversion to 1/3rd of the desired LO frequency is performed by 6-transistor Gilbert-type mixers with tuned passive inductor loads. The phases of the input signals from the first two respective up-conversions are summed at the loads to generate subharmonics, $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$. Each mixer, including the buffers, consumes 7.5 mA from a 1-V supply.

Fig. 9 illustrates how the phases of the simulated transient waveforms $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$ change with differential phase tuning. As $\mathrm{V_{TUNE-V}}$ (i.e., $\mathrm{V_{TUNE-V}} + -\mathrm{V_{TUNE-V}}-$) increases, $\mathrm{LO_{T1}}$ and $\mathrm{LO_{T2}}$ lag $\mathrm{LO_{T3}}$ and $\mathrm{LO_{T4}}$ with a maximum phase difference of more than 60° in Fig. 9(a). With decreasing $\mathrm{V_{TUNE-V}}$, $\mathrm{LO_{T1}}$ and $\mathrm{LO_{T2}}$ lead $\mathrm{LO_{T3}}$ and $\mathrm{LO_{T4}}$, with a maximum phase variation above $-60°$. The frequency tripler in each transmitter increases the phase tuning range by 3x, to approximately $\pm 180°$. Likewise, increasing $\mathrm{V_{TUNE-H}}$ (i.e., $\mathrm{V_{TUNE-H}} + -\mathrm{V_{TUNE-H}}-$) gives a maximum phase variation of more than $\pm 60°$ in the 10-GHz band between $\mathrm{LO_{T1}}$ and

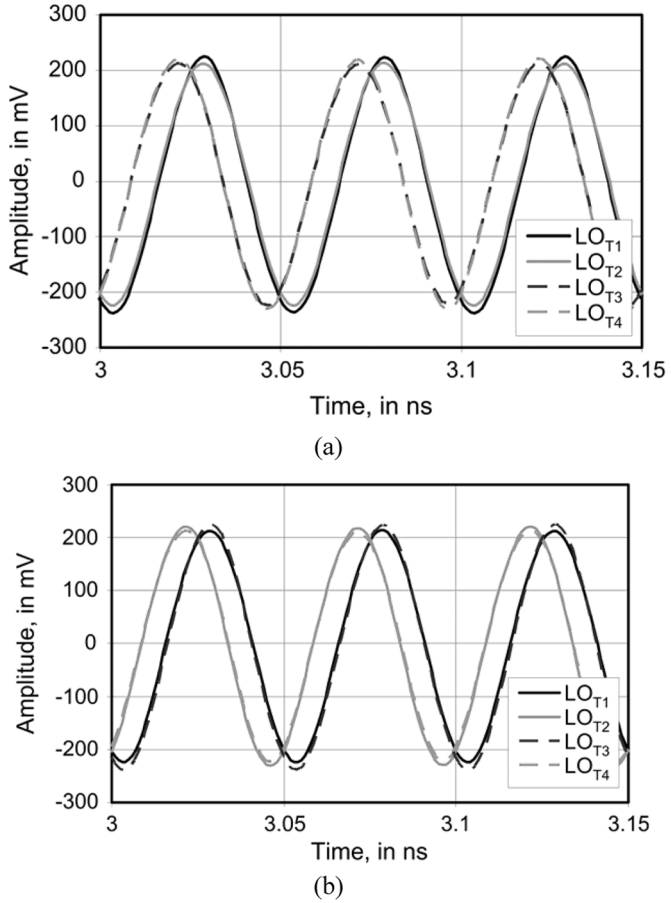

Fig. 9. Transient waveforms of $\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$ with differential phase tuning: (a) $\mathrm{V_{TUNE-V}} = 0.5$ V, (b) $\mathrm{V_{TUNE-H}} = 0.5$ V.

$\mathrm{LO_{T3}}$, and $\mathrm{LO_{T2}}$ and LO_{T4} as seen in Fig. 9(b). Fig. 10 shows how the simulated phase variation between the transmitted outputs $\mathrm{RF}_1, \mathrm{RF}_2$ and $\mathrm{RF}_3, \mathrm{RF}_4$ in Fig. 2 varies with differential tuning of $\mathrm{V_{TUNE-V}}$. The phase difference between $\mathrm{RF}_1, \mathrm{RF}_3$ and $\mathrm{RF}_2, \mathrm{RF}_4$ with differential tuning of $\mathrm{V_{TUNE-H}}$ is identical. The RF output power changes by less than 0.01 dB over the entire phase tuning range. Thus, simultaneous tuning of $\mathrm{V_{TUNE-V}}$ and $\mathrm{V_{TUNE-H}}$ introduce phase variations among $\mathrm{RF_1}$–$\mathrm{RF_4}$ that enable beam steering in any direction above the plane of the antenna array.

D. I/Q Generator

The respective outputs from the second LO up-conversion ($\mathrm{LO_{T1}}$–$\mathrm{LO_{T4}}$) each drives a differential pair loaded by a two-stage *RC* polyphase filter (PPF) with inductive termination (see Fig. 11). The 20-GHz band quadrature outputs ($\mathrm{INJ_I+}, \mathrm{INJ_I-}$ and $\mathrm{INJ_Q+}, \mathrm{INJ_Q-}$) of the PPF injection-lock the frequency tripler. Driving the PPF with a current instead of a voltage source minimizes distortion of the signal waveforms for a given power consumption, especially at high frequency. The filter outputs drive symmetric load inductors ($\mathrm{L_1}, \mathrm{L_2}$ and $\mathrm{L_3}, \mathrm{L_4}$), which provide some much needed common-mode rejection that helps to maintain symmetry between the differential signals. The inductors also tune out parasitic capacitance in the circuit.

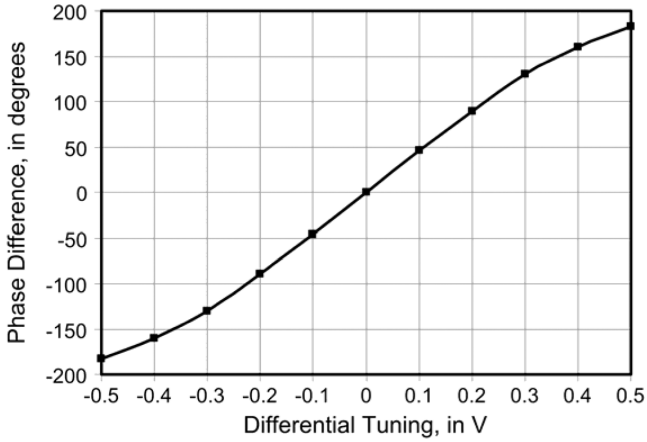

Fig. 10. Phase variation at the 60-GHz band RF outputs with differential tuning of $\mathrm{V_{TUNE-V}}$ (or $\mathrm{V_{TUNE-H}}$).

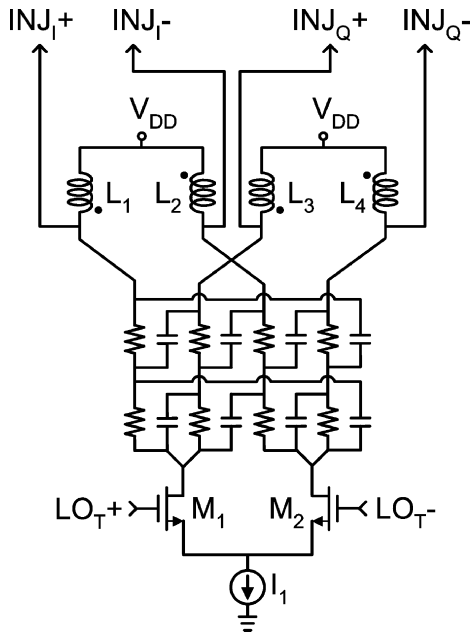

Fig. 11. Schematic of the I/Q generator.

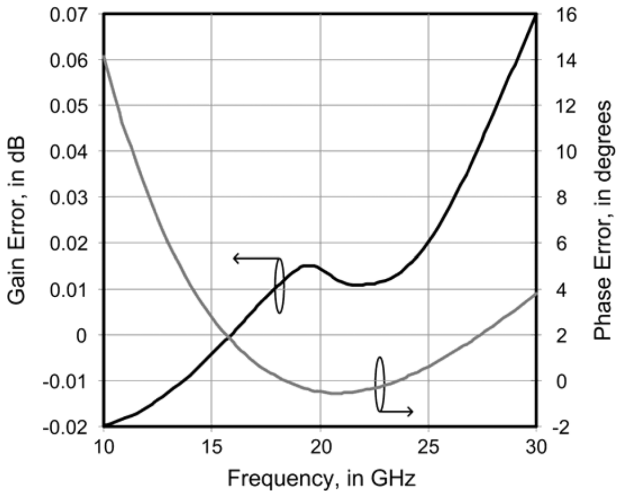

Fig. 12. Simulated gain and phase errors of the I/Q generator.

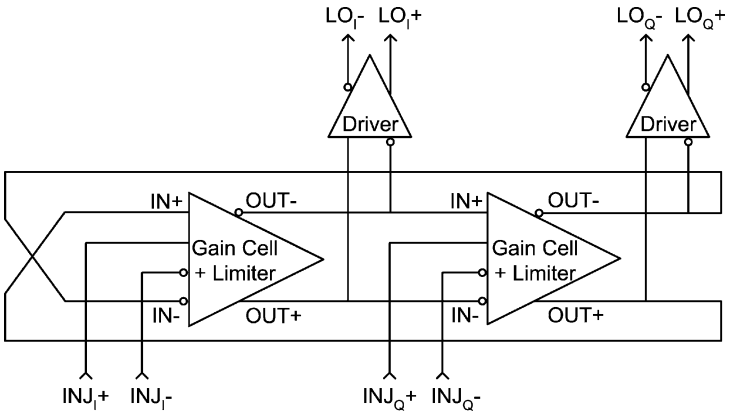

Fig. 13. Block diagram of the injection-locked frequency tripler.

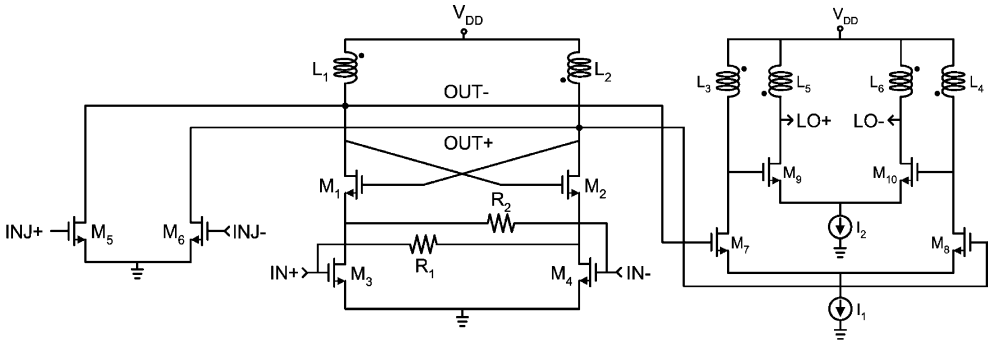

Fig. 14. Schematic of oscillator gain stage and limiter with output driver.

To ensure proper operation under PVT variations, three-stages of buffering with inductively-tuned differential pairs amplify the I/Q outputs and drive the tripler with more than 300 mV-pk. The I/Q generator (including PPF) consumes 10 mA, while each buffer consumes 5 mA, all from a 1-V supply. Simulation with extracted parasitics shows output quadrature and amplitude errors smaller than 1° and 0.02 dB, respectively, across the 17–25 GHz input range (see Fig. 12).

E. Frequency Tripler

The tripler consists of identical self-oscillating differential cores connected in cascade to form a ring oscillator [21] that free-runs at 60 GHz, as shown in Fig. 13. The buffered outputs drive an I/Q baseband-to-RF up-conversion mixer. Each stage provides 90° phase shift, while the feedback connection adds another 180° for a total loop phase shift of 360°.

Fig. 14 shows the circuit implementation of the gain cell with a differential hard limiter and the output driver. The negative resistance cell incorporates positive feedback loops around $\mathrm{M}_1, \mathrm{M}_2$ and $\mathrm{M}_3, \mathrm{M}_4$ (via R_1, R_2) to increase the overall loop gain of the ring oscillator without increasing the power consumption. R_1 and R_2 load the inductor of the preceding stage, thereby lowering its Q-factor and increasing the injection-locking range. Differential limiting amplifier $\mathrm{M}_5, \mathrm{M}_6$ is driven from inputs $\mathrm{INJ}+, \mathrm{INJ}-$ via the I/Q generator to produce the third harmonic that injection locks each stage. Class-B biasing of M_5 and M_6 maximizes the third harmonic content of the signal.

Regenerative peaking of the output driver reduces its power consumption and optimizes the frequency response of the buffer. Differential pair $\mathrm{M}_7, \mathrm{M}_8$ is cascaded with a second differential amplifier $\mathrm{M}_9, \mathrm{M}_{10}$. Each pair is biased independently by its own current source (I_1 and I_2, respectively). Positive feedback via load transformers L_3–L_5 and L_4–L_6 increases the gain and signal driving capability of M_9 and M_{10} without increasing the bias current consumption. The buffer provides more than 400 mVpp output swing to drive the RF up-conversion mixer. The positive feedback between the primary and secondary coils of the transformer is not strong enough to cause self-oscillation (magnetic coupling factor, $\mathrm{k} = 0.3$), but narrows the circuit bandwidth.

The tripler consumes 10 mA, while its output driver requires another 10 mA, all from a 1-V supply. The simulated phase and amplitude errors between the quadrature outputs of the tripler (including extracted parasitics) are smaller than 1° and 0.2 dB, respectively, which corresponds to a sideband suppression of more than 35 dBc when used with an ideal I/Q up-converter.

F. RF Up-Conversion Mixer

Fig. 15 shows the differential quadrature mixer which up-convert the baseband inputs ($\mathrm{BB_I}+, \mathrm{BB_I}-$ and $\mathrm{BB_Q}+, \mathrm{BB_Q}-$) to the RF band (i.e., transmit signal $\mathrm{RF}+, \mathrm{RF}-$). LO driving signals $\mathrm{LO_I}+, \mathrm{LO_I}-$ and $\mathrm{LO_Q}+, \mathrm{LO_Q}-$ are generated by the I/Q tripler. Full current bleeding suppresses up-conversion of flicker noise by reducing the DC bias current flowing through the switching quad transistors to zero. Consequently, only leakage current flows through the switching quads (M_3–M_6

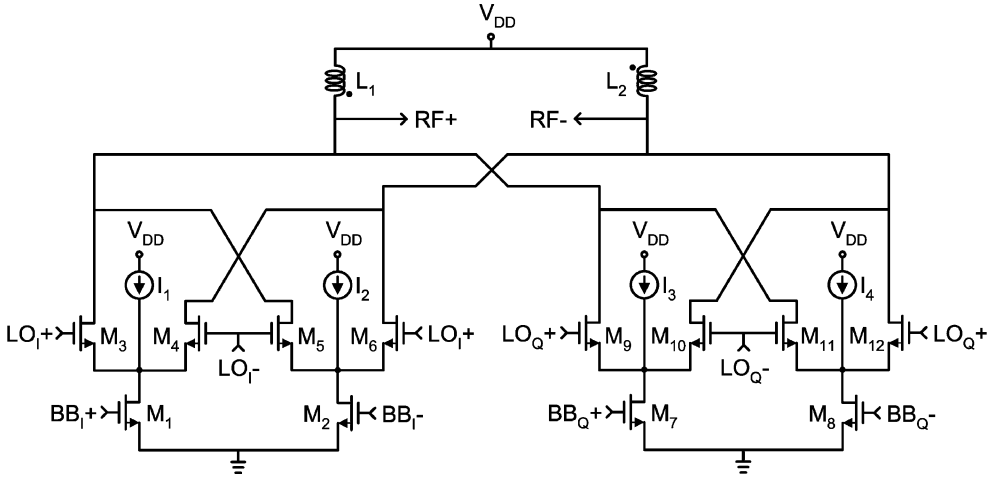

Fig. 15. I/Q up-conversion mixer with current bleeders.

and $\mathrm{M_9}$–$\mathrm{M_{12}}$), which reduces the simulated flicker noise corner frequency from about 40 MHz to approximately 4 MHz in the 65-nm CMOS technology. Bleeding current sources ($\mathrm{I_1}$–$\mathrm{I_4}$) supply DC current to transconductance pairs ($\mathrm{M_1}, \mathrm{M_2}$ and $\mathrm{M_7}, \mathrm{M_8}$) [22]. Higher quiescent currents can be used to increase the transconductance of $\mathrm{M_1}, \mathrm{M_2}$ and $\mathrm{M_7}, \mathrm{M_8}$, thereby increasing the conversion gain of the up-converting I/Q mixer without raising the supply voltage, as the voltage drop across the switching quad transistors remains constant. The I/Q mixer consumes 15 mA from a 1-V supply.

Carrier feedthrough occurs because the differential LO signal leaks to the RF output due to asymmetry in the switching quad transistors when they are driven large-signal. Dynamic DC biasing of the differential LO inputs corrects for LO amplitude mismatch and suppresses this carrier leakage. Fig. 16 shows the biasing circuitry for both the $\mathrm{LO_I}$ and $\mathrm{LO_Q}$ inputs of the I/Q mixer. It senses the amplitude difference between the $\mathrm{LO+}$ and $\mathrm{LO-}$ signals by converting the voltage inputs into a current via differential pair $\mathrm{M_1}, \mathrm{M_2}$ to give a voltage difference at the drains of $\mathrm{M_3}$ and $\mathrm{M_4}$. The upconverting mixer LO inputs (and the gates of transistors $\mathrm{M_1}$ and $\mathrm{M_2}$) then see this difference as they are biased from the drain nodes of $\mathrm{M_1}$ and $\mathrm{M_2}$ via resistors R_1 and R_2. Dynamic LO bias increases carrier suppression at the mixer RF nodes from 20 dBc to more than 25 dBc (from simulation with extracted parasitics).

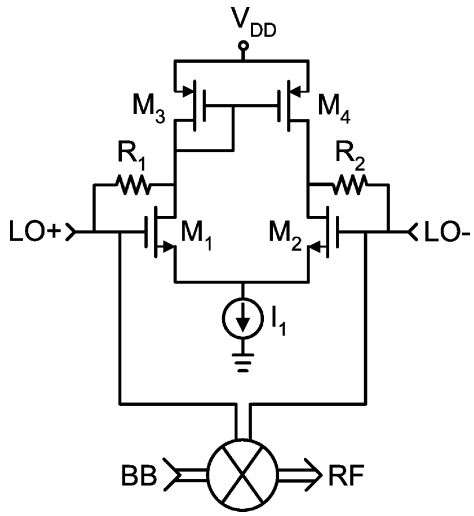

Fig. 16. LO biasing circuitry.

G. Power Amplifier

The mixer differential outputs $(\mathrm{RF+}, \mathrm{RF-})$ drive a transformer-coupled three-stage neutralized PA with an integrated 50-Ω to RF output balun [23], as shown in Fig. 17. The first two driver stages are designed for maximum gain, while the last stage is optimized for output power. Each stage consists of a neutralized pseudo-differential amplifier. Common-source (i.e., non-cascode) stages allow maximum signal swing within each amplifier to achieve high gain and power-added efficiency (PAE) under low voltage operation.

Neutralization with cross-coupled drain-gate feedback capacitors is applied to mitigate the Miller effect and increase the isolation between stages [23], [24]. The neutralizing capacitors are implemented using interdigitated backend metal-insulator-backend metal capacitors. MOS (transistor) neutralizing capacitors, which would track the active device parasitics under PVT variations, are not used because they introduce extra parasitics that may cause instability at 60 GHz (from simulation). In each stage, the neutralizing capacitance is slightly smaller than the device gate-drain capacitance [23] so that the PA remains unconditionally stable (in simulation), even with $\pm 20\%$ variation in each neutralizing capacitance value. The amplifier stages are coupled to each other through 2 overlaid transformer windings (top and second metals) in order to maximize the magnetic coupling within the smallest chip area. Floating metal shielding strips [25] placed beneath the windings reduce power losses from the coupling and output transformers to the substrate. The overall power amplifier, while consuming 55 mA from a 1-V supply, is unconditionally stable from Monte Carlo simulation of 100 runs with Rollett's stability factor, $\mathrm{K} > 1$ (smallest K of 12 at 56 GHz) and $|\Delta|$ (determinant of the S-parameter matrix) less than 1 from DC to 100 GHz.

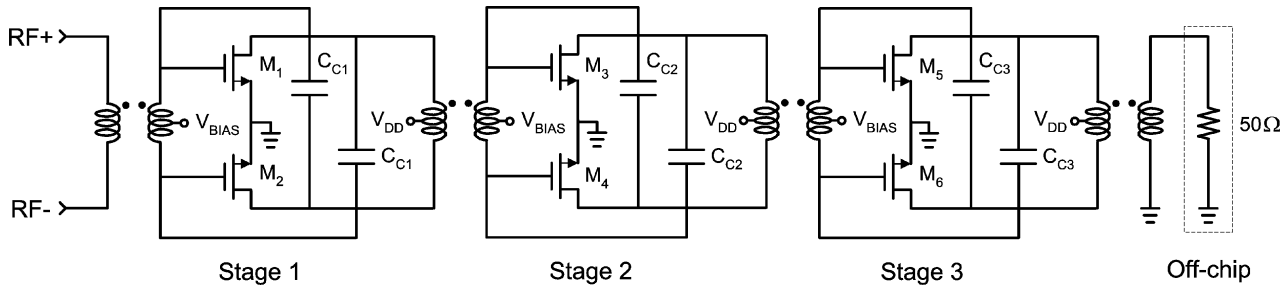

Fig. 17. Schematic of the three-stage neutralized power amplifier.

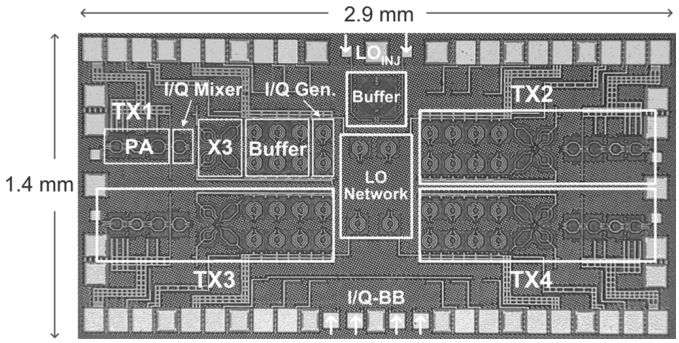

Fig. 18. Microphotograph of the phased-array transmitter test chip.

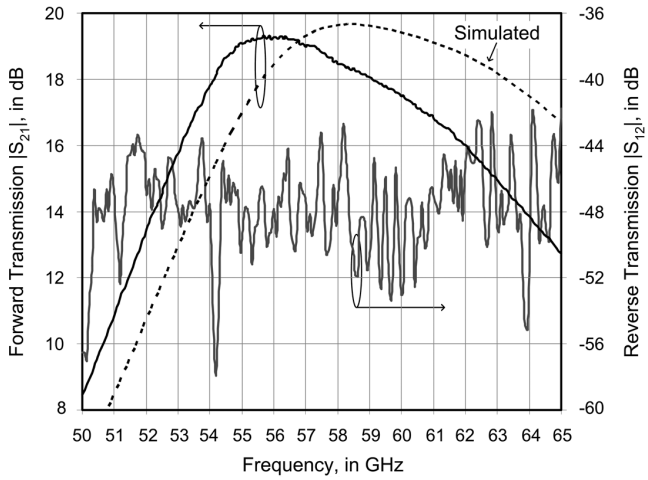

Fig. 19. Measured S_{21} and S_{12} of the standalone PA.

IV. Experimental Results

A microphotograph of the fully-differential 2×2 phased-array transmitter is shown in Fig. 18. The chip is fabricated in a production 65-nm bulk CMOS process with nine metal layers available for interconnections [26]. All of the on-chip magnetic components (i.e., inductors and transformers) are realized with the top two metals (1.3-μm and 0.4-μm thickness, respectively) above a floating bottom metal shield on a 1 Ω-cm substrate. The top metal is less than 7 μm above the silicon substrate. All capacitors are implemented as interdigitated vertical parallel-plate backend metal. No process-option MIM capacitors are used. The 2.9×1.4 mm^2 (including bondpads) prototype is attached and wirebonded to a custom PCB to facilitate DC and low frequency connectivity, while all RF inputs/outputs are on-die probed.

The transformer-coupled, three-stage neutralized PA has been separately characterized. The measurement setup and procedures are the same as detailed in [23]. Fig. 19 shows the measured S_{21} and S_{12} of the PA when operating from a 1-V supply. A peak small-signal (S_{21}) gain of 19 dB at 56 GHz agrees well with the simulated peak S_{21} of 19.5 dB at 58 GHz. The -3-dB bandwidth lies between from 53 GHz to 62 GHz, or approximately 9 GHz. The PA gain makes up for the low up-conversion gain of the mixer in the transmitter. The reverse transmission or S_{12} of the PA is lower than -42 dB from 50 GHz to 65 GHz (simulated S_{12} equals -67 dB, without accounting for substrate coupling or effects of the external test setup), which greatly reduces the possibility of oscillation and LO pulling by the PA due to the high isolation seen between its input and output.

The measured large-signal behavior of the PA used in the transmitter at a single frequency (57 GHz) is presented in Fig. 20. A saturated output power $(\mathrm{P}_{\mathrm{sat}})$ of more than 10 dBm is realized. The maximum power-added efficiency (PAE) of about 20% occurs at an output power approximately 10 dBm with 13 dB (compressed) gain. The input power at -1 dB of gain compression $(\mathrm{P}_{1\mathrm{dB}})$ is -10 dBm, corresponding to 8 dBm output power at a PAE of 14%. Fig. 21 plots the measured performance of the PA from 50 GHz to 65 GHz in steps of 1 GHz. From 54–63 GHz, the peak PAE is more than 15%, while the corresponding output power at which the maximum PAE occurs is better than 9 dBm. Note that the decrease in the PAE and output power at 62 GHz is due to the inability of test source to drive the PA into compression at this frequency.

The 4.1-mm^2 phased-array transmitter IC consumes a total of 590 mW from a 1-V supply. Fig. 22 shows the measured output spectrum of one of the four transmitters with an IF of 1.7 GHz (i.e., the occupied bandwidth of the IEEE 802.15.3c-2009 high-rate physical layer). The I/Q IF input to the device under test (DUT) is split on-chip without amplification to drive the four transmitters. The LO leakage is at the free-running carrier frequency of each transmitter, which varies between 56.4 GHz and 57.1 GHz for TX1–TX4 from 10 samples tested. Carrier suppression is 20.5 dBc $\pm$0.5 dB and sideband rejection of 25 to 28 dBc is measured among the 4 transmitters on the same die. Spurs are more than 30 dB below the RF output power of 6.5 dBm. They may be caused by the circuit itself, added by the external down-conversion mixer used for measurement, and introduced by the part of the test setup that provides the baseband

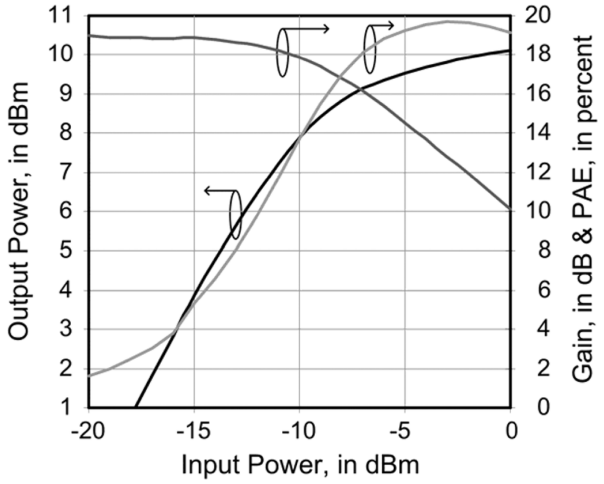

Fig. 20. Output power, gain and PAE of the PA versus input power at 57 GHz.

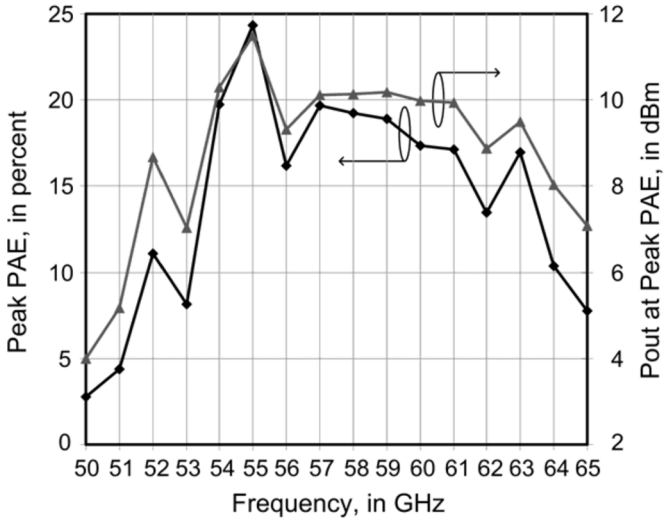

Fig. 21. Measured peak PAE and output power at which peak PAE occurs versus frequency.

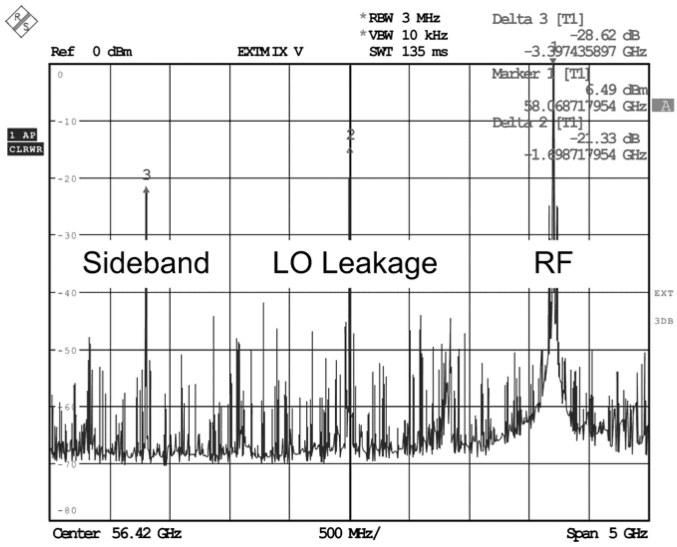

Fig. 22. Measured frequency spectrum at one transmitter output.

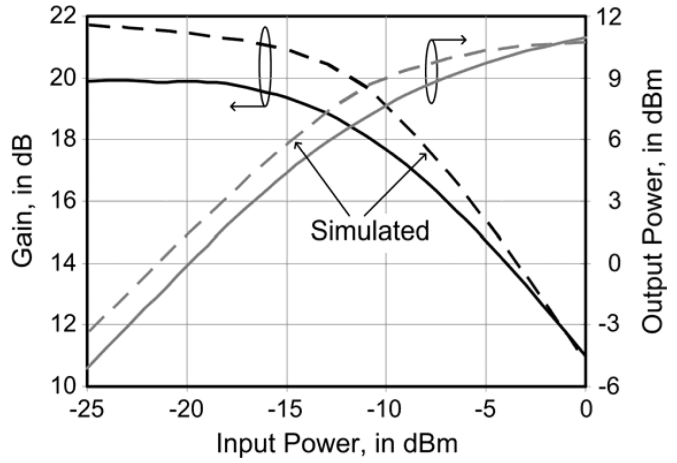

Fig. 23. Measured and simulated transmitter gain and output power at 58 GHz.

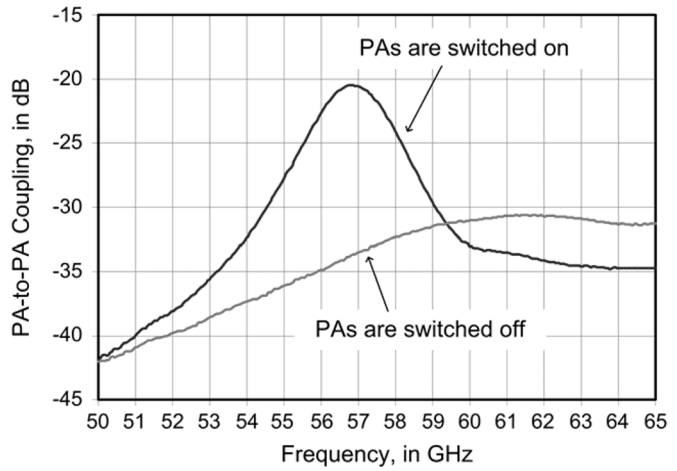

Fig. 24. PA-to-PA coupling between adjacent transmitters on the same side of the die.

inputs to the transmitter IC. Fig. 23 shows the measured performance of one transmitter upconverting an IF of 1.7 GHz to RF at 58 GHz (without IF amplification). A total gain of 20 dB (simulated 21.7 dB) is achieved with $\mathrm{P_{sat}}$ of 11 dBm. The output power at 1-dB compression is about 6 dBm. The large-signal -3-dB bandwidth is 5 GHz. Isolation between adjacent transmitters on the same side of the die is limited by coupling between the RF output bondpads (i.e., to facilitate probing with 150 μm pitch). It is greater than 20 dB when both PAs are active (see Fig. 24).

The measured phase noise of the RF output at 58 GHz under sub-harmonic injection locking is plotted in Fig. 25 together with the phase noise of the injected LO source (4.7 GHz) for comparison. The phase noise of the IF generator at 100-kHz offset from the 1.7-GHz carrier frequency is -136 dBc/Hz. This is much lower than the phase noise of the 4.7-GHz source used to provide the injected LO, and therefore does not affect the phase noise of the up-converted RF output. At 100-kHz offset, the measured phase noise difference between the injected LO and RF transmit output is approximately 23.3 ± 1 dB. This is only 1.7 dB away from the ideal 21.6 dB difference (i.e., $20 \log_{10}$ [12]) caused by multiplication of the source frequency by a factor of 12. The RF output phase noise curve

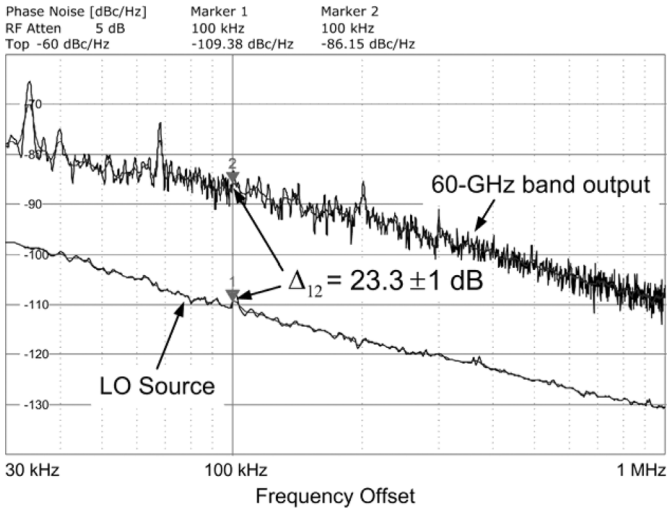

Fig. 25. Measured phase noise of the LO source and RF output.

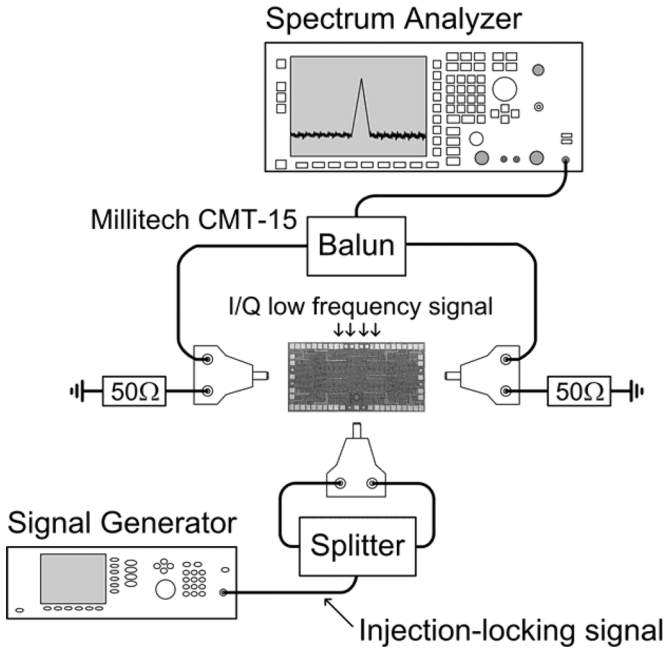

Fig. 26. Phase measurement test setup.

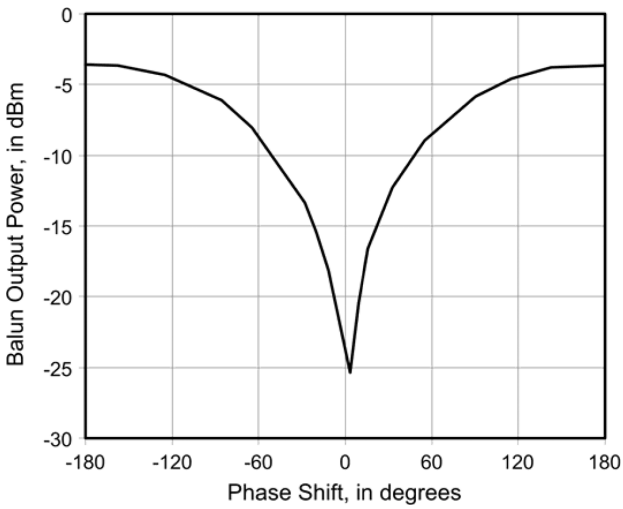

Fig. 27. Measured balun output power variation with differential tuning of V_{TUNE-V} between TX1 and TX3 signals.

reaches the thermal noise floor of the test setup (approximately -120 dBc/Hz) at about 2-MHz offset.

Fig. 26 shows the measurement setup used to determine the phase variation between the RF outputs (i.e., RF_1–RF_4) as the phase tuning inputs V_{TUNE-V} and V_{TUNE-H} are varied differentially. Since the IF inputs are up-converted from 1.7 GHz to 58 GHz (i.e., frequency offset from the transmit outputs), a network analyzer is not used for phase characterization as it is not possible to phase-lock all of the test signal sources. Instead, an external balun was used to determine the phase change indirectly. No discrete phase-shifters are used. The balun (ideally) outputs 3 dB more power when both inputs are antiphase, whereas the signals cancel each other at the output node of the balun (giving a null in the RF signal) when the inputs are in-phase. As the phase between the 2 inputs to the balun varies from in-phase to antiphase, the output power will also vary according to the phase relationship. By characterizing this behavior of the balun separately to account for its phase and amplitude imperfections, and knowing the RF input power and output power from the balun, the phase relationship between the balun inputs may be deduced.

In order to measure phase relationship between the outputs, the phased-array transmitter is first injection-locked at $1/12$th of the carrier frequency to maintain a stable RF output at 58 GHz. The measured output power of transmitters RF_1–RF_4 changes by less than ± 0.5 dB with respect to each other as V_{TUNE-V} or V_{TUNE-H} is adjusted. Each pair of transmitter outputs is then summed using an external balun, while the other two outputs are terminated with 50-Ω loads. The variation in the RF output power with phase tuning is then measured with a spectrum analyzer. The associated phase change is determined from simulation based on the measured transmitter output power and the characterized S-parameter data of the balun (i.e., the measured balun data shows the differential phase and amplitude errors varying between 10° and 0.2 dB, respectively, from 52 to 65 GHz). A phase shifter is inserted before one input of the balun (driven by the transmitter output power) in simulation, and its phase is adjusted until the simulated balun output power is close to, or equals the measured value. This establishes the amount of phase variation introduced by tuning either V_{TUNE-V} or V_{TUNE-H}. Fig. 27 is an example plot which illustrates the change in measured balun output power with differential tuning of V_{TUNE-V} between TX1 and TX3 signals at an output power of approximately -5 dBm. The null in the balun output power occurs close to a phase shift of 0°, indicating only a small phase mismatch between the TX1 and TX3 signals.

Fig. 28 presents the synthesized array patterns for both vertical (a) and horizontal (b) steering from the measured transmitter output power and its associated phase, assuming ideal antennas separated by one-half wavelength. The synthesized patterns are in good agreement with the theoretical predictions, indicating only small phase and amplitude mismatches between

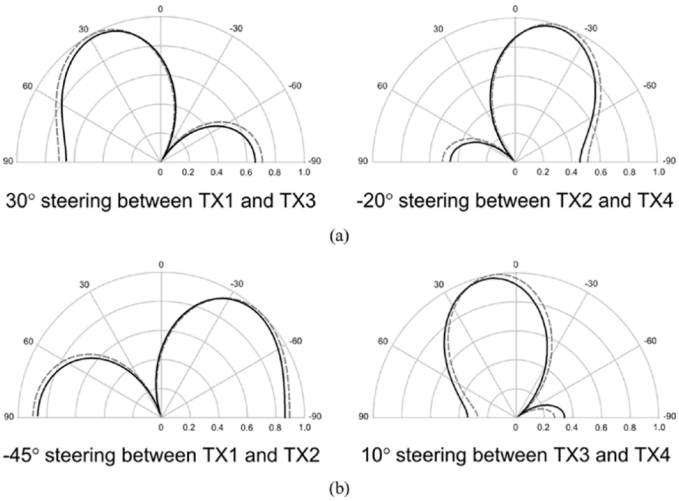

Fig. 28. Synthesized two-element array patterns (solid traces computed from measured data, dashed traces are theoretical predictions): (a) vertical steering, (b) horizontal steering.

TABLE I
PERFORMANCE SUMMARY

Transmitter

Maximum Output Power / Channel	11 dBm
PA Peak PAE	> 15%
Gain	20 dB
-3-dB Bandwidth	5 GHz
Carrier Suppression	20.5 dBc ± 0.5 dB
Sideband Rejection	25-28 dBc

Power Consumption

PA + I/Q Mixer (4x)	4 x 70 mW @ 1 V
Tripler + I/Q Generator including buffers (4x)	4 x 60 mW @ 1 V
First LO Up-Conversion with buffers (2x)	2 x 20 mW @ 1 V
Second LO Up-Conversion with buffers (1x)	30 mW @ 1 V
2 x 2 Phased-Array Transmitter	590 mW @ 1 V

Chip Area	2.9 x 1.4 mm^2
Technology	65-nm CMOS

the four transmitter outputs as either V_{TUNE-V} or V_{TUNE-H} is differentially tuned.

The experimental results of the 2×2 phased-array transmitter are summarized in Table I. The prototype allows $\pm 180^{\circ}$ phase shift for full beam steering, while consuming 590 mW from a 1-V supply. Each transmit channel provides up to 11 dBm output power with 20 dB gain.

Table II compares the measured performance of the phased-array transmitter designed in this work to prior silicon-based realizations for the 60-GHz band. Each implementation adopts a different phase-shifting architecture. It should be noted that the phased-array transmitter of [27] up-converts an applied differential IF input at 12 GHz to 60 GHz (i.e., a single-stage up-conversion but without I/Q mixing) with an external LO at 48 GHz. This accounts for its lower power consumption per channel, as the design also has smaller gain and output power unlike the design reported in [28] and this work, where the differential I/Q baseband inputs are directly upconverted to 60 GHz. This implementation achieves higher gain and saturated output power with moderate power consumption and chip area by making extensive use of active inductors under low voltage operation.

TABLE II
PHASED-ARRAY TRANSMITTER PERFORMANCE COMPARISON

Reference	[27]	[28]	This work
Frequency [GHz]	60	60	60
P_{sat} / element [dBm]	3.5	6	11
Gain / element [dB]	7	15	20
P_{DC} / element [mW]	19.5	160	147.5
Total P_{DC} [mW]	78 @ 1.3 V	960 @ 1 V	590 @ 1 V
Area [mm^2]	1.6 (Inc. LNA)	12.5	4.06
Technology	90-nm CMOS	90-nm CMOS	65-nm CMOS
Notes	4-channel TX, Ext. LO @ 48 GHz, RF Phase-Shifting	6-channel TX, with PLL, IF Phase-Shifting	4-channel TX, LO Phase-Shifting

V. CONCLUSION

A four-output phased-array transmitter capable of phase tuning for vertical and horizontal steering of the beam radiated by a 2×2 antenna array was implemented in a production 65-nm bulk CMOS technology. This design can easily be scaled to higher order in order to drive a larger antenna array. The fully-differential design reduces potential instability in this multi-transmitter design operating in the mm-wave regime. LO phase shifting of the four transmitters is preferred due to the low transconductance of the active devices, which consumes much power to provide amplification. Active inductors are used extensively in the phase shifters and mixers to up-convert the injected LO at $1/12$th of the carrier frequency to four phase-tuneable outputs at $1/3$rd of the final LO frequency. They require 2 orders of magnitude less silicon area, unlike their passive equivalents. The input LO injection-locks a tripler to generate quadrature outputs in the 60-GHz band for a single up-conversion of the baseband inputs. Flicker noise of the mixer is suppressed by full current bleeding, whereas carrier feedthrough is minimized by dynamic LO biasing. The power amplifier exploits neutralization to mitigate the Miller effect, thus simultaneously achieving unconditional stability and high isolation. From a 1-V supply, the prototype provides four channels with maximum output of 11 dBm and 20 dB gain per transmitter, while consuming 590 mW. Measured carrier suppression and sideband rejection is 20.5 dBc ± 0.5 dB and 25 to 28 dBc, respectively, among the four RF outputs of the phased-array transmitter. The measured phase noise difference is 23.3 ± 1 dB with respect to a 4.7-GHz injected source.

APPENDIX

The input impedance of the active inductor from the small-signal equivalent circuit of Fig. 4 is given by

$$Z_{\rm IN}(s)=\frac{\frac{1}{R}+s(C_{gs}+C_{gd})}{\frac{1}{R}\left(g_m+\frac{1}{r_0}\right)+s\left[C_{gd}\left(g_m+\frac{1}{r_0}\right)+C_{gs}\left(\frac{1}{R}+\frac{1}{r_0}\right)\right]}. \tag{7}$$

Multiplying the numerator and denominator of (7) by the complex conjugate of its denominator yields a result which can be partitioned into real (dissipation) and imaginary (inductive reactance) parts. Assuming

$$\left(\frac{1}{R}\right)^2\left(g_m+\frac{1}{r_0}\right)\gg\omega^2(C_{gd}+C_{gs})\times\left[C_{gd}\left(g_m+\frac{1}{r_0}\right)+C_{gs}\left(\frac{1}{R}+\frac{1}{r_0}\right)\right]$$

in the numerator and

$$\left[\frac{1}{R}\left(g_m+\frac{1}{r_0}\right)\right]^2\gg\omega^2\left[C_{gd}\left(g_m+\frac{1}{r_0}\right)+C_{gs}\left(\frac{1}{R}+\frac{1}{r_0}\right)\right]^2$$

in the denominator, giving

$$Z_{\rm IN}(s)\approx\frac{\left(\frac{1}{R}\right)^2\left(g_m+\frac{1}{r_0}\right)+s\left[\frac{C_{gs}}{R}\left(g_m-\frac{1}{R}\right)\right]}{\left[\frac{1}{R}\left(g_m+\frac{1}{r_0}\right)\right]^2} \tag{8}$$

which is equivalent to (1).

The differential input impedance of the active inductor of Fig. 7 is

$$Z_{\rm IN}(s)=\frac{2\left[\frac{1}{(R//r_0)}-g_m\right]+s(2C_{gs}+8C_{gd})}{(g_m+sC_{gs})\left[\frac{1}{(R//r_0)}+s(4C_{gd})\right]}. \tag{9}$$

Since $(g_m)/((R//r_0))\gg 4\omega^2C_{gs}C_{gd}$, (9) can be approximated by

$$Z_{\rm IN}(s)\approx\frac{2\left[\frac{1}{(R//r_0)}-g_m\right]+s(2C_{gs}+8C_{gd})}{\frac{g_m}{(R//r_0)}+s\left[\frac{C_{gs}}{(R//r_0)}+4g_mC_{gd}\right]}. \tag{10}$$

Multiplying both the numerator and denominator of (10) by the conjugate of the denominator, and assuming

$$\frac{g_m}{(R//r_0)}\left[\frac{1}{(R//r_0)}-g_m\right]\gg\omega^2(C_{gs}+4C_{gd})\left[\frac{C_{gs}}{(R//r_0)}+4g_mC_{gd}\right]$$

applies in the resulting numerator polynomial and

$$\left[\frac{g_m}{(R//r_0)}\right]^2\gg\left[\frac{C_{gs}}{(R//r_0)}+4g_mC_{gd}\right]^2$$

for the resulting denominator, gives (11), shown at the bottom of the page. Dividing the numerator of (11) by the denominator gives (4).

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$$Z_{\rm IN}(s)\approx\frac{2\left\{\frac{g_m}{(R//r_0)}\left[\frac{1}{(R//r_0)}-g_m\right]+s\left[\frac{g_mC_{gs}}{(R//r_0)}\left(2-\frac{1}{g_m(R//r_0)}\right)+4g_m^2C_{gd}\right]\right\}}{\left(\frac{g_m}{(R//r_0)}\right)^2}. \tag{11}$$

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