A 44–46-GHz 16-Element SiGe BiCMOS High-Linearity Transmit/Receive Phased Array

Choul-Young Kim, *Associate Member, IEEE*, Dong-Woo Kang, *Associate Member, IEEE*, and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—This paper presents a 16-element Q-band transmit/receive phased array with high receive linearity and low power consumption. The design is based on the all-RF architecture with passive phase shifters and a 1:16 Wilkinson network. An input $P_{1\mathrm{dB}}$ from -9 to -10 dBm and a noise figure of 10–11.5 dB at 44–46 GHz is achieved in the receive mode with a power consumption of 0.95 W. In the transmit mode, each channel has an output $P_{1\mathrm{dB}}$ of 3–2 dBm and P_{sat} of 6–4 dBm at 44–46 GHz with a power consumption of 1.16 W. The design results in a low root mean square (rms) gain error due to a high-resolution variable gain amplifier in each channel. Measurements on multiple channels show near-identical gain and phase response in both the transmit and receive mode due to the use of a symmetrical passive combiner. The measured on-chip coupling is <-40 dB and results in insignificant additional rms and phase error.**

***Index Terms*—Millimeter-wave integrated circuits, phase shifters, phased arrays, silicon germanium.**

I. Introduction

SILICON-BASED phased arrays based on the all-RF architecture have been demonstrated in transmit and receive modes for microwave and millimeter-wave applications with 4–32 elements [1]–[8]. The silicon designs allow the integration of many elements on the same chip, together with the power-combining network and all the necessary digital control electronics. This results in a significant advantage over GaAs- or InP-based phased arrays due to the small space available per unit cell in a phased array, especially at millimeter-wave frequencies The silicon designs also result in nearly identical response between the channels due to the high yield and relatively low transistor count (hundreds to thousands of RF transistors) in these chips. At millimeter-wave frequencies, passive power combiners (or dividers) can be used such as Wilkinson couplers, and these occupy a small chip area and have low loss per stage (0.7–0.8 dB).

Silicon millimeter-wave phased array chips have relatively low linearity in the receive mode with a $P_{1\mathrm{dB}}$ from -16 to -25 dBm and a noise figure (NF) of 7–11 dB [1]–[8]. This is acceptable for several consumer applications, but if the phased-array requires a system NF of ≤ 3 dB, then it must be preceded by a 20-dB gain InP low-noise amplifier (LNA), and this reduces its input $P_{1\mathrm{dB}}$ to -37 to -45 dBm, which is not acceptable for many defense and satellite applications. A 20-dB gain is required so as to reduce the noise contribution from the silicon chip. For these applications, it is imperative to build relatively high-linearity receive phased-array chips with a $P_{1\mathrm{dB}}$ of -10 dBm, while maintaining a relatively low NF (10–12 dB) and power consumption. The silicon chip gain in the receive mode can be 0–5 dB per channel since the front-end gain is given primarily by the InP LNA. In the Tx mode, and for high-power phased arrays (25–50 mW per element, 2000–4000 elements), the silicon phased-array chip should have an output power of 0–3 dBm per element so as to be able to drive a millimeter-wave InP medium power amplifier (MPA).

This paper expands the work done in [1] and demonstrates a 44–46-GHz transmit/receive 16-element phased array, as shown in Fig. 1, with high linearity in the receive mode, while consuming only 0.9 W. In the transmit mode, the output power per channel is 0–3 dBm at 44–46 GHz with a power consumption of 1.1 W. The chip architecture is similar to [1], but with improved linearity and power consumption using a careful system-level optimization and full electromagnetic (EM) simulations. The application areas are in Q-band satellite communication systems with a large number of phased-array elements (256–4048). Therefore, the transceiver is not integrated on-chip, and is placed at the sum port of the entire phased array.

II. System-Level Analysis: Transmit and Receive Phased Array

A. Linearity

The key issue in high-linearity phased arrays is the linearity of the phase shifter. This is because silicon millimeter-wave phase shifters are generally lossy (-3 dB for active vector modulators, to -14 dB for passive implementations) and an NF of 13–16 dB [2], [5], [10]. In order to achieve a reasonable NF at the input of the silicon chip, the phase shifter must be preceded by an on-chip silicon LNA with a gain of 15–20 dB and an NF of 4–5 dB. Therefore, a high input $P_{1\mathrm{dB}}$ on the silicon chip translates to a high power at the output of the silicon LNA, and active

Manuscript received July 31, 2011; revised December 01, 2011; accepted December 13, 2011. Date of publication February 06, 2012; date of current version March 02, 2012. This work was supported by the Defense Advanced Research Projects Agency (DARPA) under the Scalable Millimeter-Wave Array Technology (SMART) program, under a sub-contract from Teledyne Scientific.

C.-Y. Kim was with the Electrical and Computer Engineering Department, University of California at San Diego, La Jolla, CA 92093 USA. He is now with the Department of Electronics Engineering, Chungnam National University, Daejeon 305-764 Korea (e-mail: kimchyee@gmail.com).

D.-W. Kang was with the Electrical and Computer Engineering Department, University of California at San Diego, La Jolla, CA 92093 USA. He is now with Samsung Electronics, Suwon 443-742 Korea (e-mail: rfhbsp@gmail.com).

G. M. Rebeiz is with the Electrical and Computer Engineering Department, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: rebeiz@ece.ucsd.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2012.2184130

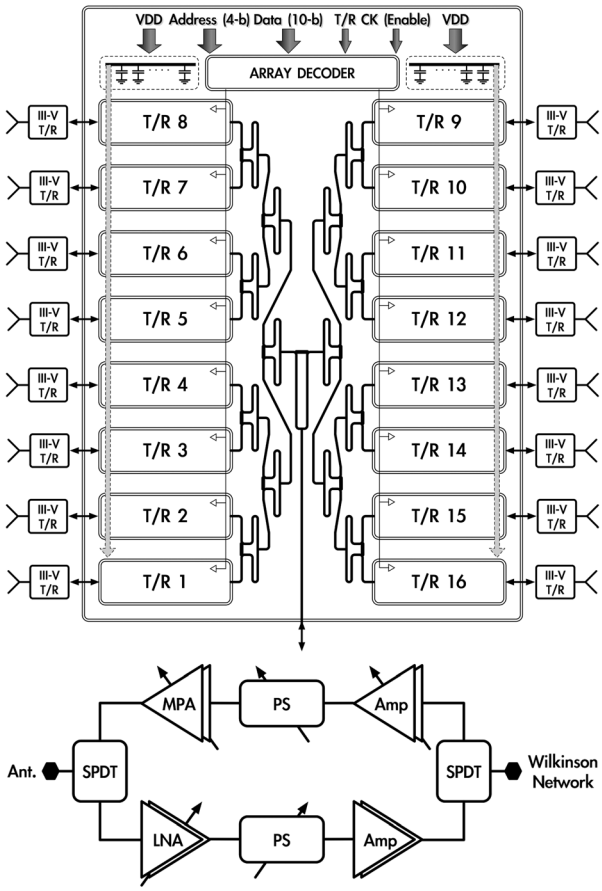
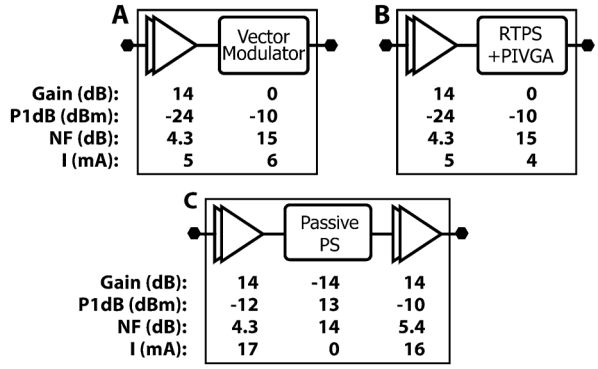


Fig. 1. Block diagram of the 16-element phased array: Silicon chip (*top*) and channel topology (*bottom*).



Topology	IP1dB (dBm)	Gain (dB)	NF (dB)	Current (mA)	Power (mW)
A	-24	14	5.9	11	25
B	-24	14	5.9	9	20
C	**-12**	**14**	**8.1**	**33**	**59**

Fig. 2. Comparison of the different RF phase-shifter topologies.

silicon phase shifters cannot handle a lot of RF power unless a high voltage/current bias is used.

Fig. 2 presents a system analysis based on the three most common phase shifters used to-date, which are: A) vector modulators [2]; B) switched-*LC* networks [10]; and C) reflective-type phase shifters [5], all using the IBM8HP SiGe BiCMOS technology (0.12-μm SiGe transistors with f_T of 200 GHz, 0.12-μm CMOS transistors with f_T of 110 GHz).

The vector modulator phase shifter is based on an in-phase/quadrature (I/Q) network and two variable gain amplifiers, and therefore it can only achieve high linearity with a high bias current. It results in a gain from $\sim$0 to -3 dB, but has a high NF (13–15 dB) and a low $P_{1\mathrm{dB}}$ $(-10$ dBm$)$ for a current consumption of 5 mA. It is a good choice for wideband systems requiring relatively low linearity. Based on simulations, increasing the overall channel linearity to -10 dBm requires that the vector modulator handles at least 3 dBm of power, and this will consume an additional 20 mA of power in the phase shifter itself (the LNA will also require additional current for an output power of $+3$ dBm).

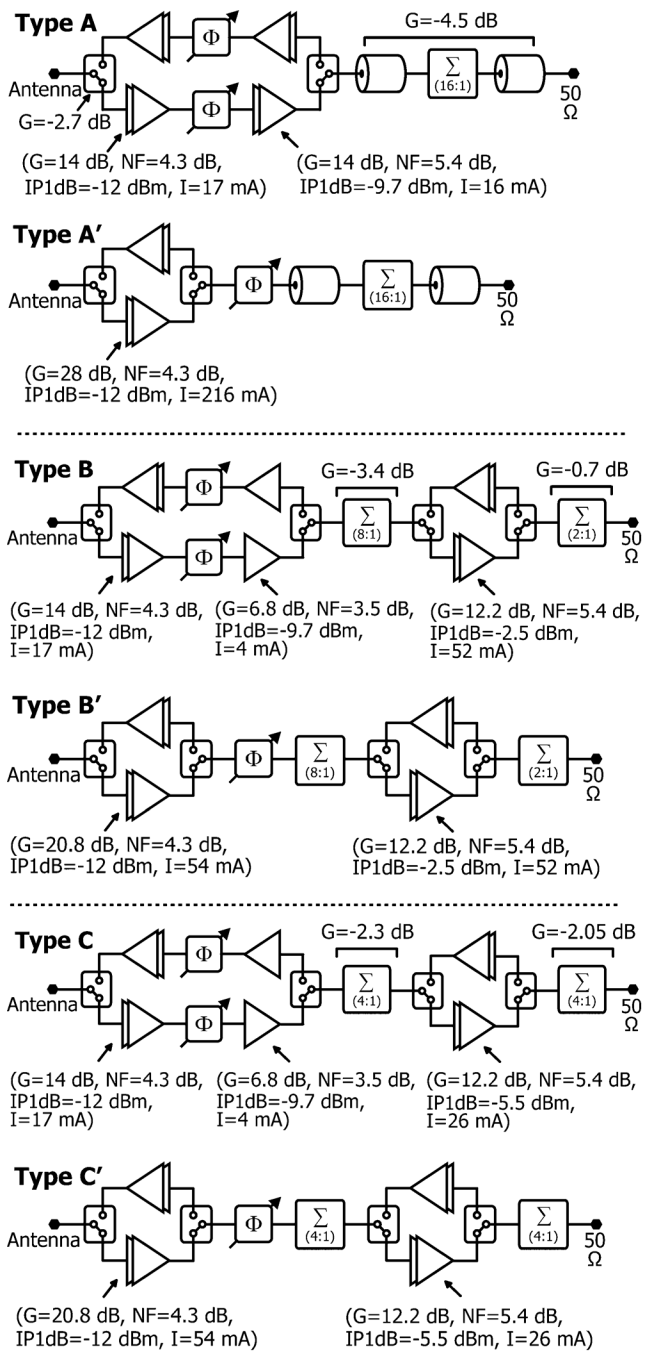
The reflective design is based on the traditional design of a hybrid (90°) coupler and SiGe varactors to obtain a 0°–90° phase shift (two of them are used to achieve from 0° to 180° phase shift) and a differential phase inverting amplifier to achieve a 0°/180° phase selection. This design cannot handle a lot of power since the varactor self-biases at high RF power and changes the insertion phase. The phase inverting amplifier also requires a lot of current to handle a high RF power. This design can also have a gain of $\sim$ 0 dB for a current consumption of 4 mA, but with a high NF (15 dB) and a low $P_{1\mathrm{dB}}$ $(-10$ dBm$)$. It is also a good choice for systems requiring relatively low linearity at low power consumption. Again, increasing the overall channel linearity to -10 dBm requires that the reflective phase shifter handles at least 3 dBm of power and this may not be possible due to the varactors used (the LNA will also require additional current for an output power of $+3$ dBm).

On the other hand, the switched-*LC* phase shifter is based on CMOS switches and has a $P_{1\mathrm{dB}}$ of 11–12 dBm, a third-order intermodulation intercept point (IIP3) of 25–27 dBm (typical of CMOS switches [11]), and permits high linearity at zero power consumption. The phase shifter loss is 14 dB at 45 GHz with an NF of 14 dB. The high power handling of the switched-*LC* phase shifter allows the use of a high-gain high-linearity LNA so as to achieve a high system linearity. The phase shifter must also be followed by another amplifier so as to achieve a channel gain of 14 dB. To our knowledge, this is a competitive topology, which allows for a high-linearity receive phased-array channel and with relatively low power consumption.

B. Optimization of Gain/Phased Shifter Blocks

The amplifier/phase shifter gain blocks are then optimized in order to achieve a 16-element high-linearity phased array with the lowest amount of dc power (Fig. 3). A passive 1:16 Wilkinson combiner/divider is employed since it allows for high-level power combining with no dc power consumption. Two key questions are: Should a single phase shifter be used in the Tx and Rx mode or two different phase shifters, one for Tx and one for Rx? And where should the gain blocks be placed?

The choice of two phase shifters results in the omission of two single-pole double-throw (SPDT) switches and is preferable for all designs because the SPDT switches have a simulated loss of 2.7 dB each (5.4 dB for a pair) and a detrimental effect on the system. Also, amplifiers inside the 1:16 combiner necessitate two SPDT switches (for the Tx and Rx operation) and must have high linearity amplifiers so as to handle the summed RF power



Topology	IP1dB (dBm)	Gain (dB)	NF (dB)	Current (mA)	Power (W)
A	**-9.3**	**4.1**	**10.7**	**528**	**0.95**
A′	-9.3	4.1	7.3	3456	6.2
B	-9.3	4.1	12.8	440	0.79
B′	-9.3	4.1	11.9	968	1.74
C	-9.3	4.1	12.2	440	0.79
C′	-9.3	4.1	11.1	968	1.74

Fig. 3. Comparison of different channel and combiner architectures in the 16-element phased array. The phase shifter loss is 14 dB.

from the different phased-array channels or to handle the drive power for many channels in case of a Tx signal, and are therefore not preferable. A 1:16 Wilkinson combiner has a simulated loss of only 4.5 dB at 44–46 GHz and this can be mitigated with added amplifier gain in each phased-array element (Rx case), or using 5 dB more input power (Tx case).

It is clear from Fig. 3 that topologies A–C all result in competitive designs in terms of power consumption, but topology A is chosen since it has the lowest NF and a passive combiner.

C. Single Ended Versus Differential Circuits

Both single-ended and differential phased arrays have been demonstrated at millimeter-wave frequencies [1]–[8]. The single-ended design results in slightly lower NF, reduced power consumption and less wafer area, while the differential design is not affected by ground and supply inductance and is more robust when packaged using bond-wires. In this study, the 16-element phased array will be packaged using polyimide redistribution layers spun on top of the silicon chip [9]. This results in a very low ground inductance, and therefore, a single-ended design is chosen for this study.

D. System-Level Linearity

A 16-element silicon phased array with an input $P_{1\mathrm{dB}}$ of -10 dB and a 0-dB gain results in an output $P_{1\mathrm{dB}}$ of $+2$ dBm with no combining loss and is a high drive for a receive mixer. For the case of a 1024-element array (adding 64 of these chips together), the output $P_{1\mathrm{dB}}$ from the phased array could be as high as $+20$ dBm with no combining losses. One line of thought is that the linearity will be limited by the receive mixer, and therefore, the effective input $P_{1\mathrm{dB}}$ is much lower than -10 dBm per channel. This is incorrect since, in a real system, the interferers are not spatially located in the main beam direction, but in a wide range of angles, and the phased-array pattern results in coherent cancellation of the interferers at the sum point (from -17 to -26 dB, depending on the sidelobe levels). A standard mixer can also be used in the receiver.

There are therefore two definitions of linearity in large phased-arrays: *main beam linearity*, which is limited by the receiver and can be quite low due to the array factor gain and finite mixer linearity, and *wide-angle (interferer) linearity*, which is generally limited by the phased-array channel linearity. The wide-angle linearity (i.e., channel linearity) is the important metric in large phased-array systems since the required signal is very low especially in satellite communications.

III. Design

A. Receive Chain

The IBM 8HP has a versatile RF metal stack that allows for low-loss coplanar waveguide (CPW) lines ($Zo = 50\ \Omega$, gap/signal/gap of 11/12/11 μm, $\varepsilon_{\mathrm{eff}} = 3.9$, $\alpha = -0.45$ dB/mm at 44 GHz), variable ground plane heights (MQ or M1 are used), high-Q (>100) metal–insulator–metal (MIM) capacitors and low-Q (~ 5) nMOS capacitors (Fig. 4).

The design is based on topology A in Fig. 3, and a detail of the power levels for high linearity are shown in Fig. 5(a). In both the transmit and receive paths, an interstage and system-level impedance of 50 Ω is used. This is due to two reasons, which are: 1) the relatively high power levels in the phased-

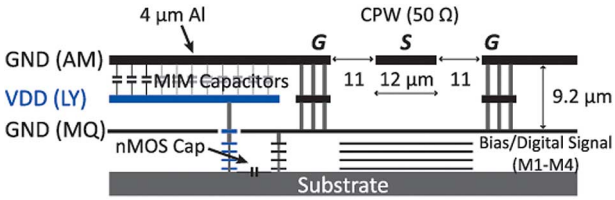


Fig. 4. IBM8HP metal stack-up.

array channel necessitate large transistors and high bias currents, and this is more congruent with a low impedance system and 2) the Wilkinson coupling network requires a 70-Ω quarter-wave line (in a 50-Ω system), which is doable in the IBM8HP technology.

A 0.12-μm CMOS SPDT series-shunt switch is first used in the Tx/Rx phased array [see Fig. 5(a)] [1]. The switch shows a simulated insertion loss of 2.7 dB, an isolation of 35 dB, and an input $P_{1\mathrm{dB}}$ of 11 dBm. The switches use standard CMOS transistors and the CMOS device size is optimized using Cadence to result in the lowest insertion loss and high isolation with reasonable inductor values.

The SiGe LNA is based on a two-stage cascode design with emitter inductor degeneration for low noise [see Fig. 5(b)]. A large bias current is used to result in an input $P_{1\mathrm{dB}}$ of -12 dBm and an output $P_{1\mathrm{dB}}$ of $+2$ dBm (Gain $=$ 15 dB). The biasing conditions are at the minimum NF point (0.4 mA/μm) in order to result in the lowest overall NF. The second stage also acts as a variable gain amplifier (VGA) using current steering with a 3-bit control. However, a gain control of only 6 dB is used so as not to affect the LNA linearity ($\mathrm{IP}_{1\mathrm{dB}} = -14$ dBm at Gain $=$ 9 dB). The inductive loads have a shunt resistor (70–200 Ω) in order to widen the frequency response. All biasing is done using standard current mirrors attached to be transistor base nodes using 3–5-kΩ resistors. The simulated gain and NF are 14.5 and 4.3 dB at 44 GHz, respectively, with a 3-dB bandwidth of 15 GHz at the maximum gain setting. The NF increases to 5.3 and 6.3 dB when the gain is reduced to 11.5 and 8.5 dB, respectively, at 44 GHz. The input and output impedance match are <-10 dB at 36–100 GHz. The cascode amplifier is stable with $S_{12} < -50$ dB and $k > 64$ at 42–50 GHz and consumes 16 mA from a 1.8-V supply.

In this design and for modeling, the entire stack was placed in Sonnet [12] and accurate EM analysis was done on the SPDT, amplifiers, and phase-shifter blocks. Fig. 6 presents the Sonnet model used for the SPDT and LNA with input and output 50-Ω ports in the AM/MQ layers. The transistors are removed from the simulation with the base, collector, and emitter nodes treated as internal Sonnet ports, and the entire EM model is then ported into Cadence and used with the IBM transistor models. The IBM MIM capacitors (46–92 fF) are also modeled and the 46 fF is composed of two 92 fF in series. The 150–230-pH inductors result in a Q of 16–20 at 44 GHz, and the EM coupling between the inductors and all structures are automatically taken into account. The full EM method is time consuming in the design stage (2 h for LNA simulations from 1 to 100 GHz using a modern desktop), but as seen in Section IV, it results in good agreement between simulations and measurements.

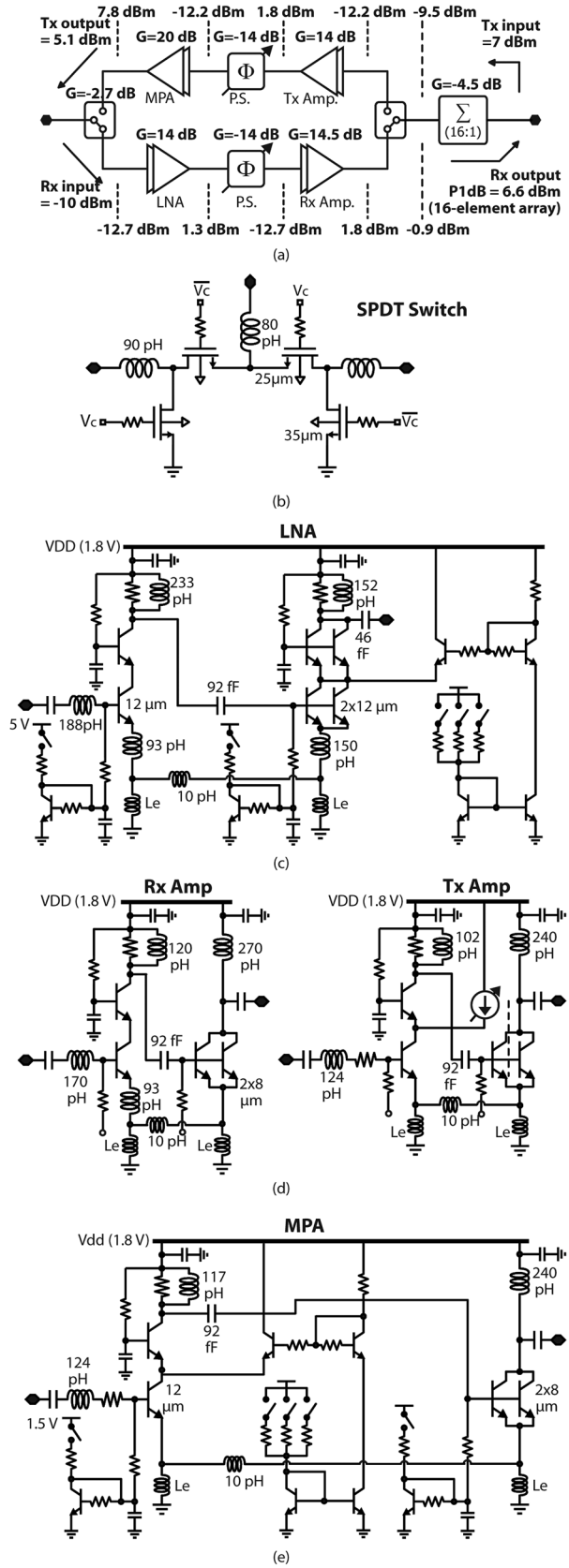


Fig. 5. (a) System-level block diagram with nominal power levels, and schematics of the: (b) SPDT, (c) LNA, (d) Rx Amp, Tx Amp, and (e) MPA, designed for 44–46-GHz operation.

The phase shifter is based on switched LC-networks and is a scaled version of an earlier design [1] (Fig. 7). The transistor

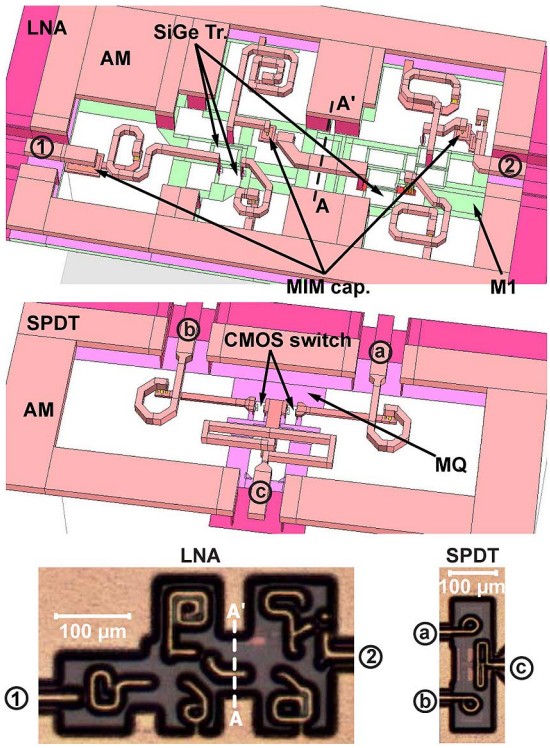
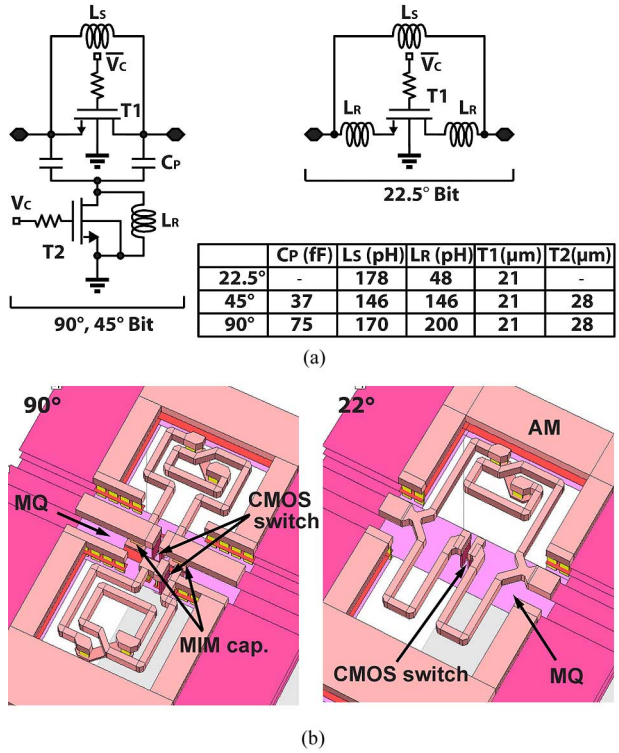


Fig. 6. EM simulation environment and microphotographs of the LNA and SPDT switch.



	CP (fF)	LS (pH)	LR (pH)	T1(μm)	T2(μm)
22.5°	-	178	48	21	-
45°	37	146	146	21	28
90°	75	170	200	21	28

(a)

(b)

Fig. 7. (a) Schematics and (b) EM simulation environment of the switched *LC* phase shifters.

sizes and LC values are chosen to match each cell to 50 Ω in the bypass and phase-delay state. Again, EM simulations are used to ensure that any coupling between Ls and Lr is taken into account (mutual coupling, $k < 0.05$ at 44–46 GHz) and the MIM capacitors are modeled and connected in series for smaller value with EM simulation. Standard IBM models are used for the CMOS transistors. As seen in Fig. 8, the 22° and 45° phase shifter cells have an amplitude variation of 0.5–1 dB at 44–46 GHz between the bypass and phase-delay state.

The 4-bit phase shifter is a concatenation of the different bits, as shown in Fig. 9, and the phase shifter bit placement was chosen using Cadence to achieve the lowest gain variation versus phase state and an rms phase error $<10°$ at 44–46 GHz. The $(0, 0, 0, 0)$ setting with the T1 transistors turned-on results in the 0° phase state and shows the highest loss (14.4 dB) since the CMOS transistors are in series with the RF transmission line, while the lowest loss (12.6 dB) occurs in the $-335°$ phase state when the T2 transistors are turned-on $(1, 1, 1, 1$ state). The simulated phase-shifter gain variation is $+/-0.9$ dB at 44 GHz over the 16 states, and is lower than what was achieved using a millimeter-wave vector modulator [2] (Fig. 9). The VGA can be used to equalize the gain versus phase state if needed. The simulated phase shifter $P_{1\mathrm{dB}}$ and IIP3 are 10 and 26 dBm, respectively, at 44–46 GHz, and therefore do not limit the system linearity. The CMOS transistors are biased using 20-kΩ resistors at the gate nodes, which sets the switching time to ~ 0.5 ns [11], [13].

An amplifier (Rx Amp) with 14.5-dB gain is placed after the phase shifter to compensate for the SPDT (2.7 dB) and the phase-shifter loss. It also provides enough gain to overcome the 1:16 Wilkinson combiner network loss (4.5 dB at 44–46 GHz). This amplifier must also have a high linearity, and is designed

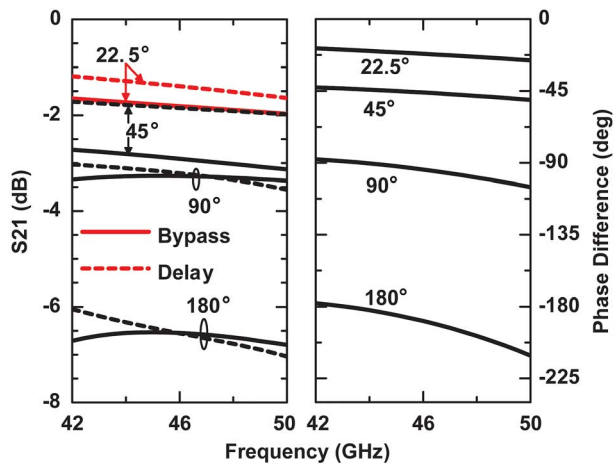


Fig. 8. Simulated insertion loss and phase of the switched *LC* phase shifters versus frequency.

with an output $P_{1\mathrm{dB}}$ of +4.3 dBm (17 mA, 1.8 V). The design is similar to the LNA, but without any gain control.

The total gain of the receive chain is simulated to be 10–9 dB at 44–46 GHz (not including the 4.5-dB Wilkinson loss), an NF of 9.5–10.5 dB, a $P_{1\mathrm{dB}}$ of -10 dBm, respectively, and with a power consumption of 59 mW per channel (33 mA, 1.8 V).

B. Transmit Chain

The transmit chain employs an amplifier (Tx Amp), a phase shifter, and an MPA, together with two SPDT switches. The input power to the 16-element array is +7 dBm at 44 GHz, resulting in a power of -12.2 dBm at the input of the Tx amplifier (12-dB Wilkinson division, 4.5-dB Wilkinson loss, 2.7-dB SPDT loss). The Tx amplifier is a two-stage cascode with a gain

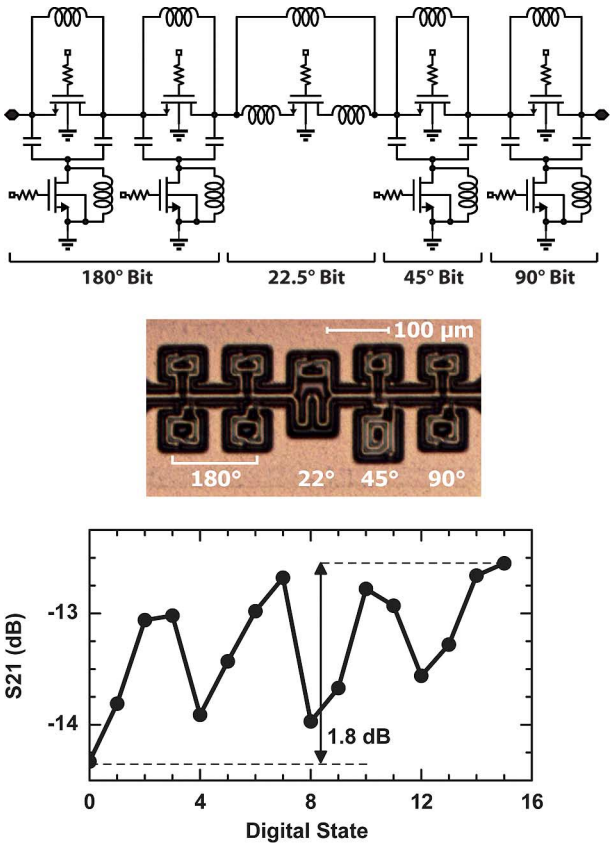


Fig. 9. Schematic, microphotograph, and simulated gain of the 4-bit phase shifter at 44 GHz.

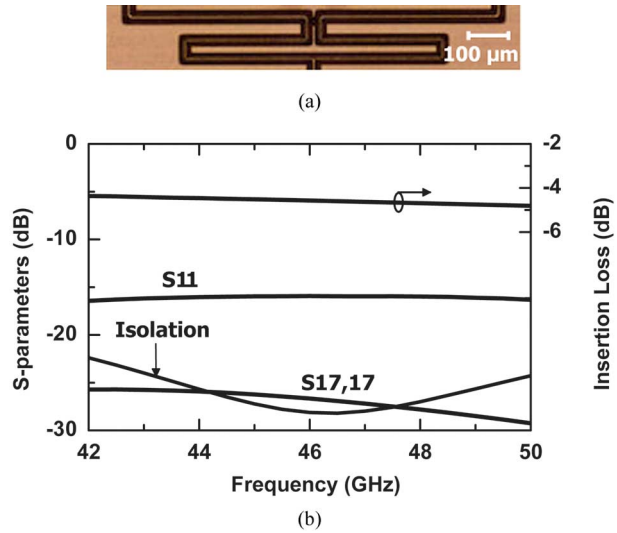


Fig. 10. (a) Photograph of a single Wilkinson combiner with connecting 50-Ω transmission line. (b) Simulated S-parameters of the 1:16 Wilkinson combiner.

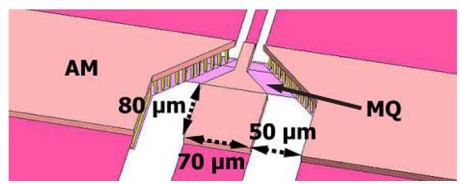


Fig. 11. EM simulation environment for the GSG transition. Note the ground plane MQ is placed 28 μm from the edge of the 80 × 70 μm pad.

of 14 dB and an output power of +1.8 dBm and does not use any emitter inductors (Fig. 5). A 5-dB gain control is built into the Tx amplifier using 3-bit current steering. After passing by the phase shifter with 12.6–14.4-dB loss (same design as above), the signal is then amplified using a two-stage cascode amplifier (MPA) with a gain of 20 dB and an output $P_{1\mathrm{dB}}$ of +7.4 dBm at 44 GHz. Again, no inductors are used in the emitters for increased gain, and a gain control of 5 dB is also included in the MPA (Fig. 5). The MPA is biased using current mirrors in a standard class A configuration with a simulated power-added efficiency (PAE) of 10% at 44 GHz. It is stable with $S_{12} < -60$ dB, $k > 50$ at 42–50 GHz, and consumes 24 mA from a 1.8-V supply. The Tx signal passes by the SPDT switch and the output power is ∼ 4 dBm per channel.

EM analysis is done on the transmit chain amplifiers (not shown for brevity) and the transistor sizes and inductor values are optimized for best performance using several iterations between Sonnet and Cadence. The simulated transmit channel gain is ∼15 dB at 44–46 GHz (not including the 4.5-dB Wilkinson loss), with an output $P_{1\mathrm{dB}}$ of +4.7 dBm, and a power consumption of 70 mW per channel (39 mA, 1.8 V).

C. EM Simulation of the Phased-Array Transmit-Receive Chain

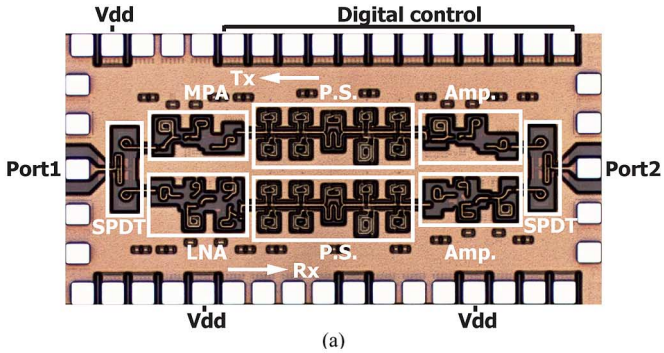
Due to the size of the circuits and the seven metal layers, it is virtually impossible to electromagnetically model the entire transmit or receive chain all together. Sonnet simulations done up to 100 GHz on an equivalent ground-plane section for a single-channel indicate the presence of a finite, but small, inductance due to the ground current return (using Y-parameters), and an approximate value of $Le \sim 7$ pH is taken (4 pH for the amplifiers close the ground–signal–ground (GSG) pad, and 10 pH for the amplifiers far from the GSG pad). This introduces an additional series impedance ($j2\ \Omega$ at 44 GHz), which is present at the emitter grounds in Fig. 5. A $Le = 7+/-3$ pH inductance is hard to model accurately, and therefore, the Sonnet simulation is taken as an estimate.

D. 1:16 Wilkinson Network

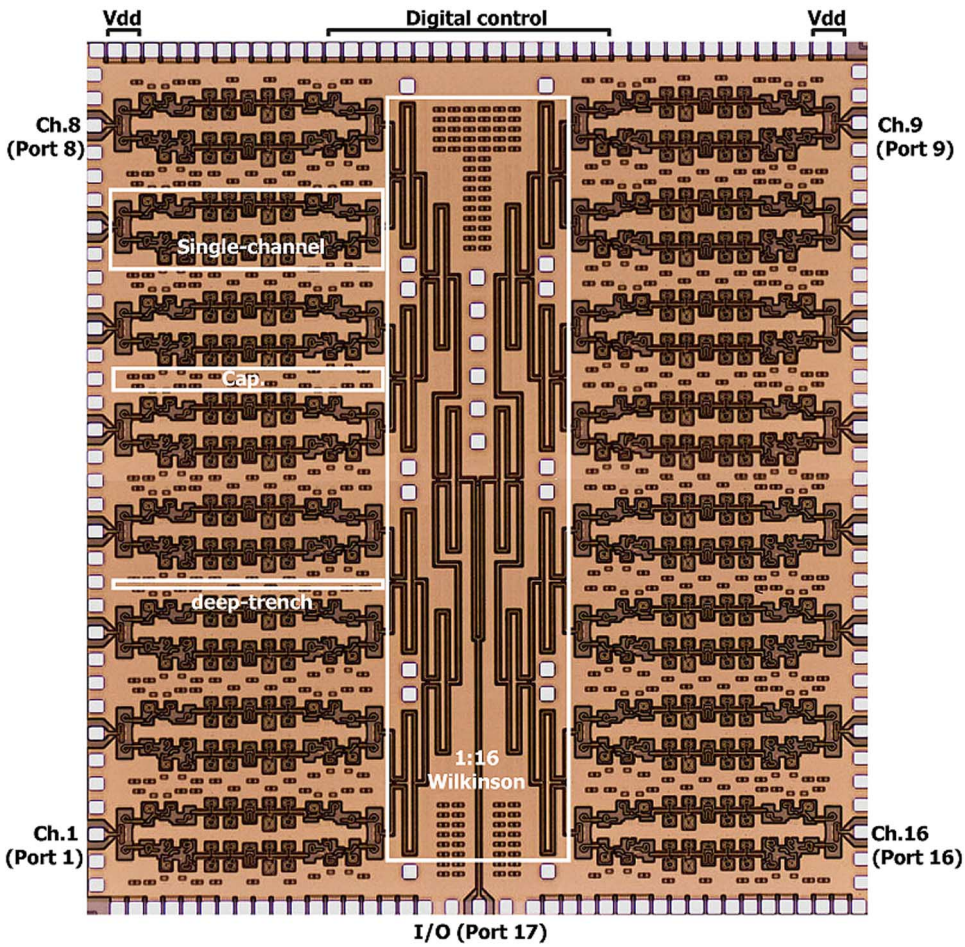
A 1:16 Wilkinson network is used for power combining and distribution [14]. The Wilkinson couplers are built using 70-Ω $\lambda/4$ transmission lines (gap/signal/gap of 11/6/11 μm) with a loss of 0.55 dB/mm at 44 GHz, and the simulated single-stage Wilkinson loss is 0.7 dB at 44 GHz [see Fig. 10(a)]. The connecting 50-Ω transmission lines have a simulated loss of 0.45 dB/mm at 44 GHz. The entire 1:16 Wilkinson network is simulated in Sonnet and results in a total loss of 4.5 dB at 44 GHz (4 × 0.7 dB +1.7 dB connecting lines), a wideband impedance match, and an isolation > 22 dB at 42–50 GHz [see Fig. 10(b)]. The 1:16 Wilkinson network has no effect on the phased-array performance, except for the additional loss.

E. GSG Pad Design

Fig. 11 presents the optimized 150-μm-pitch GSG pad layout for the phased-array chip. The GSG transition is simulated using Sonnet and the taper and ground plane (MQ) location is chosen to result in a wideband impedance match at 40–50 GHz. The



(a)



(b)

Fig. 12. Microphotographs of the: (a) single-element (1.8×0.9 mm^2) and (b) 16-element phased-array transmit/receive chip (4.9×5.1 mm^2).

transition results in $S_{21} = -0.1$ dB and $S_{11} < -28$ dB at 44–46 GHz.

F. Digital Control Section

The control logic in the array decoder is designed with 0.12-μm CMOS and is controlled using a 1.5-V supply. The output from a 4:16 address decoder loads a 10-bit parallel data stream -4 bits for phase, 6 bits for gain (three per amplifier block) into a register when the enable signal is set to high. There are two registers per channel selected by the transmit/receive control voltage: one for transmit and one for receive, thus allowing the array to transmit in one direction and receive in another direction if needed. The 10-bit registers (32 of them) are composed of level-triggered D-flip-flops with a delay of 20 ns. The transmit/receive control voltage also selects the SPDT polarity and disconnects the biasing current mirrors in either the Tx (when Rx is selected) or Rx (when transmit is selected).

Metals M2 and M3 are used for the digital signal distribution with M1 as ground plane so as not to couple the digital transients to the silicon wafer. The longest transmission line length is 5 mm and the estimated *RC* delay of the interconnection lines is < 110 ps. The main delay is set by the D-flip-flops and is 20 ns with a maximum control frequency of 50 MHz.

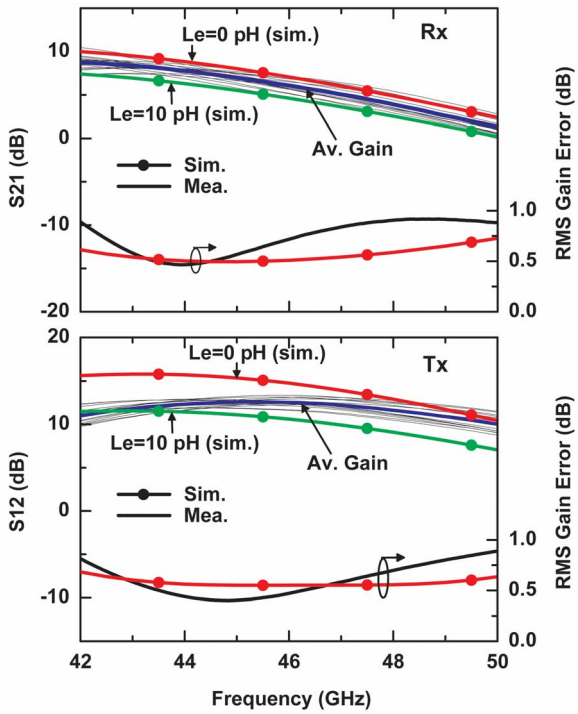


Fig. 13. Measured and simulated receive and transmit gain for the single element chip for 16 different phase states. The solid blue line (in online version) is the average gain over 16 phase states.

G. Other

Single-ended designs require excellent decoupling of the bias lines. Therefore, each amplifier block uses 3 pF of bias decoupling capacitors ($X = -j1.2\ \Omega$ at 44 GHz) composed of an array of 100–200-fF MIM capacitors with a series-resonant frequency >50 GHz, and n-CMOS capacitors with low-Q ($Q{\sim}5$) for added stability. The total de-coupling capacitor value between V_{DD} and ground is 40 pF for each transmit/receive channel. Additional bias supply de-coupling capacitors are placed all around the Wilkinson couplers and close to the V_{DD} pins.

Via walls are used between the channels from the top AM metal to the substrate to reduce any coupling between the channels. The IBM 8HP process also offers 5–10-μm-deep trenches in the silicon substrate, and these are used between the different channels for breaking the RF currents in the substrate and for added isolation. To our knowledge, careful studies have not yet been done to establish if the via-walls or the deep trench help the isolation between the channels, but they are "free," do not take additional space, and are used throughout the chip. All low-current bias and digital control lines are routed under the MQ ground plane using M1–M4 and have no effect on the RF performance.

The NF and output power are degraded by the SPDT loss of 2.7 dB. In hindsight, and due to the relatively narrowband design of 42–50 GHz, a series-resonant switch design could be used with a loss of 1.5 dB [11]. A power amplifier (PA)-LNA circuit with no switches may also be an excellent choice for this application [15]. Both of these could result in better gain and NF than the conservative series-shunt SPDT design.

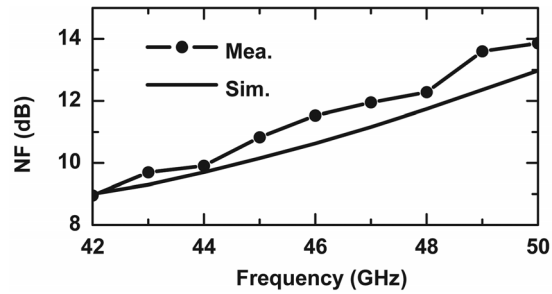


Fig. 14. Measured and simulated NF for the single-element chip.

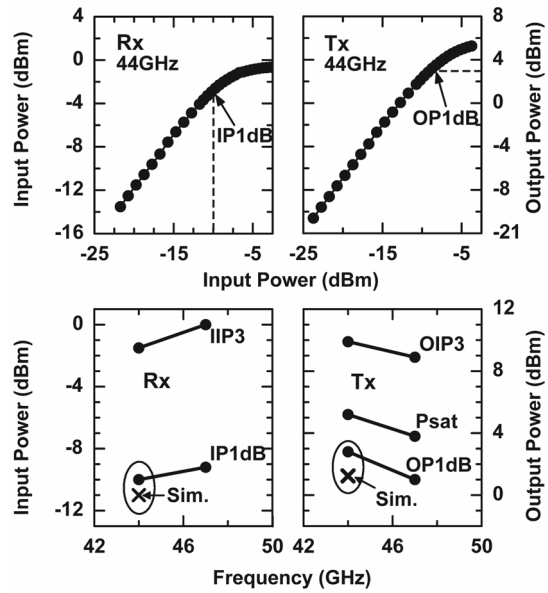


Fig. 15. Measured and simulated input $P_{1\mathrm{dB}}$ and IP3 (Rx mode) and $\mathrm{OP}_{1\mathrm{dB}}$, P_{sat} and OIP3 (transmit mode) for the single-element chip. These values are within $+/-0.5$ dB for all 16 phase states.

H. Final Chips

Both a single- and 16-element phased array were fabricated (Fig. 12). The single-element chip is 1.8×0.9 mm^2. The 16-element array is 4.9×5.1 mm^2 and consumes 640 mA (Tx) and 530 mA (Rx) from a $V_{DD} = 1.8$ V supply, and virtually no current from the 1.5-V CMOS supply (in hindsight, 1.2 V would have been better for the long-term reliability in 0.12-μm CMOS, but the chip operated well at 1.5 V). Several V_{DD} supply voltage nodes are used to result in a low voltage drop across the chip and to allow for a multitude of off-chip capacitors for added stability at RF/microwave frequencies. The current references can also be individually controlled using an external bias voltage, but they are generally tied to a 1.5-V analog supply. The 16-element chip has 656 inductors, 608 SiGe transistors, and 4632 CMOS transistors. There is no electrostatic discharge (ESD) protection on the RF pads.

IV. Measurements

A. Single-Element Phased-Array Chip

The single-channel transmit/receive chip was measured on-chip using a vector signal network analyzer (Agilent, PNA-E8364B) after a standard short-open-load-thru (SOLT)

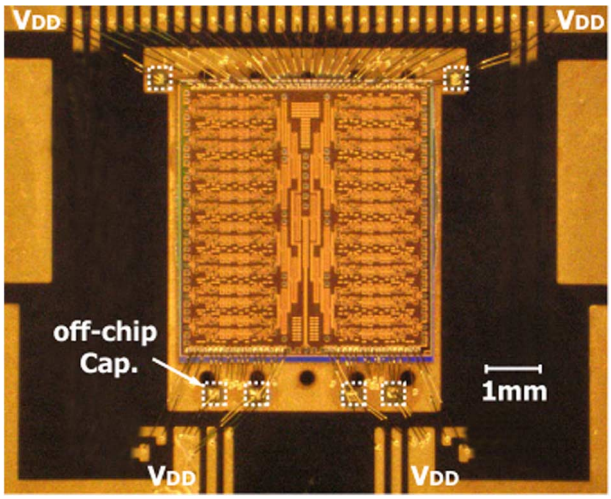


Fig. 16. Photograph of the 16-element phased array mounted on a Teflon board with bias de-coupling capacitors. The chip is still probed using 150-μm-pitch GSG probes. Inputs are East and West, Output is center South, and Bias is North and South.

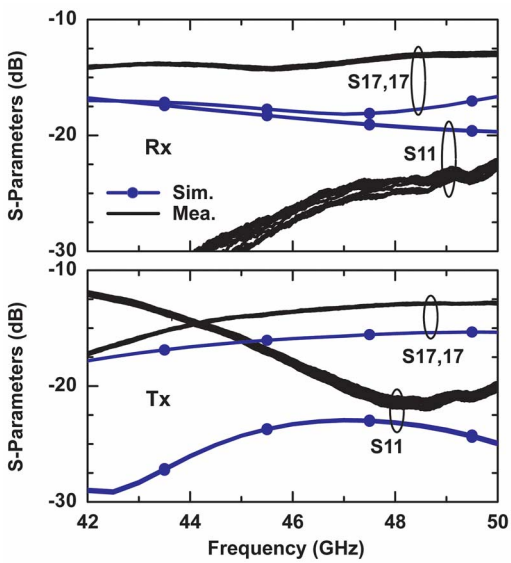


Fig. 17. Measured and simulated input and output reflection coefficients in the receive and transmit modes for 16 different phase states.

calibration to the GSG probe tips. The measurements are done without any trimming. The chip consumes 36 mA (Rx) and 42 mA (Tx) from a 1.8-V supply, which is similar to simulations. The measured Tx and Rx gain agrees well with simulations and are bounded by $Le = 0$ pH and $Le = 10$ pH (added inductance on the emitter nodes) (Fig. 13). The transmit chain is affected more than the receive chain by the Le value since emitter degeneration was not used in the MPA and the Tx Amp. The measured average Tx and Rx gains over the 16 phase states are 11.2–11.4 and 8.0–6.5 dB at 44–46 GHz, respectively, both with an root mean square (rms) gain error of < 0.7 dB. The measured reverse isolation, S_{12}, is < -50 dB for both Tx and Rx modes and is not shown. Phase measurements will be presented in Section V.

In the receive mode, the measured NF is 10–11.5 dB at 44–46 GHz (Fig. 14). The measured input $P_{1\mathrm{dB}}$ and third-order

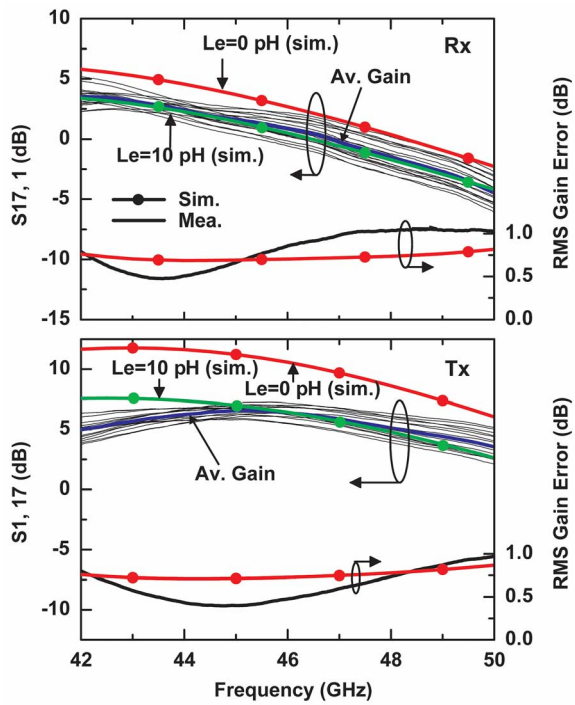


Fig. 18. Measured and simulated receive and transmit gain for a single channel in the 16-element array for 16 different phase states. The solid blue line (in online version) is the average gain over 16 phase states.

intercept point (IP3) are from -10 to -9 dBm and from -1.5 to 0 dBm at 44–46 GHz, respectively, which is the highest achieved in a receive millimeter-wave phased array (Fig. 15). In the transmit mode, the measured output $P_{1\mathrm{dB}}$ and P_{sat} and output third-order intercept point (OIP3) are 3–1.5, 5.5–4.5, 10–9 dBm at 44–46 GHz, respectively (Fig. 15). These values were maintained across all phase states showing that the phase shifter does not limit the linearity or output power of the phased-array channel. Additional measurements that apply to both the single- and 16-element phased array are presented in Section V.

B. 16-Element Phased-Array Chip

The 16-element array was first assembled on a Teflon board with off-chip bias de-coupling capacitors (110 pF each) placed very close to the chip on the 1.8-V V_{DD} and 1.5-V reference current pads (Fig. 16). The supply pins, located at the four chip corners, are all connected to V_{DD}, which results in an insignificant voltage drop to the center channels. Additional 10–100-nF capacitors are also placed far away from the chip, together with commercial ESD protection diodes for the digital control lines. The chip consumes 530 mA (Rx) and 680 mA (Tx) from the 1.8-V supply, which is close to simulations.

The phased-array chip is measured using GSG probes, and the S-parameters are obtained after a standard SOLT probe-tip calibration. A single channel is measured at a time with all other channels left open circuited. This results in 12 dB of additional loss in the Wilkinson combiner since the isolation resistors in the Wilkinson stages absorb 3 dB of the power per stage. Therefore, 12 dB are numerically added to the measured gain for accurate comparison to simulations.

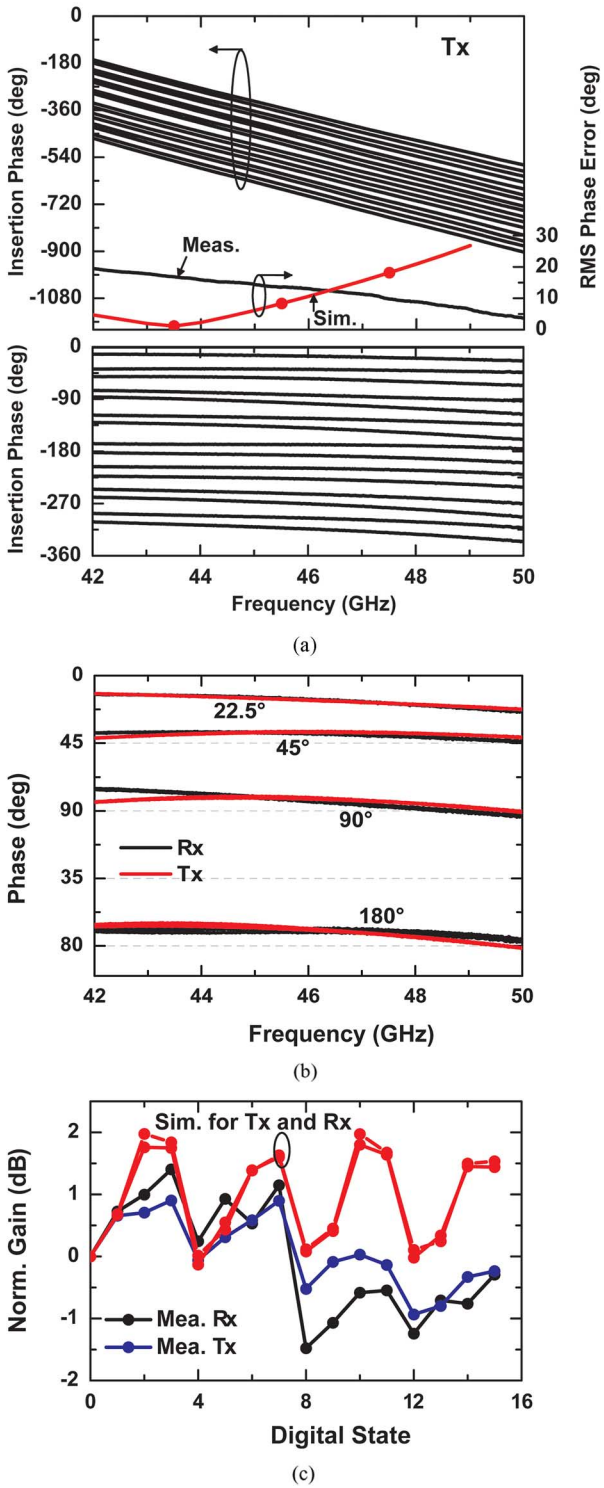


Fig. 19. (a) Measured insertion phase for a single channel in the 16-element array: shown are linear phase response, and phase difference with 0° state as a reference. (b) Measured phase for four different channels in the transmit and receive modes. (c) Measured and simulated normalized phase shifter gain in the transmit and receive modes at 46 GHz.

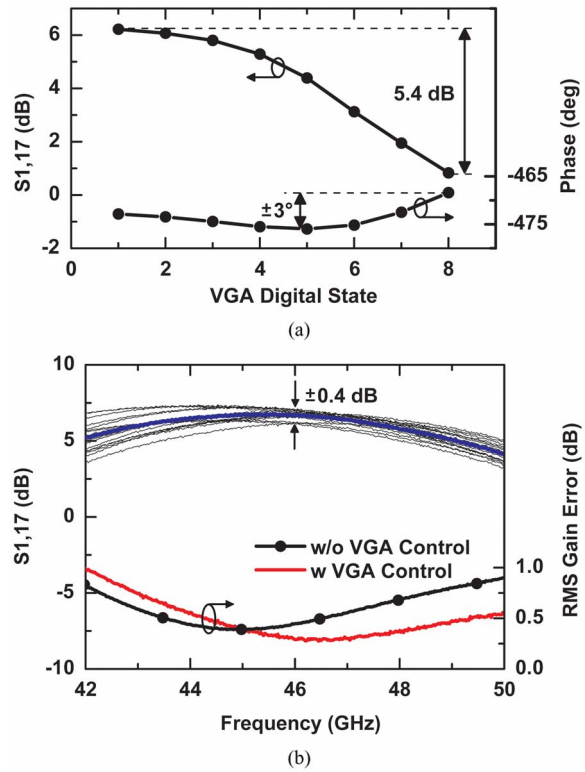


Fig. 20. (a) Measured VGA gain control and insertion phase at 46 GHz. (b) Measured channel gain versus 16 phase states with VGA control. The solid blue line (in online version) is the average gain over 16 phase states.

Fig. 17 presents the measured reflection coefficients in the Tx and Rx modes and with good agreement with simulations at the common port (Port 17). The channel port shows a measured $S_{11}<-12$ dB in both the Tx and Rx modes. The gain of a single channel in the 16-element array is shown in Fig. 18, and it is 5.2–5.3 dB lower than an equivalent channel on the single-element phased-array chip in both the Tx and Rx modes, which is due to the ohmic loss of the 1:16 Wilkinson network (simulation is 4.5 dB at 44 GHz, measurement is 5.2 dB). The measured average Tx and Rx gains over 16 phase states are ~5.8 and 2.8–1.3 dB at 44–46 GHz, respectively. The measured rms gain error in the Tx path is < 0.5 dB at 44–46 GHz.

The measured phase in the Tx mode is shown in Fig. 19 and the lowest rms phase error shifted from the design frequency of 44–50 GHz. We believe that this is due to the CMOS model, which is not accurate enough for high-Q switched resonant-LC circuits. The CMOS switch in the LC phase shifter is either turned off, resulting in a high-Q LC-network with no resistors, or turned on with a low Ron and also resulting in another high-Q LC network. The Tx and Rx phase shifters result in virtually identical performance over all states, as shown in Fig. 19. In this case, four channels are shown each for Tx and Rx settings of 22°, 45°, 90°, and 180° states. The four channels have essentially the same phase response since they all pass by a symmetrical 1:16 Wilkinson network. The measured gain variation due to the phase shifter is 2.7–3.5 dB at 46 GHz (simulation is 1.8–2.0 dB) [see Fig. 19(c)]. The comparison is done at 46 GHz since the measured optimal phase shifter response shifted to 48–50 GHz.

The 16-element phased array results in a large output $P_{1\mathrm{dB}}$ in the receive mode. For an input of -10 dBm and a small-signal gain of 2.8 dB at 44 GHz, the output power at the sum port for a single channel is -7.2 dBm at port 17, and is $+4.8$ dBm when all 16 channels are adding in phase. Therefore, it is essential that

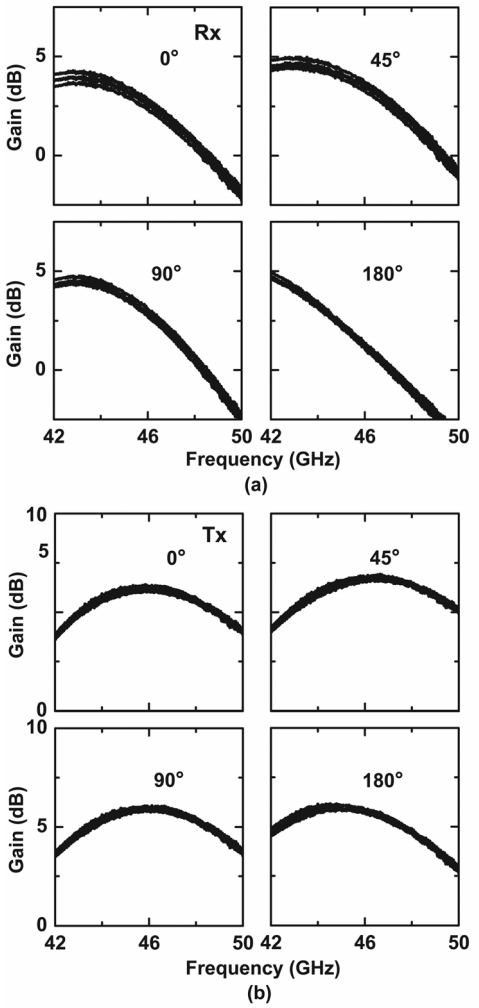


Fig. 21. Measured gain in the: (a) receive and (b) transmit modes for four different channels. Near identical results are achieved due to the symmetrical 1:16 Wilkinson combiner.

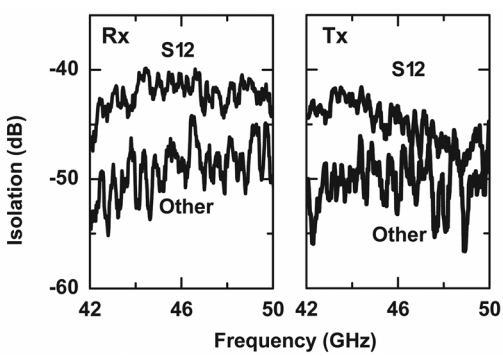


Fig. 22. Measured isolation between different channels in the receive and transmit modes for the 16-element array. Only the neighboring channel has a measurable value.

a passive Wilkinson network is used as the summing network for low power operation.

The VGAs can be controlled over a 5.4-dB range with only $+/-3^{\circ}$ phase variation, which is necessary for obtaining a low rms gain error without introducing any additional phase error [see Fig. 20(a)]. Fig. 20(b) presents the results of VGA employed in the Tx path to reduce the rms gain error from 0.7 dB

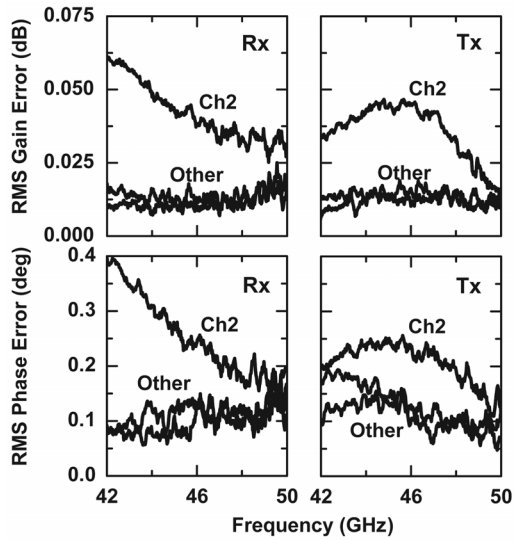


Fig. 23. Measured rms gain and phase error present in channel 1 when the phase of channel 2 (and other channels) is changed from 0° to −335°. The effect of channel 2 is negligible.

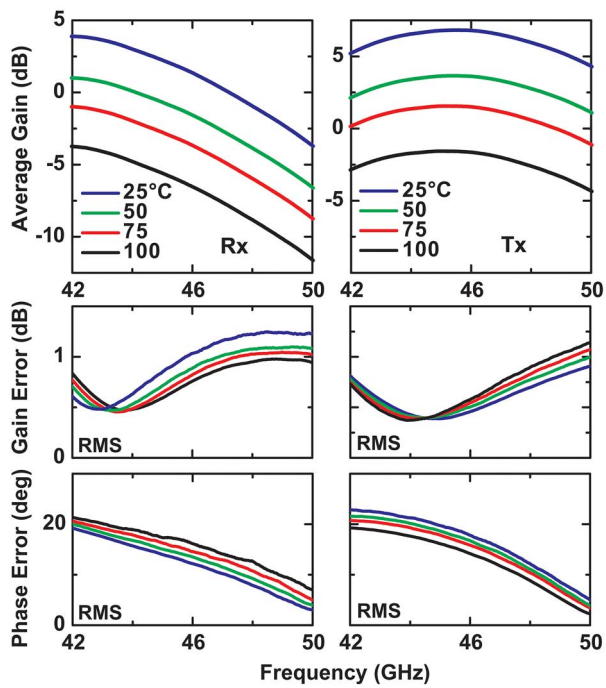


Fig. 24. Measured average gain and rms errors versus temperature for a single channel in the 16-element array. The average gain is obtained by averaging the gain over the 16 phase states.

to $<$ 0.3 dB at 45–46 GHz. This is important for low-sidelobe phased arrays.

Fig. 21 presents the Tx and Rx gain versus frequency for four different channels in the array at various phase settings, and with near identical response. We have also measured the entire array and found similar results. In general, the error is limited by drift and calibration and not by the silicon chip, and shows that silicon-based phased arrays require minimal calibration on a channel-to-channel basis.

Isolation measurements were done in two different ways; First, S_{12} and S_{1n} (n is the channel number, n = 2–16) were measured in the Tx and Rx modes with all other channels left

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH SILICON-BASED PHASED ARRAYS

	This work	This work (Tx only)[a]	This work (Rx only)[a]	[1]	[2]	[3]	[4]	[5]	[6]	[7]
f_0 [GHz]	44 – 46	44 – 46	44 – 46	36	42	60	60	60	60	60
Technology	120 nm BiCMOS	120 nm BiCMOS	120 nm BiCMOS	120 nm BiCMOS	180 nm BiCMOS	90 nm CMOS	90 nm CMOS	120 nm BiCMOS	120 nm BiCMOS	65 nm CMOS
f_T (GHz)	200	200	200	200	150	130	130	200	200	170
Phase Shifter Topology	Switched LC	Switched LC	Switched LC	Switched LC	Vector Mod.	Vector Mod.	Switched LC	Reflect.	Reflect.	Vector Mod.
#of Channels	16	16	16	4	16	1	32	16	16	2
Function	T/R	Tx	Rx	T/R	Tx	Rx	T/R	Tx	Rx	Rx
Phase bits	4	4	4	5	4	4	2	6	5	4
Gain (dB)	Tx 5.7 – 5.8 Rx 2.8 –1.3	11.2	8.2	Rx -2.5 Tx 0	12.5	12.5	12.5	22[b]	72[c]	12
NF[d] (dB)	10 -11.5	-	7.3 – 8.8	9	-	6.5	11	-	7.4	7.2
Rx IP_{1dB}, IIP3 (dBm)	-10 – -9, -1.5 – 0	-	-12.7 – 11.7 -4.2 – -2.7	-16 -5.9		-13.3, -	-17, -	-	-32.6, -23	-16, -
Tx OP_{1dB}, Psat (dBm)	3 - 1.5, 5.5 - 4.5	5.7 – 4.2, 6 - 7	-	4.7 7	-5 -2.5	-	Psat: -7	OP_{1dB}: 9	-	-
Power(W)	Tx 1.16 Rx 0.95	1.16	0.95	Tx 0.17 Rx 0.14	3.6	0.06	Tx 0.5 Rx -	3.8[b]	1.8[c]	0.16

[a] SPDT switch not included. [b] includes up-conversion block. [c] includes down-conversion block. [d] Single channel.

open circuited, and show < -40 dB coupling (Fig. 22). Second, the amplitude and phase of channel 1 was measured at a fixed phase state, while the phase of channel 2 (and other channels) was changed from 0 to $-335°$, as shown in Fig. 23. In all cases, the resulting rms gain and phase error in channel 1 is < 0.06 dB and 0.6° at 42–50 GHz. Both values are truly negligible and show very low on-chip coupling.

Finally, the S-parameters were measured over temperature and a gain drop of 7–8 dB is seen from 25 °C–100 °C, as shown in Fig. 24. In this case, a PTAT was not used, and in the future, optimized biasing circuits could alleviate some of the gain drop [16]. On the other hand, the rms gain and phase error remain essential constant over temperature, as expected from switched-*LC* phase shifters [1].

Table I compares the performance of this array with published work. It is seen that this work results in higher receive linearity than any other millimeter-wave phased array. The same design can also be built without the two SPDT switches, each with 2.7-dB insertion loss, resulting in either a standalone Tx or a Rx array with state-of-the-art NF, linearity, and output power for low dc power consumption.

V. CONCLUSION

This paper has presented a 16-element high-linearity 44–46-GHz silicon BiCMOS phased array with 4-bit phase control. A single-ended topology was employed with a passive phase shifter and a perfectly symmetrical 1:16 Wilkinson combiner network. Full EM modeling was done to predict the array performance, and the measurements agree well with simulations. It was found that, due to the single-ended design, the simulated ground inductance can have an effect on the transmit channel due to the absence of any emitter degeneration (in the Tx path). An expected, but still surprising, finding is the near-perfect on-chip gain and phase uniformity between the channels in the Tx and Rx modes. This means that silicon-based arrays may allow for a single calibration per chip, which will lower the cost of chip-level testing.

ACKNOWLEDGMENT

The authors thank Dr. J. Hacker and C. Hillman, both with Teledyne Scientific, Thousand Oaks, CA, for technical support and discussions. Author C.-Y. Kim thanks S. Y. Kim, University of California at San Diego (UCSD), La Jolla, for his help in the preparation of this paper's manuscript.

REFERENCES

[1] D. W. Kang, J. G. Kim, B. Min, and G. M. Rebeiz, "Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3534–3543, Dec. 2009.

[2] K. Koh, J. W. May, and G. M. Rebeiz, "A millimeter-wave (40–45 GHz) 16-element phased-array transmitter in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[3] K. Kim, K. Ahn, T. Lim, H. Park, and J. Yu, "A 60 GHz wideband phased-array LNA with short-stub passive vector generator," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 11, pp. 628–630, Nov. 2010.

[4] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A thirty two element phased-array transceiver at 60 GHz with RF-IF conversion block in 90 nm flip chip CMOS process," in *IEEE Radio Freq. Integr. Circuits Symp.*, May 2010, pp. 457–460.
[5] A. Valdes-Garcia, S. T. Nicolson, J. Lai, A. Natarajan, P. Chen, S. K. Reynolds, J. C. Zhan, D. Kam, D. Liu, and B. Floyd, "A fully integrated 16-element phased-array transmitter in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2757–2773, Dec. 2010.
[6] S. K. Reynolds, A. S. Natarajan, M. Tsai, S. Nicolson, J. C. Zhan, L. Duixian, D. G. Kam, O. Huang, A. Valdes-Garcia, and B. A. Floyd, "A 16-element phased-array receiver IC for 60-GHz communications in SiGe BiCMOS," in *IEEE Radio Freq. Integr. Circuits Symp.*, May 2010, pp. 461–464.
[7] Y. Yu, P. G. M. Baltus, A. Graauw, E. Heijden, C. S. Vaucher, and A. H. M. Roermund, "A 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1697–1709, Sep. 2010.
[8] T. Yu and G. M. Rebeiz, "A 4-channel 24–27 GHz CMOS differential phased-array receiver," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 455–458.
[9] A. Fischer, Z. Tong, A. Hamidipour, L. Maurer, and A. Stelzer, "A 77-GHz antenna in package," in *IEEE Eur. Microw. Conf.*, Oct. 2011, pp. 1316–1319.
[10] B. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.
[11] B. Min and G. M. Rebeiz, "Ka-band low loss and high isolation switches in 0.13 μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 6, pp. 1364–1371, Jun. 2008.
[12] Sonnet. ver. 12.56, Sonnet Softw. Inc., Syracuse, NY, 1986–2011.
[13] B. Cetinoneri, Y. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13 μm CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 1093–1096.
[14] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York: Wiley, 2004.
[15] J. Kim and J. F. Buckwalter, "A fully integrated Q-band bidirectional transceiver in 0.12-μm SiGe BiCMOS technology," in *IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2010, pp. 57–60.
[16] S. Kim and G. M. Rebeiz, "A low-power BiCMOS 4-element phased array receiver for 76–84 GHz radars and communication systems," *IEEE J. Solid State Circuits*, vol. 47, no. 2, pp. 359–367, Feb. 2012.

Choul-Young Kim (S'04–A'07) received the B.S. degree in electrical engineering from Chungnam National University (CNU), Daejeon, Korea, in 2002, and M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2004 and 2008, respectively.

From March 2009 to February 2011, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla. He is currently an Assistant Professor of electronics engineering with Chungnam National University, Daejeon, Korea. His research interests include millimeter-wave integrated circuits and systems for short-range radar and phased-array antenna applications.

Dong-Woo Kang (A'07) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2001, 2003, and 2007, respectively.

From September 2007 to September 2010, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla. He is currently with Samsung Electronics, Suwon, Korea. His research interests include CMOS/SiGe integrated circuits (ICs) for microwave and millimeter-wave phased-array systems.

Gabriel M. Rebeiz (S'86–M'88–SM'93–F'97) received the Ph.D. degree from the California Institute of Technology, Pasadena.

He is the Wireless Communications Industry Chair Professor of electrical and computer engineering with the University of California at San Diego (UCSD), La Jolla. From 1988 to 2004, he was with The University of Michigan at Ann Arbor. He has contributed to planar millimeter-wave and terahertz antennas and imaging arrays from 1988 to 1996, and his group has optimized the dielectric-lens antennas, which is the most widely used antenna at millimeter-wave and terahertz frequencies. His group also developed 6–18- and 40–50-GHz eight- and 16-element phased arrays on a single silicon chip, and the first millimeter-wave silicon passive imager chip at 85–105 GHz. His group also demonstrated high-Q RF microelectromechanical systems (MEMS) tunable filters at 1–6 GHz ($Q > 200$) and the new angular-based RF MEMS capacitive and metal-contact switches. As a consultant, he helped develop the USM/ViaSat 24-GHz single-chip SiGe automotive radar, phased arrays operating at X-, Ku-, and W-band for defense and commercial applications, the RFMD RF MEMS switch, and the Agilent RF MEMS switch. He is the Director of the UCSD/Defense Advanced Research Projects Agency (DARPA) Center on RF MEMS Reliability and Design Fundamentals. He has graduated 42 Ph.D. students and 15 post-doctoral fellows, and currently leads a group of 21 Ph.D. students and post-doctoral fellows in the area of millimeter-wave RF integrated circuits (RFICs), tunable microwaves circuits, RF MEMS, planar millimeter-wave antennas, and terahertz systems. He authored *RF MEMS: Theory, Design and Technology* (Wiley, 2003).

Prof. Rebeiz is a National Science Foundation (NSF) Presidential Young Investigator. He has been an associate editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and a Distinguished Lecturer for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) and the IEEE Antennas and Propagation Society (IEEE AP-S). He was a recipient of the URSI Koga Gold Medal Recipient, the IEEE MTT-S 2003 Distinguished Young Engineer, the IEEE MTT-S 2000 Microwave Prize, the IEEE MTT-S 2010 Distinguished Educator Award, and the IEEE AP-S 2011 John D. Kraus Award. He was also the recipient of the 1998 Eta Kappa Nu Professor of the Year Award and the 1998 Amoco Teaching Award given to the best undergraduate teacher at The University of Michigan at Ann Arbor, and the 2008 Teacher of the Year Award of the Jacobs School of Engineering, UCSD. His students have been the recipients of a total of 19 Best Paper Awards presented at IEEE MTT-S, RFIC, and AP-S conferences.