A 160-GHz Subharmonic Transmitter and Receiver Chipset in an SiGe HBT Technology

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***Abstract*—A monolithically integrated 160-GHz transmitter and receiver chipset with in-phase/quadrature baseband inputs and outputs and on-chip local oscillator (LO) generation has been implemented in a 0.25-μm silicon–germanium heterojunction bipolar transistor technology. The chipset features a three-stage differential power amplifier, a low-noise amplifier, up- and down-conversion subharmonic quadrature mixers, and an 80-GHz voltage-controlled oscillator equipped with a 1/16 frequency prescaler for frequency locking by an external phase-locked loop. To investigate the behavior of the Gilbert-cell-based subharmonic mixer operated close to $f_{\max}$, the correlation between LO phases and conversion gain is studied. The conclusion suggests that the maximum conversion gain can be obtained with certain LO phases at millimeter-wave frequencies. Over the 150–168-GHz bandwidth, the transmitter delivers an output power of more than 8 dBm with a maximum 10.6-dBm output power at 156 GHz. The receiver provides a noise figure lower than 9 dB and more than 25 dB of conversion gain at 150–162 GHz, including the losses of an auxiliary input balun. The transmitter and receiver chips consume 610 and 490 mW, respectively.**

***Index Terms*—Heterojunction bipolar transistors (HBTs), millimeter-wave integrated circuits, silicon germanium (SiGe), subharmonic, transceiver architectures.**

I. Introduction

MILLIMETER-WAVE transceivers with operating frequencies beyond 100 GHz, at the 2-mm atmospheric window (140–160 GHz), are currently mainly deployed for radio astronomy and remote-sensing applications [1] with very stringent system specification. Hence, present transceiver designs are optimized for high-power and low-noise performance and are typically implemented with discrete subsystems in waveguide technology using high-performance III–V-based semiconductors. There are, however, a number of emerging applications with much relaxed specifications, which call for fully integrated low-cost transceiver solutions in this frequency range. Examples include future 154-GHz automotive radar [2], high-resolution millimeter-wave imaging [3], and gigabit-rate wireless communication. Silicon–germanium (SiGe) HBT and BiCMOS technologies can meet the requirements of such systems by combining the integration and volume production capabilities of commercial silicon technology with good millimeter-wave performance.

However, with current SiGe technologies available, it is still challenging to design transceiver circuits beyond 100 GHz, mainly due to the difficulties of the local oscillator (LO) generation as the operation frequency is about one-third of $f_{\max}$. A few 160-GHz monolithic integrated transmitters or receivers based on a conventional heterodyne [4], [5], or zero-IF quadrature down-conversion architecture [6], have been demonstrated. These front-end architectures require the generation of a 160-GHz LO signal either by means of an integrated fundamental-frequency voltage-controlled oscillator (VCO) or a frequency multiplier. High-frequency VCOs are difficult to design for low power consumption and low phase noise, whereas multiplier-based LO chains are area and power consuming.

An alternative solution is offered by a polyphase subharmonic mixing architecture based on a Gilbert cell [7]. It provides two-stage down-conversion by multiplying the RF signal with the in-phase/quadrature (I/Q) components of the LO in two cascaded mixer cores. This allows the mixer to be operated from a more easily generated 70–80-GHz LO signal, and thus facilitates a harder switching of the mixer transistors, as required for higher efficient mixing and lower noise figure (NF). The subharmonic mixing approach combined with a fully differential circuit architecture also largely eliminates dc-offset problems in zero-IF applications caused by LO leakage to the receiver input since no strong fundamental or harmonic component of the LO signal is present within the RF bandwidth of the receiver front-end. Similar mixers driven by quadrature LO signals have been realized at microwave [8] and millimeter-wave [9]–[11] frequencies. In these designs, the quadrature LO signals are always required, but the reasons are not fully discussed. In addition, the above designs obtain quadrature LO signals either by the use of *RC*-polyphase filters, which suffer from high insertion losses, or a lower loss branch-line 90° hybrid at the cost of a relatively large die area and narrow bandwidth.

This paper presents a detailed study on the LO phases of the Gilbert-cell-based subharmonic mixer, which promotes a better understanding of how the LO phases impact the conversion gain

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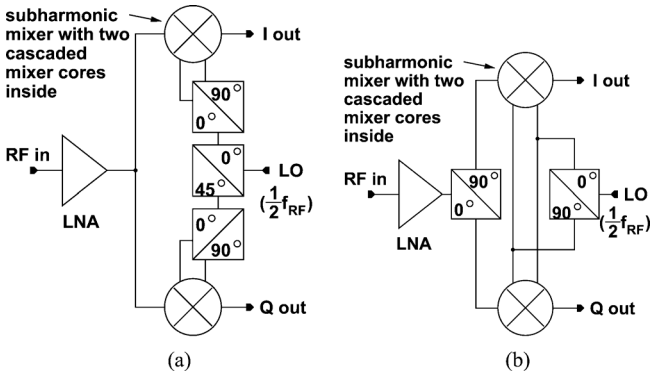


Fig. 1. Two receiver schemes for subharmonic I/Q conversion. (a) 45° phase shift on the LO signal. (b) 90° phase shift on the RF signal.

and NF of the mixer operated close to $f_{\max}$. A monolithic integrated 160-GHz transmitter and receiver with a three-stage differential power amplifier (PA), a differential low-noise amplifier (LNA), up- and down-conversion subharmonic quadrature mixers with I/Q-baseband inputs/outputs, and an on-chip 80-GHz VCO with a prescaler for external frequency locking by a phase-locked loop (PLL) is then demonstrated in a 0.25-μm SiGe HBT technology. Additionally, a compact low-loss 90° coupler is introduced to generate quadrature LO signals.

This paper is arranged as follows. Section II introduces the system architectures and the detailed study on the mixer LO phases. Section III presents the electrical design of circuits while the SiGe technology and layout is described in Section IV. Finally, Section V presents the characterization setup and results, and conclusions are provided in Section VI.

II. System Design

A. Quadrature Conversion Scheme

In a subharmonic mixer, the IF frequency is determined by

$$f_{\mathrm{IF}} = \pm f_{\mathrm{RF}} \mp 2f_{\mathrm{LO}}. \tag{1}$$

In order to realize a quadrature up-/down-conversion in subharmonic mode, two LO signals with 45° phase shift are needed due to the phase/frequency doubling of the LO signal in the mixer. A commonly used system architecture is shown in Fig. 1(a), but there are two drawbacks in this solution. First, 45° outputs are hardly available in standard hybrid coupler design without sacrificing amplitude balance. Second, two extra 90° couplers are required to provide quadrature LO signals for each mixer with two cascaded mixer cores. Therefore, an alternative quadrature mixing solution, shown in Fig. 1(b), is proposed to avoid the 45° issue by separation of the RF signal into quadrature paths, similar to the 60-GHz receiver presented in [12], so that the quadrature mixing can be realized.

Based on the proposed scheme, the system diagram of our transmitter and receiver chipset is depicted in Fig. 2. In the receiver, a three-stage differential LNA is used at the input to provide sufficient gain and suppress the noise of the down-converter. The amplified 160-GHz RF signal is divided into an I/Q

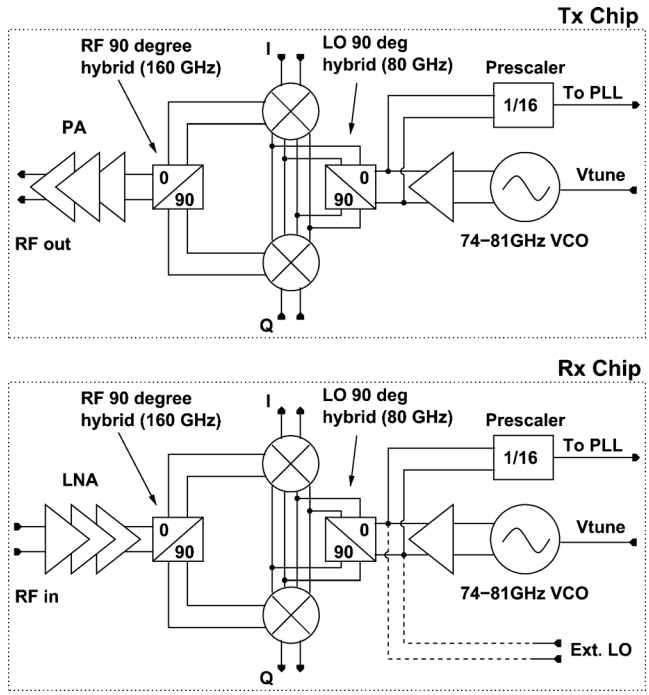


Fig. 2. Block diagram of the integrated 160-GHz transmitter and receiver, with separate I/Q paths, cascaded mixer cores for subharmonic up-/down-conversion, on-chip generation of the 80-GHz LO signal, and an optional external LO port.

path through a 90° coupler and fed to cascaded mixers. In the transmitter, an I/Q signal are fed to cascaded quadrature mixers and up-converted to RF frequency in an I/Q path. The RF power of the two paths are then combined by a 90° coupler and further amplified by a three-stage differential PA. The differential output of the PA and input of the LNA can be directly interfaced to balanced on- or off-chip antennas, such as folded-dipole radiators. The on-chip VCO provides the 80-GHz LO signal to the mixers through a buffer amplifier and a 90° coupler. The VCO output is also fed to a 1/16 frequency divider in order to provide a 5-GHz signal for locking of the VCO by an external low-frequency PLL.

B. Study on Mixer LO Phases

In our proposed system architecture, both quadrature RF and LO paths are required. The quadrature RF path is needed for quadrature up-/down-conversion, while understanding the purpose of the quadrature LO path requires knowledge on how the LO phases relate to the mixer performance, such as conversion gain and NF.

Operation of the Gilbert-cell-based subharmonic mixer can be understood as two cascaded fundamental mixers, shown in Fig. 3. In large-signal operation, an ideally switching LO signal can be defined as a 50% duty-cycle square wave whose Fourier series consists of odd harmonic frequencies. If ω is the LO fundamental frequency, the LO square wave involved in fundamental mixer 1 can be described as

$$\mathrm{LO}(t) = \frac{4}{\pi} A_{\mathrm{LO}} G_{\mathrm{LO}} \sum_{m=0}^{\infty} \frac{1}{2m+1} \sin[(2m+1)\omega t]. \tag{2}$$

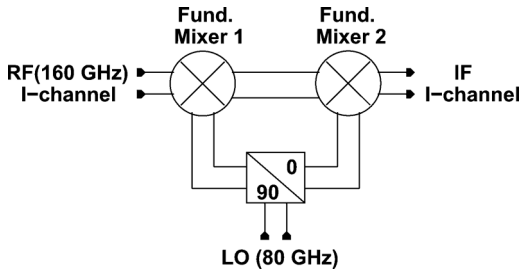


Fig. 3. Block diagram of the subharmonic mixer.

The LO square wave in mixer 2 with an arbitrary phase shift ϕ is

$$\mathrm{LO}(t+\frac{\phi}{\omega}) = \frac{4}{\pi}A_{\mathrm{LO}}G_{\mathrm{LO}}\sum_{n=0}^{\infty}\frac{1}{2n+1} \times \sin[(2n+1)\omega t + (2n+1)\phi] \quad (3)$$

where A_{LO} is the voltage amplitude of the LO signal, and G_{LO} stands for the voltage gain of the LO signal inside the mixer.

The IF signal is obtained by the operation of $\mathrm{RF}(t)\times\mathrm{LO}(t)\times \mathrm{LO}(t+\phi/\omega)$. Assuming a lower sideband RF signal in the I-channel down-conversion mixer,

$$\mathrm{RF}(t) = A_{\mathrm{RF}}G_{\mathrm{RF}}\cdot\cos(2\omega-\omega_{\mathrm{IF}})t \quad (4)$$

where ω_{IF} is the IF frequency, A_{RF} is the voltage amplitude of the RF signal, and G_{RF} denotes the voltage gain of the RF signal inside the mixer. The initial phase of the RF signal is set to zero for simplicity. The overall mixing products can be expressed as

$$\begin{aligned}&\mathrm{RF}(t)\times\mathrm{LO}(t)\times\mathrm{LO}\left(t+\frac{\phi}{\omega}\right)\\ &= \frac{4}{\pi^2}A_{\mathrm{RF}}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2\sum_{m,n=0}^{\infty}\frac{1}{(2m+1)(2n+1)}\\ &\quad\{-\sin[((2m+2n)\omega+\omega_{\mathrm{IF}})t+(2n+1)\phi]\\ &\quad-\sin[((2m-2n+2)\omega-\omega_{\mathrm{IF}})t-(2n+1)\phi]\\ &\quad+\sin[((2m-2n-2)\omega+\omega_{\mathrm{IF}})t-(2n+1)\phi]\\ &\quad+\sin[((2m+2n+4)\omega-\omega_{\mathrm{IF}})t+(2n+1)\phi]\} \quad (5)\end{aligned}$$

where m and n denote the $(2m+1)$th and $(2n+1)$th harmonics of the LO signal. Four terms with different frequency components are obtained in the above equation, but only the first three terms could result in IF products, if the coefficients in front of ω are zero. Hence,

$$m = n = 0 \quad (6)$$

$$n = m+1 \quad (7)$$

$$m = n+1. \quad (8)$$

Thus, (6) stands for the mixing of the fundamental $\mathrm{LO}(t)$ with the fundamental $\mathrm{LO}(t+\phi/\omega)$, while (7) indicates the mixing of the $(2m+1)$th harmonic of $\mathrm{LO}(t)$ with the $[2(m+1)+1]$th harmonic of $\mathrm{LO}(t+\phi/\omega)$, and likewise, (8) is the mixing of the $(2n+1)$th harmonic of $\mathrm{LO}(t)$ with the $[2(n+1)+1]$th harmonic of $\mathrm{LO}(t+\phi/\omega)$. For $m=n=0$, the IF signal is

$$\mathrm{IF}_0(t) = -\frac{4}{\pi^2}A_{\mathrm{RF}}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2\cdot\sin(\omega_{\mathrm{IF}}t+\phi) \quad (9)$$

and for $n=m+1$, we have

$$\mathrm{IF}_1(t) = \frac{4}{\pi^2}A_{\mathrm{RF}}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2\sum_{m=0}^{\infty}\frac{1}{(2m+1)(2n+1)} \times\sin(\omega_{\mathrm{IF}}t+(2m+3)\phi) \quad (10)$$

and for $m=n+1$,

$$\mathrm{IF}_2(t) = \frac{4}{\pi^2}A_{\mathrm{RF}}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2\sum_{n=0}^{\infty}\frac{1}{(2m+1)(2n+1)} \times\sin(\omega_{\mathrm{IF}}t-(2n+1)\phi). \quad (11)$$

Combining (9)–(11), we can write the mixer conversion gain as

$$CG = \frac{4}{\pi^2}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2 \times\left\{1-\sum_{k=0}^{\infty}\left[\frac{2}{(2k+1)(2k+3)}\right]\cos[(2k+2)\phi]\right\}. \quad (12)$$

The derivative of CG with respect to ϕ leads to the maximum or minimum conversion gain if

$$\phi = N\cdot\frac{\pi}{2}, \qquad N=0,1,2,\ldots. \quad (13)$$

For in-phase LO signals ($\phi=0$), (12) can be simplified as

$$CG = \frac{4}{\pi^2}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2\left\{1-\sum_{k=0}^{\infty}\frac{2}{(2k+1)(2k+3)}\right\} = 0 \quad (14)$$

noted that the summation of the above infinite series is 1.

For quadrature LO signals ($\phi=\pi/2$), (12) can be developed as

$$CG = \frac{4}{\pi^2}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2 \times\left\{1-\sum_{k=0}^{\infty}\frac{2}{(2k+1)(2k+3)}\cos[(k+1)\pi]\right\} \quad (15)$$

noting that the summation of the infinite series in (15) is

$$\sum_{k=0}^{\infty}\frac{2}{(2k+1)(2k+3)}\cos[(k+1)\pi] \approx -0.57. \quad (16)$$

The mixer conversion gain with I/Q LO signals is expressed as

$$CG = \begin{cases}0, & \text{if } \phi=0\\ 1.57\times\frac{4}{\pi^2}A_{\mathrm{LO}}^2G_{\mathrm{RF}}G_{\mathrm{LO}}^2, & \text{if } \phi=\frac{\pi}{2}.\end{cases} \quad (17)$$

Therefore, (17) confirms that in-phase LO signals provide zero conversion gain while quadrature LO signals provide a maximum conversion gain, assuming that the Gilbert-cell-based subharmonic mixer is pumped by LO signals with ideal square waveforms. Sweeping the phase ϕ from 0° to 360° in (12),

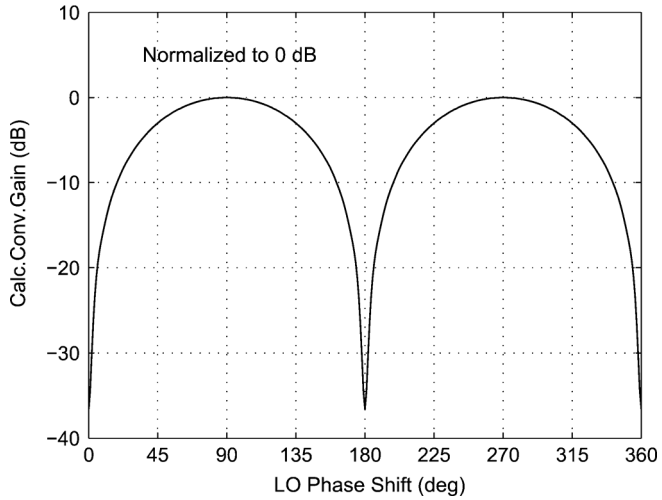


Fig. 4. Calculated conversion gain with sweeping ϕ and up to 41st LO harmonics considered (k is up to 20). The peak conversion gain is normalized to 0 dB.

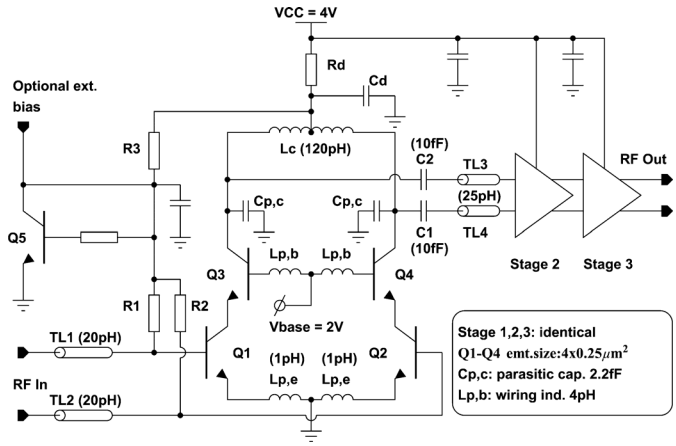


Fig. 5. Schematic diagram of the three-stage differential LNA detailing the first stage and its important capacitive and inductive layout parasitics.

a correlation between the mixer LO phases and conversion gain in decibel is plotted in Fig. 4. The peak and valley of the conversion gain curve appear at 90°/270° and 0°/180° LO phase shifts, respectively, supporting that quadrature LO signals result in a maximum mixing efficiency.

The variation of conversion gain with respect to the LO phase shift is briefly explained as follows. For the in-phase LOs, the mixer suffers zero conversion gain because the IF product $f_{\mathrm{RF}} - f_{\mathrm{LO},0^\circ} - f_{\mathrm{LO},0^\circ}$ is completely canceled by the rest of the 180° out-of-phase IF products $f_{\mathrm{RF}} - mf_{\mathrm{LO},0^\circ} - nf_{\mathrm{LO},0^\circ}$, $(m, n = 0, 1, 2, \ldots)$. For the quadrature LOs, a highest conversion gain is obtained because the IF product $f_{\mathrm{RF}} - f_{\mathrm{LO},0^\circ} - f_{\mathrm{LO},90^\circ}$ is strengthened by the I IF products $f_{\mathrm{RF}} + (2n+1)f_{\mathrm{LO},0^\circ} - (2n+3)f_{\mathrm{LO},90^\circ}$ and $-f_{\mathrm{RF}} + (2n+3)f_{\mathrm{LO},0^\circ} - (2n+1)f_{\mathrm{LO},90^\circ}$, though partly canceled by the 180° out-of-phase IF products $f_{\mathrm{RF}} + (2n+3)f_{\mathrm{LO},0^\circ} - (2n+5)f_{\mathrm{LO},90^\circ}$ and $-f_{\mathrm{RF}} + (2n+5)f_{\mathrm{LO},0^\circ} - (2n+3)f_{\mathrm{LO},90^\circ}$, where $n = 0, 1, 2, \ldots$.

The RF–IF and LO–IF isolations can be also derived from (5).

III. Transmitter and Receiver Design

A. LNA Design

A schematic diagram detailing the first stage of the three-stage differential LNA is shown in Fig. 5. The transistors Q1–Q4 are arranged in a differential cascode configuration in order to maximize the gain and reverse isolation per stage. Devices with an emitter-window size of $A_E = 4 \times 0.25\ \mu\mathrm{m}^2$ biased at $I_C = 2.8$ mA were selected for the cascode since it yields an optimum differential source impedance for minimum NF equal to a 100-Ω system impedance. The output of the cascode is impedance-matched to the 100-Ω system impedance by a conventional LC-tank consisting of a center-tapped differential shunt inductor $L_C = 120$ pH and 10-fF output series capacitors C_1/C_2. With a 4-pH parasitic wiring inductance $L_{p,b}$ in each of the base connections of Q3/Q4 and $L_{p,e}$ in the emitter connections of Q1/Q2, a small amount of gain peaking and emitter degeneration of the stage is obtained. This leads to a simulated 10-dB gain, 8-dB NF, and 6-dB return loss of the first stage at 160 GHz. Lower input return loss can be obtained by increased inductive degeneration, which increases the real part of input impedance.

The LNA was designed with three cascaded stages in order to secure sufficient gain for a low system NF in the presence of potential process parameter changes. Since the input stage is equipped with large devices, it has a high enough compression point to be used as the intermediate and the final stage of the amplifier. Hence, the three-stage LNA has been designed as three cascaded identical stages. Individual optimization of each stage can, however, yield improved bandwidth and linearity of the amplifier. The power supply voltage to each stage is low-pass filtered by the *RC* network $R_d = 50\ \Omega/C_d = 0.8$ pF in order to suppress any common-mode instabilities due to power-rail crosstalk in the multistage amplifier.

B. Subharmonic I/Q Mixer Design

Fig. 6(a) presents the schematic diagram of the subharmonic I/Q receiver mixer.

The 160-GHz RF output signal of the LNA is split into an I/Q path by the −3-dB differential 90° coupler. Separate RF stages Q1/Q2 and Q3/Q4 with emitter areas $A_E = 4 \times 0.25\ \mu\mathrm{m}^2$ are used for the I/Q channel. The subharmonic down-conversion is performed by two stacked switching quads in each channel, consisting of the devices Q5–Q20. This arrangement provides current sharing between the cascaded mixer cores at the cost of an increased supply voltage. Each of the four switching quads is equipped with small $A_E = 1 \times 0.25\ \mu\mathrm{m}^2$ devices biased at a quiescent current $I_{CQ} = 0.9$ mA in order to minimize the LO-drive power requirement. In each quad, the transistors are arranged as two $BECEB$ cells with shared collector terminals.

Equation (15) discussed above is helpful to understand the benefit of quadrature LO signal in Gilbert-cell-based subharmonic mixer, but in reality, the behavior of conversion gain is not in agreement with the above discussions due to the limited circuit bandwidth, thus only lower harmonics are involved in the mixing and suffer from different gain with respect to frequency, which can be described by the gain-magnitude frequency response of the differential pair used in quads. As shown

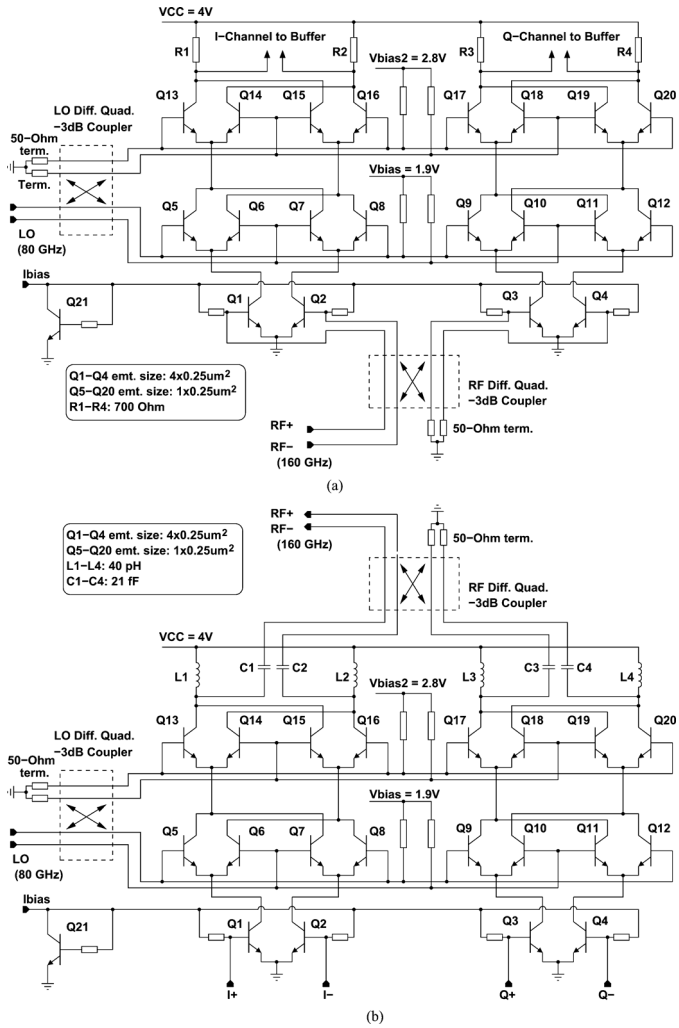


Fig. 6. Schematic of the: (a) subharmonic I/Q receiver mixer and (b) transmitter mixer.

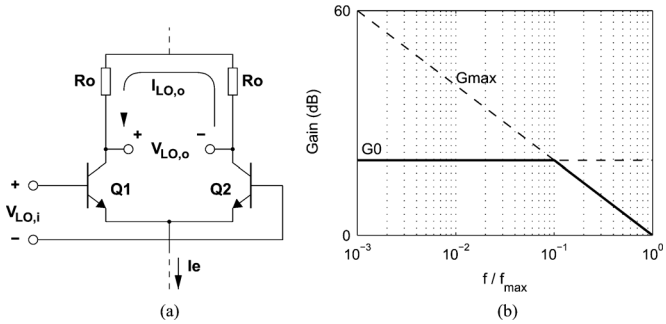


Fig. 7. Analysis of differential pair used in the mixer quad. (a) Schematic and (b) large-signal gain response.

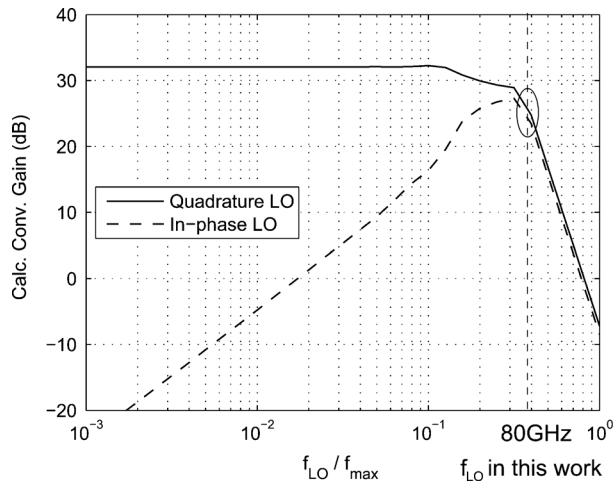


Fig. 8. Calculated conversion gains with respect to the ratio of $f_{\rm LO}/f_{\rm max}$.

in Fig. 7(a), the differential pair is operated in a large-signal mode, steering the emitter current I_e back and forth between two transistors. With a strong input signal at low frequencies, the output waveform of the differential pair is clipped as a square wave with peak-to-peak voltage swing of I_eR_o, where R_o is the equivalent load resistance at collectors. Thus, given a fixed input power, the large signal gain of the differential pair is a constant value G_0 with respect to frequency. However, the gain drops at high frequencies where the maximum power gain $G_{\rm max}$ is not high enough to push the output voltage swing beyond I_eR_o. Combining the gain at low and high frequencies, we have a large-signal gain curve shown in Fig. 7(b). It can be described in decibels as

$$\mathrm{dB}[G] = \begin{cases} \mathrm{dB}[G_0], & \text{if } f < f_{\rm corner} \\ -10\log\left(\frac{f}{f_{\rm max}}\right), & \text{if } f > f_{\rm corner} \end{cases} \tag{18}$$

where $f_{\rm corner}$ is the frequency when $G_{\rm max} = G_0$. Replacing the $G_{\rm LO}$ term in (2) and (3) by (18) and modifying (12), the conversion gain with I/Q LOs is plotted in Fig. 8 by using numerical calculation with proper assumption of $A_{\rm LO}$, G_0, and $f_{\rm max}$ according to the input LO power, the transistor size and bias current in the design. The conversion gain curves move closer to each other as frequency increases, leading to less variation of conversion gain over 360° LO phase shift at higher LO frequencies. It should be noted that Fig. 8 is only intended to qualitatively describe the correlation between the mixer conversion gain and LO phases over frequency, ignoring all the parasitic effects of transistors.

However, the optimum LO phases drift away from 90° at millimeter-wave frequencies mainly due to the base–emitter capacitance C_{be}. In the mixer quads, transistors can be regarded as common base (CB) stages during the switching-on period for the RF signals. The CB stage and its small-signal equivalent circuit are depicted in Fig. 9(a), where I_e is an input ac current and I_c is the output. They are in phase at low frequencies, but out-of-phase at millimeter-wave frequencies. As shown in Fig. 9(b), voltage V_e has a phase delay of Δd with respect to I_e due to the *RC* constant of C_{be} and the emitter resistance r_e. Δd can be calculated as

$$\Delta d = \phi(V_e) - \phi(I_e) = -\arctan(\omega r_e C_{be}). \tag{19}$$

Ignoring the Miller capacitance for simplicity, I_c and V_e are in phase. Thus, I_c is delayed by Δd with respect to I_e. For the receiver mixer core shown in Fig. 10(a), the transistors that are switched off by the LOs are drawn in gray for a better understanding of the large-signal operation. As depicted in Fig. 10(b), I_{2+} and I_{2-} are the sequence of I_{1+} and I_{1-} chopped by $V_{{\rm LO},i}$

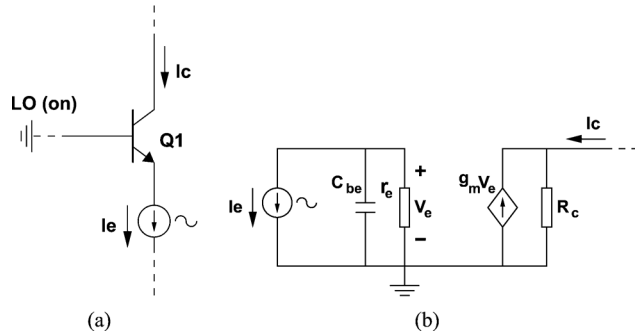


Fig. 9. Analysis C_{be} influence on the phase delay between I_c and I_e.

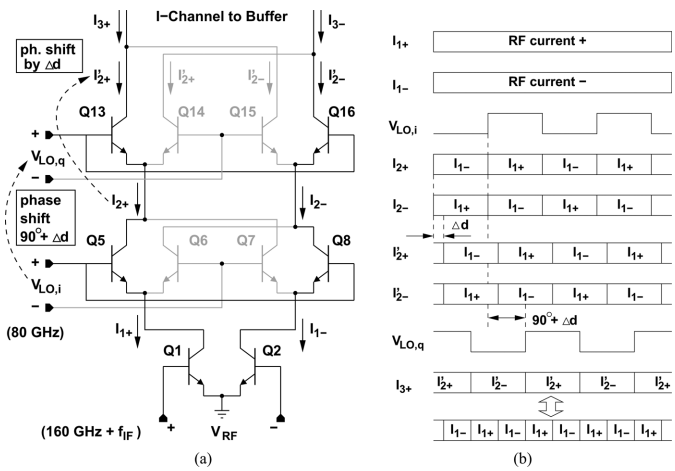


Fig. 10. Analysis of nonquadrature LO phases in mixer: (a) mixer core and (b) time-domain analysis.

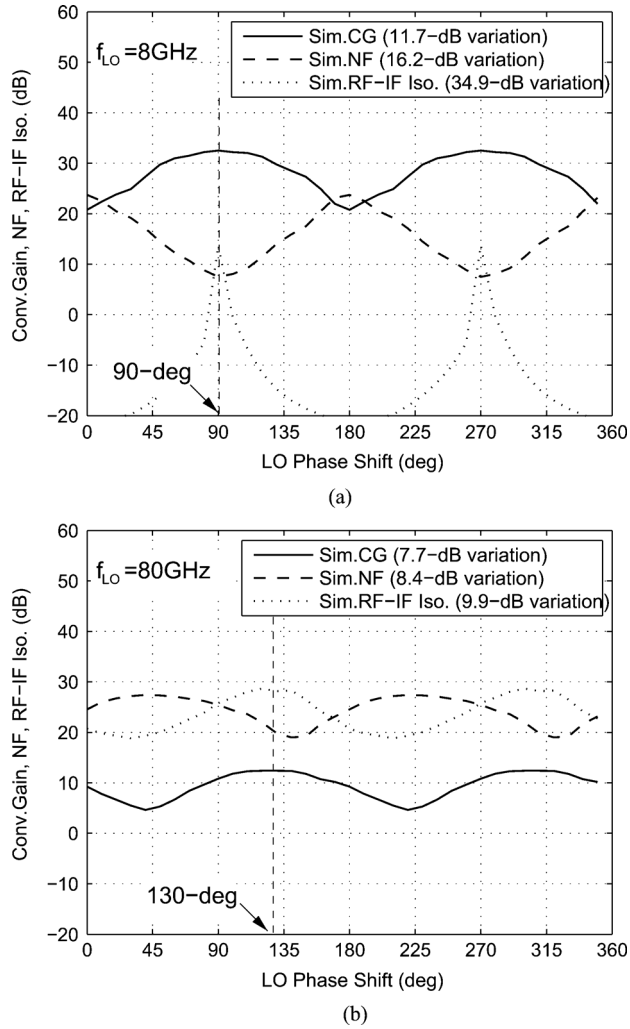


Fig. 11. Simulated conversion gain, NF, and RF–IF leakage of the mixer with respect to LO phase shift. The mixer is pumped by: (a) 8- and (b) 80-GHz LO, delivering an IF signal at 100 MHz.

in the lower quads, and are further chopped by $V_{\mathrm{LO},q}$ in the higher quads and merged into I_{3+} and I_{3-}. For the higher quads, I'_{2+} and I'_{2-} is the collector current response of the emitter current I_{2+} and I_{2-}, respectively. There is a phase delay of Δd between I'_{2+} and I_{2+} and I'_{2-} and I_{2-}, which requires the same phase delay on the quadrature LO signals for alignment in time slot. Therefore, the phase of input "quadrature" LO signals for the higher quads should be compensated by an extra phase shift of Δd. It should be noted that the ω in (19) is equal to $\omega_{\mathrm{RF}} - \omega_{\mathrm{LO}}$ for the down-converter and $\omega_{\mathrm{LO}} + \omega_{\mathrm{IF}}$ for the up-converter. Fig. 11 compares the three performances at the different LO frequencies, 8 and 80 GHz. The maximum conversion gain, minimum NF, and the best RF–IF isolation are obtained at 90° and 130° phase shifts, respectively, and their variations are smaller at 80-GHz LO frequency than at 8 GHz, leading to a higher tolerance on phase error of the coupler. The minimum NF is obtained at the peak conversion gain for their inversely proportional relationship. The best RF-IF isolation also appears at the peak conversion gain since more RF power is involved into down-conversion instead of leaking into IF.

Although the mixer conversion gain is not maximized with a 90° coupler used in the 80-GHz LO path, it is still close to the peak value due to its less variation over the LO phases at 80 GHz. According to the simulation, the mixer has a 10.8-dB conversion gain and a 25-dB NF at 90° LO phase shift. Compared to the maximum 12.4-dB conversion gain and the minimum 19-dB NF at the 130° LO phase shift, the system conversion gain is decreased by 1.6 dB and the NF is increased by 0.2 dB at 90° LO phase shifts, assuming a 30-dB-gain LNA is used in front of the mixer. Therefore, the -3-dB 90° coupler is still used to provide quadrature 80-GHz LO signals to the two stacked switching quads without sacrificing much performance degradation. The optimum LO phase distribution will be implemented in future work by investigating a novel hybrid coupler with arbitrary phase shift.

Resistive collector loads are used together with emitter–follower output buffers to provide wideband I/Q-baseband outputs.

In the up-conversion subharmonic mixer, shown in Fig. 6(b), the mixer core is reused by swapping the IF and RF ports. At the RF ports, resistive collector loads and emitter–follower output buffers are replaced by the *LC* matching networks and the 90° coupler.

C. PA Design

The PA uses a differential cascode circuit topology for high gain and high output power, shown in Fig. 12. The differential architecture provides an additional 3-dB output power. In order

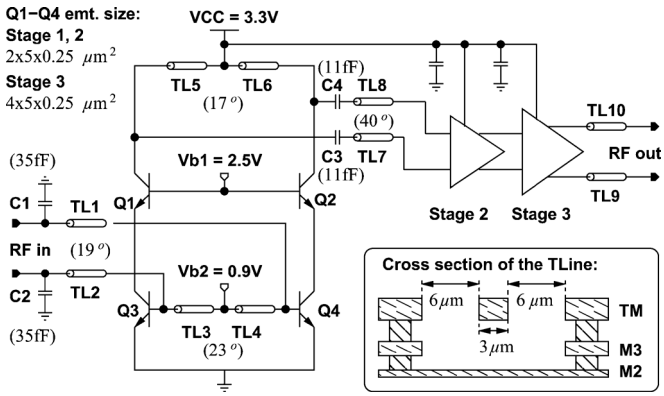


Fig. 12. Schematic diagram of the three-stage differential PA.

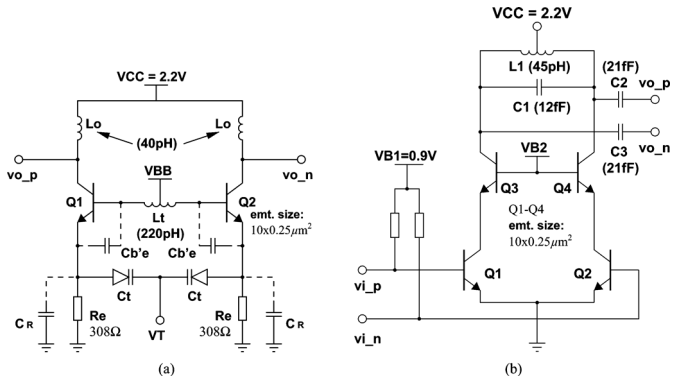


Fig. 13. VCO: (a) core and (b) buffer amplifier schematic.

to accommodate large input power, each transistor device used in the first and second stage is made of two parallel connected two $BECEB$ cells with the emitter-window size of $A_E = 5 \times 0.25\ \mu\text{m}^2$. The optimum bias current for each transistor is 7 mA. In order to enhance the output compression point, each transistor used in the third stage is arranged as four $BECEB$ cells mentioned above and biased at a 14-mA quiescent current. The standard LC matching network is used to match the input and output impedance to 100 Ω. The inductors are implemented by microstrip lines with side-ground shields to reduce the cross-coupling effect. A 50-Ω characteristic impedance of the transmission line is obtained from a 2.8-μm-thick and 3-μm-wide conducting strip on the top metal layer with a 6-μm distance to the side-ground shields built from metal 2 to the top metal, depicted in Fig. 12.

D. VCO and LO Buffer Design

The Colpitts topology is widely used in millimeter-wave oscillator design for its low phase noise. As shown in Fig. 13(a), a modified Colpitts topology is used for our 80-GHz VCO design. L_t is the resonating inductor, while L_o works as the output matching inductor. For a low phase-noise oscillation, the transistor size and bias current are the first important consideration. Transistors with a $10 \times 0.25\ \mu\text{m}^2$ emitter area biased with a 2.5-mA current are used in the VCO core. The second major contributor to the phase noise is the current source connected to the emitters. Instead of using a transistor, the resistors (R_e) are used for proper bias current since the flicker noise of transistor dominates the close-carrier phase noise. Alternatively, a quarter-wavelength transmission line can feed bias current and block the ac signal, but it was not employed in this design due to its large area requirements. The third factor that must be considered is the tradeoff between the phase noise and the tuning range. The resonating inductor L_t and output inductor L_o have been selected as 220 and 40 pH, respectively, to cover a simulated 10-GHz bandwidth (by a 0.4–5-V tuning voltage) without sacrificing much phase-noise performance. The fourth design parameter, according to the phase-noise theory of the Colpitts oscillator [13], [14], is the capacitive divider ratio n. To calculate n, the parasitic PN-junction capacitance $C_{b'e}$ and the parasitic parallel capacitance of the resistor C_R must be considered as follows:

$$n = \frac{C_t + C_R}{C_t + C_R + C_{b'e}} \tag{20}$$

where C_t is the capacitance of the varactor. The optimized n value is related with the quality factors of the inductors and varactors and bias current. The n value is set between 0.3 and 0.4 considering the above transistor size, bias current, and inductor configurations.

The VCO buffer is designed as a differential cascode, as shown in Fig. 13(b), equipped with a differential L-match tank circuit. To shrink the size of the matching inductor L_1, a capacitor C_1 is added in parallel. The series matching capacitors, C_2 and C_3, are 21 fF. The simulated power gain is 10 dB with a 3-dB bandwidth from 68 to 93 GHz, covering the whole tuning range of the VCO. The simulated maximum output power delivered by the VCO and the buffer is 5 dBm.

E. Frequency Prescaler Design

Static frequency dividers are used in the frequency prescaler chain. The first divider stage operates at 80 GHz. As shown in Fig. 14, resistors R_1–R_4 and transistors Q_1–Q_4, and Q_8–Q_{11} form a feedback loop that determines the input sensitivity of the divider. In the first stage, a 30-Ω load resistor and transistors with an emitter area of $4 \times 0.25\ \mu\text{m}^2$ are used. The simulated input sensitivity at 80 GHz is -8 dBm. In order to minimize the impact of the input impedance of the divider on the impedance matching between the output of buffer and the input of mixer, a pair of 66-pH series inductors, L_1 and L_2, are introduced at the differential input of the divider, leading to a 2-dB reduction of the input sensitivity.

IV. SiGe Technology and Layout

A. SiGe HBT Technology

The receiver is fabricated in an advanced SiGe bipolar technology, which has been derived within the DOTFIVE project from Infineon's high-speed bipolar production process B7HF200. B7HF200 is qualified for automotive applications such as 77-GHz adaptive cruise control, and it is based on the process described in [15]. The transistors are realized

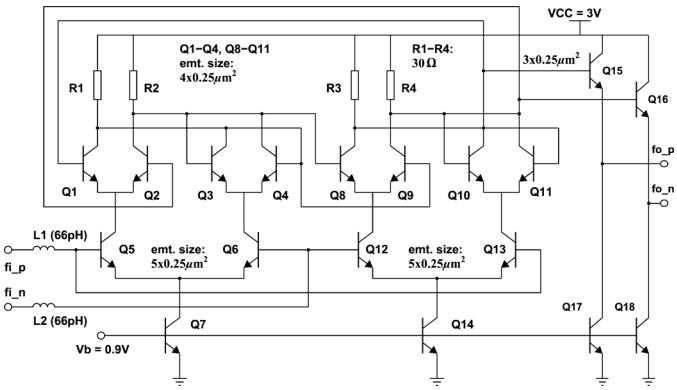


Fig. 14. Schematic showing the input divider stage of the four-stage 1/16 LO prescaler.

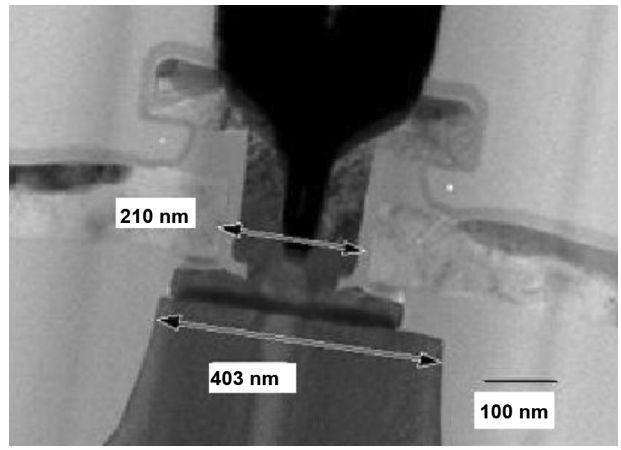


Fig. 15. TEM cross section of the npn transistor with an emitter window opening of 0.21 μm.

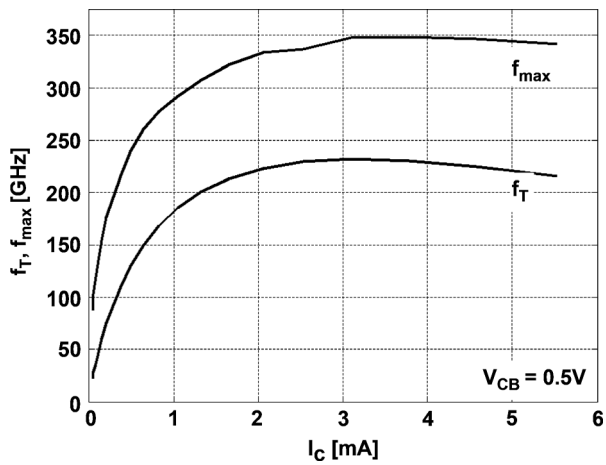


Fig. 16. f_T and $f_{\max}$ versus collector current for a device with an effective emitter size of $0.12 \times 2.7\ \mu\text{m}^2$.

in a double-polysilicon self-aligned transistor concept with shallow and deep trench isolation. The SiGe base is deposited by selective epitaxy. With B7HF200 as a starting point, the npn transistors have been significantly scaled laterally and vertically. The emitter window width has been reduced from 0.35 to 0.23 μm. By additionally reducing the emitter–base spacer width from 75 to 45 nm, this yields a reduction of the effective emitter width from 0.2 to 0.14 μm. These measures simultaneously reduce base collector capacitance C_{BC}, base emitter capacitance C_{BE}, and base resistance R_B. Furthermore, the active area opening in the STI oxide has been reduced by more than a factor of 2 to reduce C_{BC} and the width of the emitter polysilicon was decreased for reducing C_{BE} and R_B. To increase the transit frequency f_T of the transistors, the vertical scaling steps included tighter SiGe base profiles with an increased Ge content of 30%, as well as a reduction of collector thickness. The peak current gain of these transistors is about 1500 at a base–emitter voltage of 0.8 V. The collector–emitter breakdown voltage with open base BV_{CE0} is 1.5 V and the collector–base breakdown voltage BV_{CB0} is 5.5 V. The npn transistors achieve a transit frequency f_T of 234 GHz and a maximum oscillation frequency $f_{\max}$ of 335 GHz. The minimum gate delay of the current-mode-logic (CML)-based ring oscillators fabricated with these transistors is 2.6 ps. A further laterally scaled version of the device with an emitter window width of 0.21 μm and an effective emitter width of 0.12 μm achieves an f_T of 230 GHz, an $f_{\max}$ of 350 GHz, and a CML gate delay of 2.5 ps. A TEM cross section of such a transistor is shown in Fig. 15, and the f_T and $f_{\max}$ characteristics are depicted in Fig. 16.

The process provides two types of polysilicon resistors with sheet resistances of 150 and 1000 $\Omega/\square$, and TaN thin-film resistors with a sheet resistance of 20 $\Omega/\square$. A metal–insulator–metal (MIM) capacitor with Al_2O_3 dielectric and a specific capacitance of 1.4 fF/μm^2 is integrated in the four-layer copper metallization. By using a double-epitaxy concept [16], the process further provides high-voltage npn transistors with breakdown voltages BV_{CE0} of 3.5 V and BV_{CB0} of 14 V with an f_T of 60 GHz on the same dies as the high-speed npn devices. This double-epitaxy concept has also allowed the implementation of varactor diodes with a capacitance ratio C (5 V)/C (0 V) of 2.3 and quality factors of about 8 at a frequency of 77 GHz.

B. Quadrature Couplers

The 80- and 160-GHz differential 90° $-$3-dB couplers used for the generation of RF and LO quadrature signals have been implemented with two stacked two-wire transmission lines in adjacent M3/M4 metal layers, as shown in Fig. 17. In contrast to a traditional coplanar stripline (CPS), these differential transmission lines are fully embedded in the SiO_2 backend. Hence, a high degree of coupling can be obtained since the phase velocity of the odd and even modes in the coupled lines are similar. The coupler was optimized using a 3-D electromagnetic (EM) simulation tool (HFSS). For a -3-dB coupling ratio and a 100-Ω system impedance, conductors with $w = 7$ μm width and $s = 8$ μm spacing have been used. The length of the coupler transmission lines corresponds to $\lambda_g/4$ and is 400 μm at 80 GHz and 200 μm at 160 GHz. In order to obtain a more compact coupler with the ports spaced closer together, the transmission lines have been folded into a C-shape.

The simulations of the two couplers are presented in Fig. 18. The 80-GHz coupler with the isolated port terminated in a 100-Ω load shows a maximum amplitude error of 0.4 dB and a phase error of 6° in the quadrature output signals over a 70–90-GHz frequency range. The simulated excess insertion

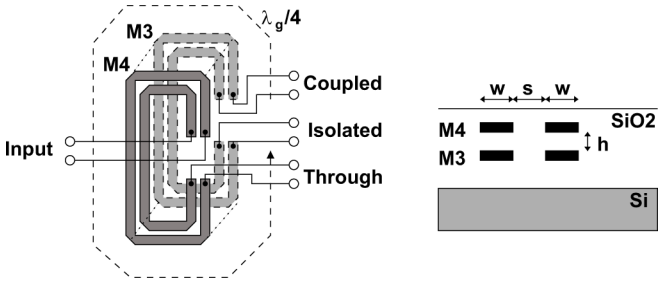


Fig. 17. Layout and cross section of the differential 80- and 160-GHz 90° couplers.

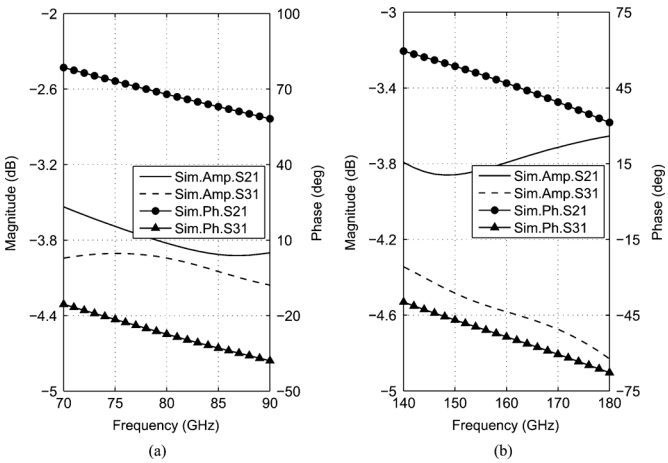


Fig. 18. Simulated amplitude and phase balance of the: (a) 80- and (b) 160-GHz coupler.

loss is 0.8 dB. For the 160-GHz coupler, a 10° maximum phase error and a 1.2-dB amplitude error over 140–180-GHz is obtained. The simulated input return losses are better than 10 dB for all the ports.

C. LNA LC-Tank

The LNA *LC*-tank has been implemented with a center-tapped lumped rectangular shunt inductor in the M4 top metal layer and series metal–oxide–metal (MOM) plate capacitors. The 30×25 μm^2 large inductor is surrounded by a grounded M1–M4 metal and via fence in order to minimize crosstalk to nearby circuit elements. Substrate contacts along the perimeter of the inductor area tie the substrate to ground potential. The 10-fF series MOM capacitors use 15×18 μm large plates in the M3–M4 layers. The influence of the parasitic substrate capacitance is minimized by connecting the sensitive high-impedance collector nodes to the top plates of the capacitors, whereas the relatively low-impedance 100-Ω output port of the stage is connected to the substrate-facing bottom plates.

The via and wire interconnects in the *LC*-tank, as well as its connections to the transistors and output port, provide a substantial parasitic inductance and capacitance at the 160-GHz operating frequency. Hence, a post-layout EM S-parameter simulation of the full *LC*-tank of each stage has been performed, with ports for the transistor collector nodes and their corresponding output ports, as well as the collector power-supply port of the inductor. By importing the resulting five-port S-matrix of the complete tank into the circuit simulator, the lumped elements can be resized to absorb the parasitics of the interconnects in order to obtain a good impedance match.

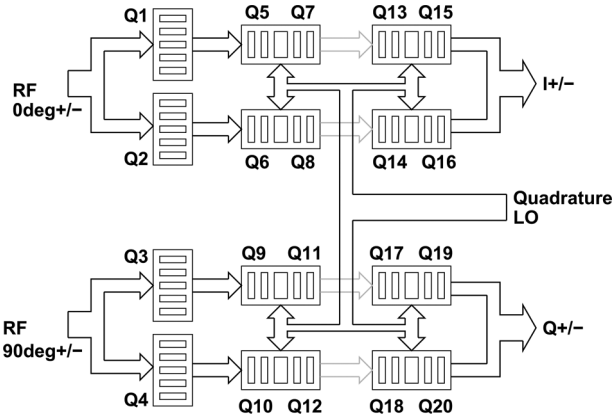


Fig. 19. Layout arrangement of the subharmonic receiver I/Q mixer core.

D. Subharmonic Mixer Core

The layout of the subharmonic I/Q mixer is carefully designed to minimize the parasitic capacitances between overlapped metal layers. An example of the receiver mixer is illustrated in Fig. 19. The I/Q mixer consists of two identical cores. Each one includes a differential pair Q1–Q2 and two stacked switching quads Q5–Q8 and Q13–Q16. The $BECEB$ cells with dual NPN transistors and shared collector are used to shrink the size of the quad and reduce the Miller capacitance. The quadrature LO signals are injected into the bases of the quads from the right. The quadrature RF signals input into the bases of Q1–Q4 from the left, and the I/Q signals output from the collectors of Q13–Q20. When the core is used in the up-conversion mixer, the RF and I/Q ports are swapped. This layout arrangement requires only two metal layers for the interconnections. The parasitic capacitance due to the overlapped metal area is minimized.

E. Baluns and Shielded Pads

A 160-GHz integrated input balun is needed at the RF input port for characterization of the receiver in a single-ended wafer-probing environment since a fully differential circuit architecture is used. In addition, an 80-GHz LO balun is needed for the characterization of the standalone VCO and mixer breakouts. A 160-GHz Marchand balun has been implemented from a 500-μm-long center-tapped balanced transmission line designed with 2.4-μm conductor width and spacing in the M4 top thick metal layer. The unbalanced input port of the balun is connected to a signal pad, which is shielded from the substrate by a grounded M1/M2 mesh metallization. A short-circuit transmission-line stub connected to the pad is used to provide inductive shunt compensation [17] of the pad capacitance. The combination of the balun and the capacitance-compensated pad has been measured using manufactured back-to-back test structures. The characterization results show an insertion loss of between 1.6 to 2.1 dB over the 150–170-GHz frequency range.

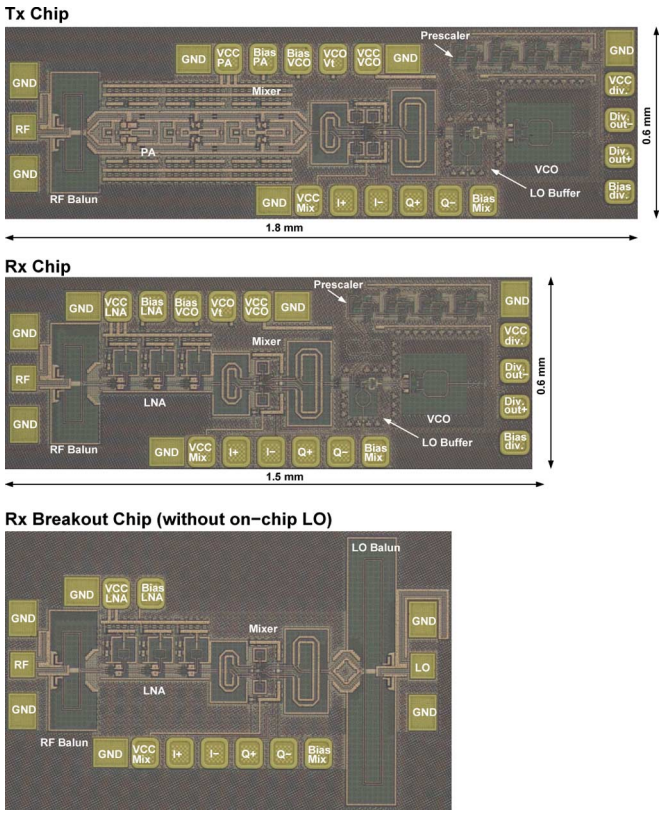


Fig. 20. Micrograph of the integrated transmitter and receiver chip including the auxiliary RF-input balun.

F. Manufactured Transmitter and Receiver

Fig. 20 shows the micrographs of the manufactured transmitter and receiver, occupying 1.8×0.6 and 1.5×0.6 mm^2, respectively. A large part of the die is occupied by the pad frame and the RF input balun, whereas the transmitter and receiver cores only require an area of 0.45 and 0.4 mm^2. The total chipset area saving compared to our previous publication [6] is about 64%. A version of the receiver without the integrated VCO was also manufactured together with breakouts of the VCO and the three-stage LNA.

V. Experimental Results

A. Three-Stage LNA

The measured S-parameters of the three-stage differential LNA breakout are shown in Fig. 21 together with the simulated $S21$ of the amplifier. The results include the total 3-dB losses of the integrated input and output baluns used for characterization purposes. Good agreement between simulated and measured gain is obtained from 140 to 160 GHz. The lower measured gain of 26 dB at the 156-GHz gain peak, compared to the 32-dB simulated value, is caused by compression of the amplifiers during the S-parameter measurement. The deviation from the targeted 160-GHz center frequency can be explained by parasitic metal to substrate capacitance $C_{p,c} = 2.2$ fF (see Fig. 5) present at the collector nodes of the stages not included in the simulation during the original design phase. In the presented simulation results, the correct capacitance has been extracted and added at these nodes.

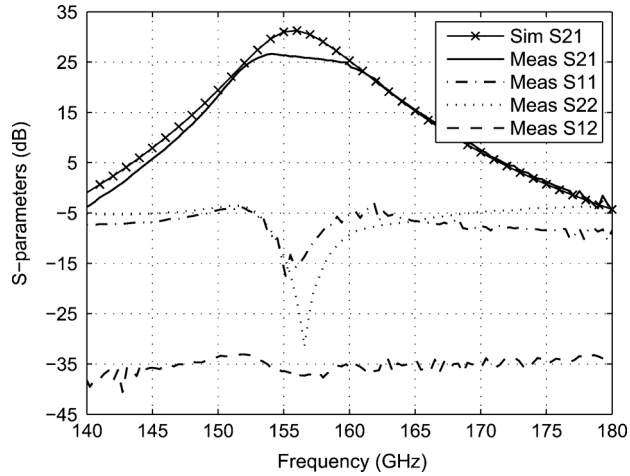


Fig. 21. Measured (solid line) and post-layout simulated (dashed line) small-signal gain of the differential three-stage LNA equipped with input and output baluns.

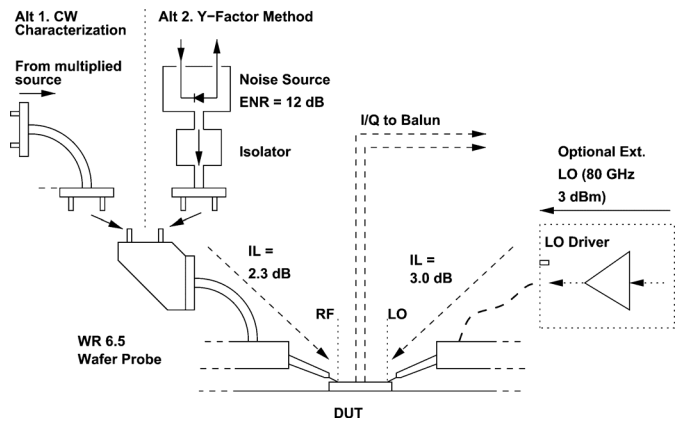


Fig. 22. NF and conversion gain measurement setup including an optional external 80-GHz LO.

The LNA NF was unable to be measured separately due to the lack of an off-chip mixer module. Alternatively, the system NF will be presented as follows.

B. Receiver Characterization

The integrated receiver has been characterized for conversion gain, NF, input compression point, and I/Q balance. For the conversion gain and NF measurements, the Y-factor method was used, whereas compression and I/Q balance measurements have been performed with a frequency-multiplier-based continuous wave (CW) source.

The measurement setup, including an optional external LO feed, is depicted in Fig. 22.

The conversion gain and NF measurements based on the Y-factor method are shown in Fig. 23 together with simulation results. In this measurement, the bias current of the VCO buffer was adjusted in order to optimize the LO drive power for maximum conversion gain and Y-factor. A commercial noise source (ElVA-1) covering from 110 to 170 GHz with a calibrated excess noise ratio (ENR) of 12 ± 2 dB was used in Y-factor measurement. The estimated 1.6–2.1-dB insertion loss

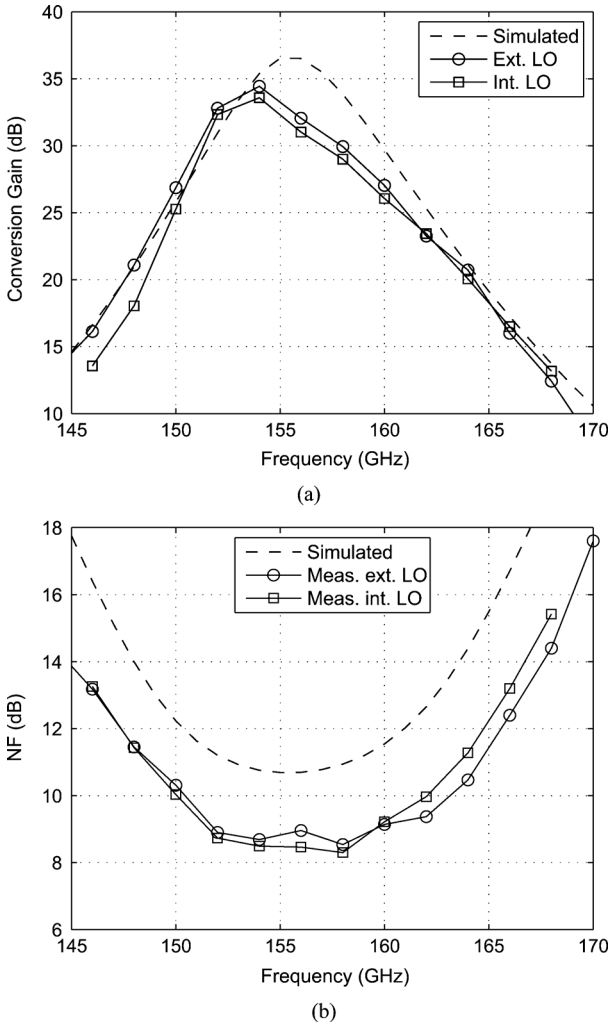


Fig. 23. Measured: (a) conversion gain and (b) system NF, 200-MHz IF of the full receiver with internally generated LO (squares) and the LNA/mixer breakout fed with an external 3-dBm 73–85-GHz LO signal (circles). The 1.6–2.1-dB losses of the integrated auxiliary RF balun and pad have not been de-embedded.

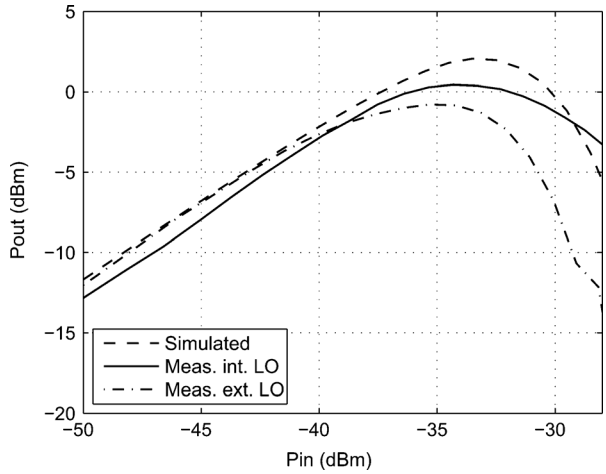


Fig. 24. Simulated (dashed line) and measured (int. LO solid line, ext. LO dashed–dotted line) 200-MHz IF output power of the receiver with a 156-GHz RF input power swept.

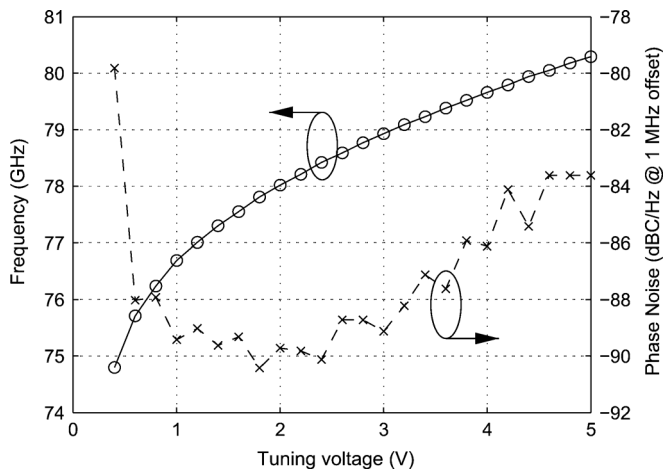


Fig. 25. Tuning characteristic (solid line) and phase noise (dashed line) of the 80-GHz VCO recalculated from the measured 1/16 divider output.

of the RF-input balun has not been de-embedded from the presented results. The 2.3-dB insertion loss of the WR-6.5 wafer probe has been calibrated out of the measurement. A maximum conversion gain of 35 dB and a minimum NF of 8.5 dB is obtained at the 156-GHz center frequency of the LNA. Similar results are obtained for the receiver with an integrated VCO as compared to the breakout circuit fed by an externally generated LO. The higher simulated NF of 11 dB can be explained by limitations of the high-frequency noise modeling capabilities of the Gummel–Poon model, which assumes noncorrelated shot noise in the base and collector currents [18]–[20]. In addition, a conservative estimation of the base-sheet resistance is used in the device model.

The combined I/Q power of receivers with and without an internally generated LO is presented in Fig. 24 for a 200-MHz IF and a sweep of the input RF power. The receiver shows −35-dBm input-referred CP1 dB with a saturated IF output power of 0 dBm. Above this input power level, the voltage swing at the collector nodes of the upper quads Q13-Q20 (see Fig. 6) saturates, thus causing a shift of the operating points of the mixer quads and the phase relationships of signals in the subharmonic mixer. Hence, a drop of the output power above the compression point is seen. This behavior has also been noticed for a similar type of subharmonic mixer in [9]. Increased voltage headroom at the collector nodes of the upper quads in the mixer or a modified load network can delay the onset of compression.

With a 100-MHz IF, the measured I/Q unbalance is better than 5° and the amplitude error is 1 dB. These errors are mainly caused by inaccurate I/Q splitting in the RF 90° coupler and could be minimized by a further optimized coupler design. A maximum dc offset of 5 mV was measured at the differential I and Q outputs. The small dc offset shows that the used subharmonic downmixing scheme efficiently minimizes the problems of self mixing.

The total power consumption of the receiver amounts to 490 mW, where the LNA and downconverter consume 240 mW from a 4-V supply, whereas the VCO and buffer require 40 mW from a 2.2-V supply, and prescaler dissipates 210 mW from a nominal 3-V supply. A redesign of the bias networks could allow single-supply operation and a reduced power consumption.

TABLE I
COMPARISON OF MONOLITHICALLY INTEGRATED TRANSMITTERS AND RECEIVERS ABOVE 125 GHz

3Technology [μm]	Integration Level [circuit blocks]	BW[1]/Freq. [GHz]	Phase noise [dBc@1MHz]	Ext. LO [GHz]	Conv. Gain [dB]	NF [dB]	Tx Pout [dBm]	Ref.
III/V-based								
0.1-μm mHEMT	PA, LNA, Mixer, LO-chain	212-224	-	55	3.5	7.4	-6	[21]
Silicon-based								
0.13-μm SiGe HBT	PA, LNA, Mixer, Prescaler	115.2-123.9	-100	Int. VCO	13	11.5	3.6	[22]
0.13-μm SiGe HBT	LNA, Mixer	125-129	-96[1]	Int. VCO	25	11	-	[11]
65-nm CMOS	PA, LNA, Mixer	135-145	-90	Int. VCO	-15	-	2	[23]
65-nm CMOS	PA, LNA, Mixer, tripler	144	-85[2]	Int. VCO	48	12.5	10.1	[24]
0.13-μm SiGe HBT	PA, LNA, Mixer	160-175		Int. VCO	-5	21	-5	[4]
0.13-μm SiGe HBT	PA, LNA, IQ-Mixer, Prescaler	158-165	-80	18	25 / 27[3]	11 / 9[3]	5	[6]
0.25-μm SiGe HBT	LNA, Mixer	200-230	-	110	16/18[3]	15/13[3]	-	[25]
0.25-μm SiGe HBT	Mixer, LO-chain	313-328	-	17.7	-13/-9[3]	32/28[3]	-	[25]
0.25-μm SiGe HBT	PA, IQ-Mixer, Prescaler	150-168	-90[1]	Int. VCO	>29 / 30.5[3]	-	10.6	This Work
0.25-μm SiGe HBT	LNA, IQ-Mixer, Prescaler	150-162	-90[1]	Int. VCO	>24 / 25.5[3]	8.5 / 7[3]	-	This Work

[1]At the half operating frequency
[2]Injection locked.
[3]Excluding the losses of the auxiliary input balun.

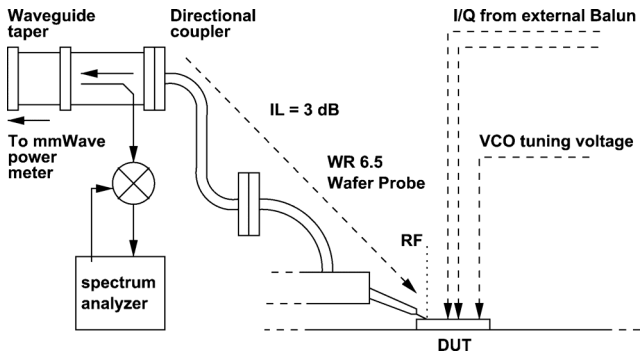
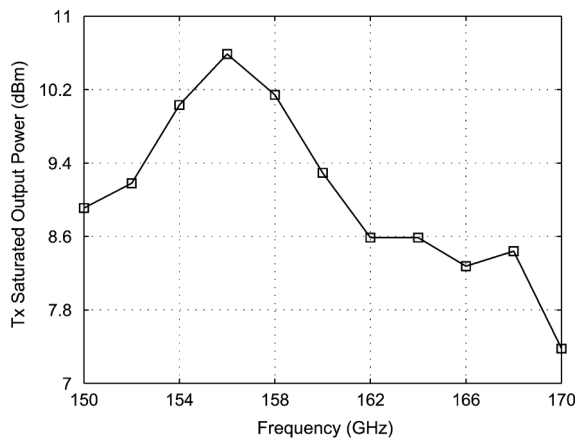
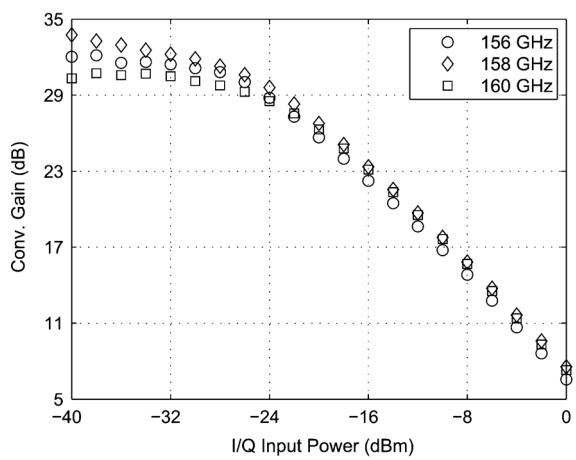


Fig. 26. Output power and conversion gain measurement setup.



(a)



(b)

Fig. 27. Transmitter characterization results. (a) Measured saturated output power. (b) Conversion gain at IF frequency of 60 MHz.

C. VCO Measurements

Fig. 25 depicts the tuning characteristic over most of the VCO frequency range with respect to the tuning voltage V_T. As V_T is tuned from 0.4 to 5.0 V, the divided frequency at the prescaler output varies from 4.765 to 5.026 GHz. Hence, the VCO frequency is from 76.2 to 80.4 GHz. The oscillating frequency and the phase noise of the VCO are calculated from the measured output signal of the 1/16 prescaler.

The phase noise of the 4.863-GHz prescaler output signal is -114.5 dBc/Hz at a 1-MHz offset. Hence, the phase noise of the VCO at 77.8 GHz is -90.5 dBc/Hz at a 1-MHz offset, for a $20\log(N)$ dB phase-noise improvement with a frequency-divided-by-N operation, where N is the frequency division number. As shown in Fig. 25, the best phase noise appears between 1.5–2.5-V tuning voltage where the capacitive ratio n [see (20)] is close to the optimized value.

D. Transmitter Characterization

The transmitter has been characterized for maximum output power and conversion gain. The measurement setup is depicted in Fig. 26.

A D-band waveguide probe and a WR-6.5 waveguide were used to pick up the RF signal. In order to observe the output spectrum of the transmitter, a D-band waveguide directional coupler and an OML M06HWD harmonic mixer were used to work with an Agilent E4440A spectrum analyzer. The RF power was simultaneously measured by a millimeter-wave power meter (Erickson PM4 with WR-10 waveguide interface) connected to the directional coupler through a WR-10–WR-6.5 waveguide taper.

The measured conversion gain and saturated output power are shown in Fig. 27. Across the 150–168-GHz band, the transmitter achieves a saturated output power above 8 dBm and maximum 10.6 dBm at 156 GHz with a -7-dBm IF input at 60 MHz, a

maximum conversion gain of 30–34 dB, and an output CP1 dB of -5 to 1 dBm.

For the output power measurement, the estimated 1.6–2.1-dB insertion loss of the on-chip RF-output balun has not been de-embedded from the presented results.

The transmitter consumes 610 mW totally, where the PA consumes 330 mW from a 3.3-V supply, and the upconverter takes 30 mW from a 4-V supply.

VI. Summary and Conclusion

A 160-GHz monolithic integrated transmitter and receiver chipset has been demonstrated in an engineering version of a 0.25-μm SiGe HBT technology. The use of cascaded up-/down-conversion mixers and compact 90° hybrids enable a direct quadrature up-/down-conversion from a subharmonic LO signal, which was generated from an integrated 80-GHz low phase-noise VCO equipped with a prescaler for external locking. In addition, this paper features a theoretical study promoting a better understanding of why the maximum conversion gain is obtained by arranging LO signals in quadrature at lower frequencies, but in nonquadrature at frequencies close to $f_{\max}$. The study also shows the less variation of the conversion gain over LO phases at higher frequencies. As a result, the mixer has a higher tolerance on the phase error of the 90° hybrid design. Compared to similar transceivers shown in Table I, this chipset provides a low-system NF of 8.5/7 dB (with/without an aux. balun) and up to 10.6-dBm saturated output power combined with a limited dc power consumption and a high level of integration. Compared to our previous publication [6], the chipset area is reduced by 64% and the power consumption is saved by 67%. To the authors' knowledge, this study shows a record receiver NF and a record transmitter output power above 125 GHz in SiGe technology. The conversion gain and output power can be traded for a wider bandwidth and higher input compression point by a re-optimization of the LNA, mixer, and PA. Hence, the presented chipset can be adapted to a number of different D-band imaging, radar, and communication applications.

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