A Fully Integrated 16-Element Phased-Array Transmitter in SiGe BiCMOS for 60-GHz Communications

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***Abstract*—A phased-array transmitter (TX) for multi-Gb/s non-line-of-sight links in the four frequency channels of the IEEE 802.15.3c standard (58.32 to 64.8 GHz) is fully integrated in a 0.12-μm SiGe BiCMOS process. It consists of an up-conversion core followed by a 1:16 power distribution tree, 16 phase-shifting front-ends, and a digital control unit. The TX core is a two-step sliding-IF up-conversion chain with frequency synthesizer that features 40 dB of gain programmability, I/Q balance and LO leakage correction, and a modulator for 802.15.3c common-mode signaling. The tradeoffs involved in the implementation of a 1:16 power distribution network are analyzed and a hybrid passive/active distribution tree architecture is introduced. Each of the 16 front-ends consists of a balanced passive phase shifter and a variable-gain, 3-stage PA that features $\mathrm{oP_{1dB}}$ programmability through the bias control of the its final stage. All of the chip features are digitally controllable and individual memory arrays are integrated at each front-end to enable fast beam steering through a high-speed parallel interface. The IC occupies 44 mm^2 and is fully characterized on wafer. The TX delivers 9 to 13.5 dBm $\mathrm{oP_{1dB}}$ per element at 60.48 GHz with a total power consumption of 3.8 to 6.2 W. Each element attains a phase-shift range $>360^\circ$ with an amplitude variation $<\pm 1$ dB across phase settings and adjacent elements. Measurement results from a packaged IC in an antenna chamber are also presented including the demonstration of spatial power combining up to +40 dBm EIRP and 16-element radiation patterns.**

***Index Terms*—60-GHz transmitter, 802153c, millimeter-wave, phased-array, SiGe BiCMOS.**

I. Introduction

THE 60-GHz frequency band features a very large bandwidth ($\sim$7 GHz worldwide) which enables multi-Gb/s short-range wireless communications [1]–[3]. The high carrier frequency, in the millimeter-wave (mmWave) regime, results in substantial path loss at a given range and increased shadowing, making non-line-of-sight (NLOS) communications challenging. Steerable, high-gain antennas are an option to overcome these limitations, and phased arrays are an excellent way to implement them. Phased arrays enable steerable directivity and, when compared with a single-element transceiver with a low-gain antenna, provide higher effective isotropic radiated power (EIRP) for the transmitter, and higher signal-to-noise ratio (SNR) for the receiver [4], [5]. mmWave silicon-based phased arrays have lately been a topic of considerable interest [6]–[11]. Silicon mmWave phased-array transmitters (TX) have been demonstrated with LO phase shifting [6], [8], IF phase shifting [9], and bidirectional [10] or unidirectional [7], [11] *RF* phase-shifting. Of these topologies, the RF phase-shifting and combining architecture results in the lowest area, lowest power consumption implementation, as the minimum number of redundant components is required. A key challenge associated with the all-RF topology is realizing high-performance RF phase shifters and compact, low-loss RF distribution networks.

This work presents a fully integrated phased-array TX which supports multi-Gb/s NLOS 60-GHz links, compliant with the IEEE 802.15.3c standard [12]. A novel RF distribution network is presented, along with high-performance, digitally controllable RF phase-shifting front-ends. In addition to beam-steering, the IC has the following major features: an on-chip power sensor at each element; three temperature sensors; LO leakage and I/Q phase and amplitude adjustment circuitry; front-end $\mathrm{oP_{1dB}}$ programmability; and an integrated modulator for $\pi/2$-BPSK/MSK signaling (common transmission mode in the IEEE 802.15.3c standard [12]).

In Section II, system-level design considerations are discussed and the overall TX architecture is presented. Section III presents the TX core and its frequency synthesis planning. The circuit-level design of the power distribution tree and the phase-shifting front-end are presented in Sections IV and V, respectively. The results from comprehensive measurements performed on-wafer are presented in Sections VI and VII discusses experimental results from a packaged IC evaluated in an antenna chamber. Finally, Section VIII summarizes the results and presents a comparison with the current state-of-the-art in phased arrays.

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II. Transmitter Architecture and System-Level Design Considerations

A. Phased-Array Transmitter Requirements for 60-GHz NLOS Communications

The quality of service (QoS) and throughput (2–6 Gb/s) required by current and future 60-GHz applications (video streaming, gaming, office networking) demand high link-margin, especially considering that the implementation of strong error-correction codes at Gb/s data-rates is challenging even in a contemporary CMOS process [13]. Moreover, for 60-GHz NLOS communications, reflection loss on the order of 10–20 dB can be expected in typical indoor environments [14] and the total NLOS path length is hard to predict *a priori*. For these reasons , robust system operation requires as much TX output power as allowable.

The United States Federal Communication Commissions (FCC) rules for communications in the 57–66-GHz band-limit emissions from the radiating source to an average power density of 9 μW/cm^2 and a maximum power density of 18 μW/cm^2, both measured at 3 meters [15]. These values correspond to an average and maximum EIRP of 40 and 43 dBm, respectively. Typical differential or single-ended PAs in SiGe deliver an output power at 1-dB compression $(\mathrm{oP_{1dB}})$ on the order of 11-15 dBm [16]–[18]. To attain a 40-dBm EIRP with these typical silicon PAs, the TX would require a very high-gain antenna $(>25\ \mathrm{dB})$ which in turn results in narrow beamwidths. Alternatively, higher output power PAs $(>20\ \mathrm{dBm})$ could be designed employing on-chip power combining; however, these structures consume considerable chip area, their on-chip output power combiners are lossy, and they will still require larger antenna apertures to achieve 40-dBm EIRP. In contrast to these, a phased-array TX enables spatial power combining, and offers paths to meeting EIRP targets with multiple elements while also providing mechanisms to steer narrow beams or synthesize wider beams.

The EIRP from a phased-array TX (TX_{EIRP}) with *N* elements is given by [4]

$$TX_{EIRP} = P_{NE} \cdot (N \cdot G_A)\,[\mathrm{W}] \tag{1}$$

where P_{NE} is the total power generated by the TX, and G_A is the gain of each antenna in the direction of radiation. As a function of the output power from each element in the array (P_{1E}), TX_{EIRP} can be expressed as

$$TX_{EIRP} = (N \cdot P_{1E}) \cdot (N \cdot G_A)\,[\mathrm{W}]. \tag{2}$$

To calculate TX_{EIRP} in dBm, (2) can be rewritten as[1]

$$TX_{EIRP} = P_{1E} + G_A + 20 \cdot \log(N)\,[\mathrm{dBm}]. \tag{3}$$

In this case, P_{1E} is the output power from each element in dBm and G_A is the antenna gain in dBi. Fig. 1 illustrates the tradeoff between the number of elements in the array and the required output power from each element to attain example levels of EIRP (28, 34, 40, and 46 dBm), assuming an elemental antenna gain of 4 dBi. For a fixed EIRP, as the number of elements is increased (i.e., the antenna aperture is increased), the single-element output power (P_{1E}) decreases by a factor of N^2, the required total chip output power (P_{NE}) decreases by a factor of N, and the total DC power consumption in the array, which is proportional to the total chip output power, decreases by a factor of N. These benefits are obtained at the cost of increased chip and package size, more complex power and signal distribution, and increased testing difficulty. Balancing these power/area/complexity considerations led to the optimum choice of 16 elements for the array, targeting 10-12 dBm single-element output power.

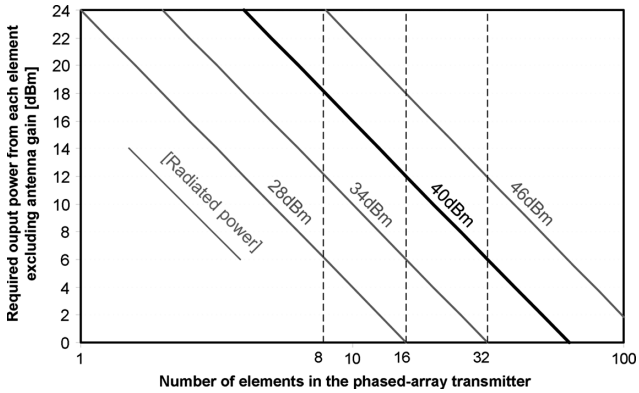


Fig. 1. Required output power from each element Vs. number of elements in a phased array TX to attain different EIRP levels. An antenna gain of 4 dBi is assumed.

B. Proposed Phased-Array TX Architecture

With these considerations in mind, the phased-array TX architecture depicted in Fig. 2 is implemented. All RF signal paths in the chip are differential. A double-conversion architecture with frequency tripler is selected, leveraging the architecture proven in [1]. The sliding-IF frequency in this architecture is 8.331–9.257 GHz, the RF center frequency is 58.32–64.8 GHz and the image is 41.657–46.286 GHz. Although LO-path and IF-path phased-array architectures are feasible at 60 GHz for a relatively small number of elements, an RF-path phase-shifting architecture is employed in this array since it offers clear advantages in terms of area and power consumption for a 16-element system. The loss penalty of employing an RF phase-shifter is compensated using gain in the power distribution tree and the front ends. In contrast to a single-element TX [1], this design includes several passive and active elements in the signal path between the final RF up-conversion mixer and the final output (including package and antenna), all of which have a bandpass response tuned at 60 GHz. Therefore, an explicit filter is not required for image rejection.

The digital core of the TX controls the bias, frequency tuning, calibration and gain settings for all the circuits in the array. Individual power-down controls are implemented at every element

[1]The N^2 or $20\log(N)$ factor is due to the use of single-element output power and antenna-gain variables. If the total output power (P_{NE}) is used instead, a $10\log(N)$ dependency in the EIRP equation is obtained due to the *N*-times increase in antenna aperture.

TABLE I
FREQUENCY PLANNING FOR THE TRANSMITTER CORE COMPLIANT WITH IEEE 802.15.3 C CHANNELIZATION

IEEE 802.15.3c Channel #	RF center freq. [GHz]	Sliding-IF freq. [GHz]	Freq. tripler output [GHz]	RF image freq. [GHz]	VCO freq. [GHz]
1	58.320	8.331	49.989	41.657	16.663
2	60.480	8.640	51.840	43.200	17.280
3	62.640	8.949	53.691	44.743	17.897
4	64.80	9.257	55.543	46.286	18.514

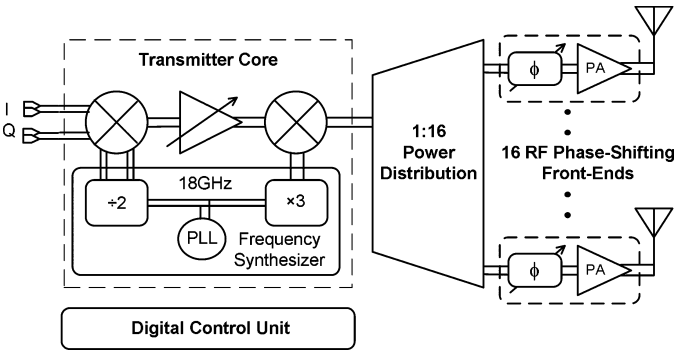


Fig. 2. 16-element phased-array transmitter architecture.

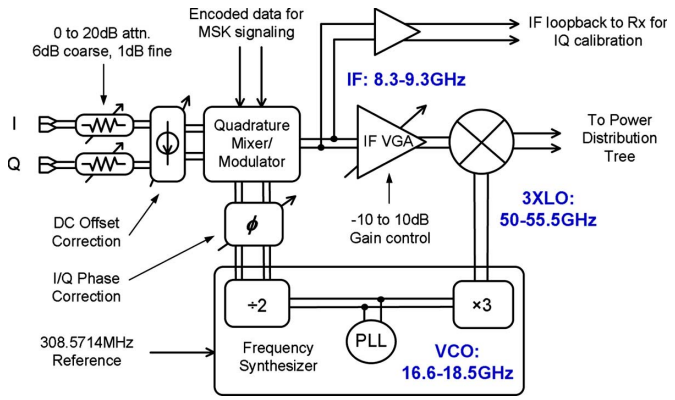


Fig. 3. Superheterodyne transmitter core with sliding-IF frequency.

so that the array can be operated with any number of elements (1–16) at reduced power consumption. The digital core also reads the output from three temperature sensors and 16 output power sensors (one for each element). The TX supports a maximum conversion gain of 35 dB to each element with 40 dB programmability. The design of the core, distribution tree and front-ends are described in detail in the next sections.

III. TRANSMITTER CORE AND FREQUENCY SYNTHESIZER

A detailed block diagram of the transmitter core section is shown in Fig. 3. The up-conversion chain follows the sliding-IF superheterodyne architecture presented in [1]; however, the present implementation is tuned to support the four frequency channels of the 802.15.3c standard. A detailed frequency plan is presented in Table I, describing the frequencies present in different sections of the core for each channel.

A passive baseband attenuator is the first block in the chain. It is programmable in steps of 6 dB for both I and Q branches simultaneously, and in steps of 1 dB independently in each branch for I/Q amplitude calibration. A DC offset correction mechanism is implemented at the output of the attenuator through DC current sources to ensure carrier leakage suppression. A quadrature mixer performs the first up-conversion to an IF frequency of $\sim$9 GHz and is followed by an IF-VGA with 20 dB of programmable gain in steps of 1 dB. A buffer is inserted after the first up-conversion to enable an IF loop-back connection with a receiver for I/Q calibration purposes. The cascaded frequency response of the I/Q mixer and IF-VGA forms a fourth-order bandpass characteristic which is digitally controllable to accommodate the sliding-IF frequency characteristics. At the end of the up-conversion chain, an RF mixer is driven by the 3 XLO and delivers the desired output signal to the distribution tree.

The I/Q mixer can also be employed as a direct MSK modulator for common-mode 802.15.3c signaling. The design details of this composite mixer-modulator are described in [19], including measurement results of its operation at 2 Gb/s.

In contrast to the synthesizers reported in [20], where the channels span from 56.5 to 64.0 GHz with 0.5 GHz spacing, the new IEEE 802.15.3c channel spacing and the corresponding VCO frequencies are listed in Table I. If a reference signal of 308.5714 MHz instead of 285.7143 MHz is used, the divider ratios of 54, 56, 58, and 60, would support the required frequencies. After verifying that the 308.5714 MHz crystal oscillator had phase noise performance (-125 dBc/Hz at 100 kHz, -142 dBc/Hz at 1 MHz) equal to or better than its counterpart at 285.7143 MHz, the sub-integer N synthesizer reported in [20] was used for this chipset. Details on the design of the frequency plan are also provided in [20]. The phase-noise performance target for this synthesizer design is ~ -90 dBc/Hz @ 1 MHz offset for the 3 X LO frequency. The impact of LO phase noise on the performance of mmWave communication systems is presented in [21], [22]. In particular, the study on the performance of different transmission modes in the 802.15.3c standard reported in [22] concludes that the phase noise does not significantly degrade the performance of either SC-FDE or OFDM when it is not higher than -87 dBc/Hz@1 MHz.

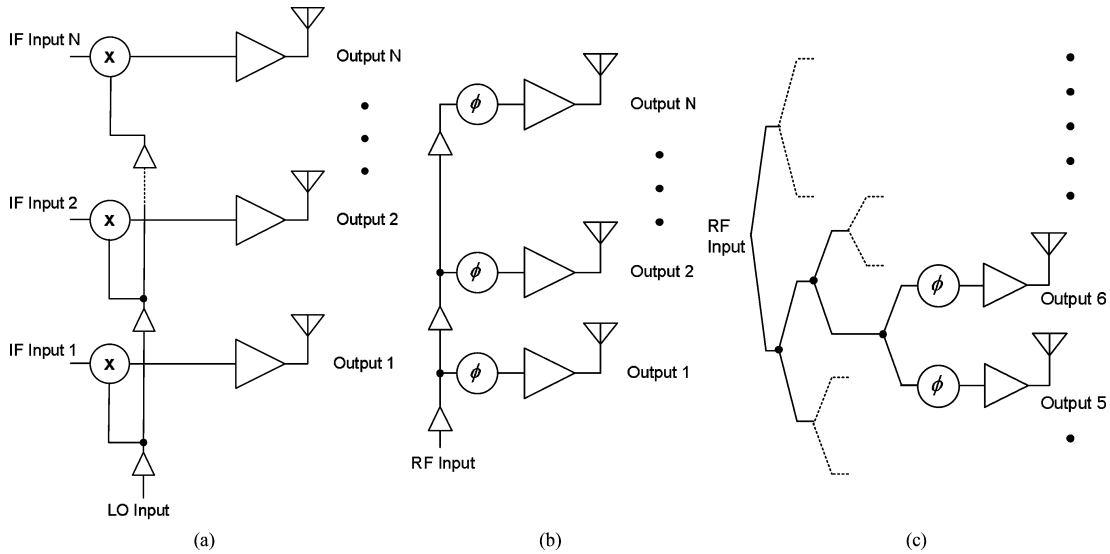


Fig. 4. General power distribution options. (a) LO series distribution in a MIMO TX. (b) RF series distribution in a phased-array TX. (c) Corporate feed architecture.

IV. Power Distribution Tree

A. Power Distribution Architecture

The distribution of signal power from a single RF mixer to 16 front-ends is difficult, especially when considering simultaneous constraints on power dissipation, linearity, area, and bandwidth. Fig. 4(a) shows an LO signal distribution topology that is suitable for RF MIMO systems. This series distribution approach has also been used in a 60-GHz phased array front-end with RF phase shifting [23] as illustrated in Fig. 4(b). This architecture minimizes the signal-routing area but the gain and $\mathrm{oP_{1dB}}$ degrade as the signal propagates towards the front-ends far away from the input. Fig. 4(c) shows the corporate distribution architecture, which requires more routing but which ensures signal amplitude and phase uniformity among all front-ends. In principle, each power division by two can be done passively, as with a Wilkinson power divider [24]. Nevertheless, as the size of the array grows, the signal amplitude degrades rapidly.

Fig. 5 illustrates how the gain and $\mathrm{oP_{1dB}}$ along a single distribution path degrade as the number of passive dividers increases in a corporate architecture. Note that in addition to the natural 3-dB power reduction at each 1:2 power divider, an extra 1 dB of loss is added to account for splitter loss and signal routing. Using an all-passive approach it is difficult to deliver the required $\mathrm{oP_{1dB}}$. In contrast, a corporate distribution network with active-only power splitting stages [25] could meet gain and $\mathrm{oP_{1dB}}$ requirements more easily. However the all-active approach makes the system bandwidth specifications harder to meet due to the cascading of active stages; furthermore, the power consumption of this approach is relatively high since at least 16 active units are required for a 16-way distribution.

The proposed power distribution architecture for the 16-element array is illustrated in Fig. 6; it is a hybrid solution combining both passive and active stages. It employs only five amplifiers in total and each path contains only two cascaded active

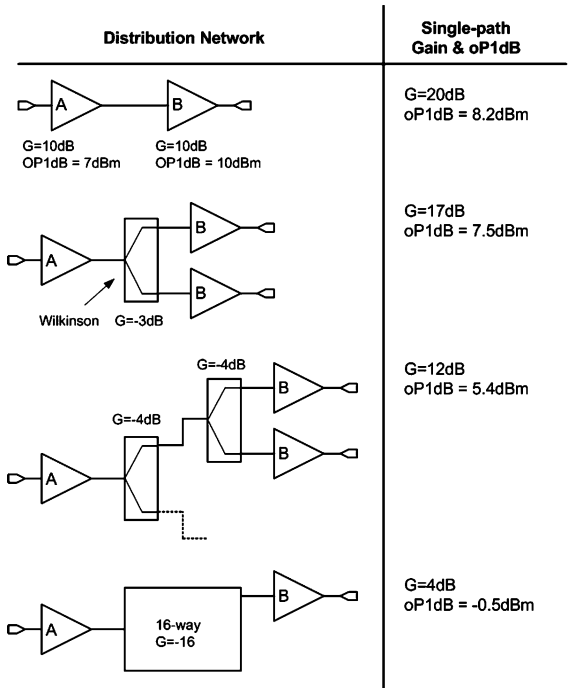


Fig. 5. Degradation of single-path gain and compression as a corporate distribution architecture grows from 2 to 16 element.

stages. Employing a smaller number of active stages (e.g., replacing the first distribution amplifier by a passive splitter) results in a smaller $\mathrm{oP_{1dB}}$ at each output of the tree. If the $\mathrm{oP_{1dB}}$ at the output of the array is to be maintained in this case, the loss of dynamic range in the tree must be compensated by a higher power gain at each front-end, which in turn demands an overall higher power consumption. Placing active and passive stages at alternate positions not only helps to maintain the overall linearity but also allows a progressive separation of the distribution outputs at their required distance.

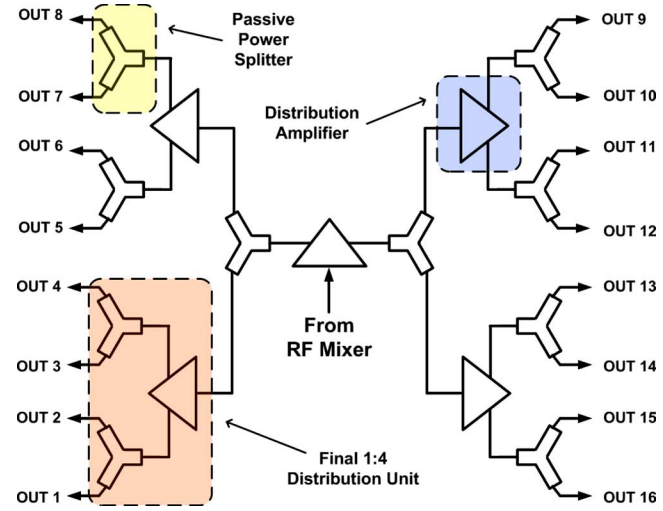


Fig. 6. Block diagram of the implemented 1:16 power distribution tree.

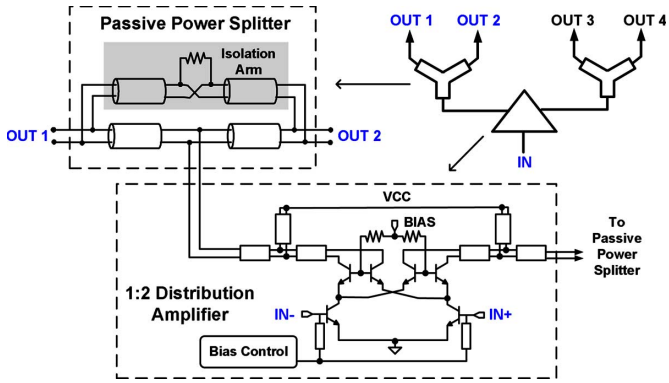


Fig. 7. Circuit-level implementation of each 1–4 distribution unit.

A final consideration for the power distribution implementation is the isolation between output branches at each 1:2 splitting stage. Ideally, if all the elements in the array are well matched, isolation is not necessary since the signals are split in-phase. However, in this first pass design, isolation between output branches was procured throughout the distribution tree to prevent cross-coupling (and hence undesired phase-shit alterations) between elements in two scenarios. 1) In a power-saving mode, where only a fraction of the elements are on, the elements (or group of elements) that are off may provide different load or become reflective. 2) Although the phase shifter is designed to be well-match, variations in its input impedance occur for different phase settings and reflections could occur at a given frequency across the 60-GHz band.

B. Power Distribution Implementation

The circuit-level implementation of each 1:4 distribution unit is shown in Fig. 7. All 1:4 distribution blocks are identical in design, although the first of them has a modified layout to accommodate its unique signal routing requirements. Each 1:4 power distribution unit occupies an area of 0.8 mm^2, and draws 12 mA from a 2.6-V supply.

The distribution amplifier circuit consists of an input differential pair followed by two parallel cascode stages that split the RF current into two independent paths. A similar active power splitter configuration was employed in the 40–45 GHz phased array transmitter presented in [7]. Common-mode stability and common-mode rejection are ensured in this design by placing resistors ($\sim 180\ \Omega$) at the base of the cascode stages.

The passive power splitter uses a modified Gysel structure [26]. The splitter achieves isolation between its outputs by introducing a cross-coupled transmission line between them. This eliminates the requirement of having co-located outputs connected to a resistor as in a differential Wilkinson divider. Effectively, the routing length is absorbed by the splitter structure. Moreover, this design reduces the required transmission-line length required for the isolation arm in a conventional Gysel divider [27]. With respect to a Wilkinson-based passive distribution tree in a 4-element 60-GHz beamformer fabricated in the same technology [28], it is estimated that for each 1:2 splitting level the proposed structure reduces the implementation and routing loss by about 1 dB and the area by about 30%.

V. Phase-Shifting RF Front-End

A. Design Considerations and Circuit-Level Implementation

Each phased-array element consists of a balanced phase shifter, a differential, variable-gain, three-stage amplifier chain, a digital memory array (beam table), and a power sensor that delivers a DC current proportional to the PA output power. The overall block diagram and circuit schematics are shown in Fig. 8(a)–(d), respectively. The back-end of the line in the employed process (IBM SiGe 8 HP) has three copper layers (M1, M2, MQ) and two thick aluminum layers (LY, AM) for low loss RF interconnects. All of the employed transmission lines in the front-end are side-shielded microstrips implemented with AM for the conductor line and side shields, and MQ as a groundplane. This configuration allows the placement of the digital and DC bias circuitry (wired using M1 and M2) underneath the transmission lines.

The passive voltage-controlled phase shifter consists of two separate single-ended reflection-type phase shifters (RTPS) that share a common voltage DAC for digital phase-shift control, as shown in Fig. 8(c). The operation principle of an RTPS was introduced in [29]; this passive phase shifter topology was chosen since it provides adequate phase shift range with moderate loss and no penalty in power consumption or linearity. In this implementation, each single-ended RTPS consists of a Lange Coupler and tunable reflective loads, following the design presented in [30]. The overall balanced RTPS has been measured as a breakout and achieves differential phase shift range $>200^{\circ}$ from 58 GHz to 65 GHz with insertion loss varying from 5.5 dB to 9.5 dB.

To define the resolution in the phase shifter the main criteria is to ensure that the peak array gain variations are minimal (<1 dB) when the beam is steered in different directions. System-level calculations show that 3-bit phase resolution is

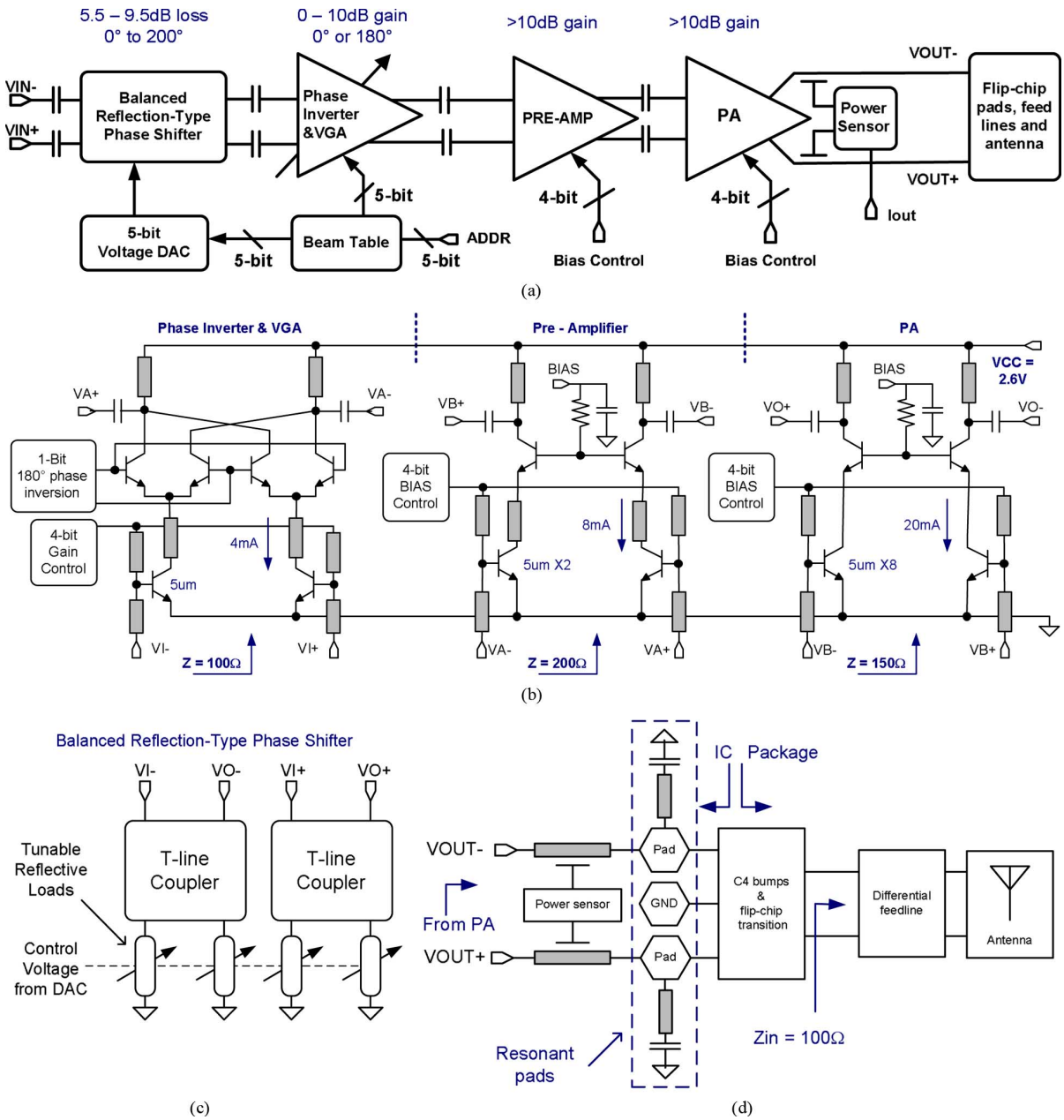


Fig. 8. Differential RF phase-shifting front-end. (a) Top-level block diagram showing passive and active elements, and digital control blocks. (b) Circuit schematics for the three-stage RF amplifier. (c) Block diagram of the balanced RTPS. (d) Block diagram of the output load, from the PA output to the antenna.

sufficient to fulfill this requirement. However, higher resolution (5-bit) was chosen in this implementation to compensate for potential DAC inaccuracies and to enable the reduction of side lobes and the formation of nulls in particular directions, when desired.

The RTPS is followed by a three-stage cascaded amplifier, in which the first two stages are driving amplifiers and the final stage is a power amplifier. All of the active stages operate from a 2.6-V supply. Phase inverting is required to extend the phase coverage of the RTPS to a full 360°. As shown in Fig. 8(b), the current-steering topology of the cascode stage in the first driving amplifier allows either 0° or 180° phase rotation controlled by switching the polarity of the base control nodes. Note that the required bit for phase inversion is additional to the 5 bits employed to control the passive phase shifter. To compensate the gain variation resulting from the changing phase settings in the RTPS, the first driving amplifier also provides gain tuning capability by controlling its bias current through a 4-bit DAC. The VGA bias current is varied within a range that maintains sufficient f_T for its input transistors. In this way, the gain adjustments have a minimal impact on the bandwidth of the front-end. A programmable gain range of 10 dB is obtained, which suffices to equalize output power variations due to the RTPS, frequency response, and mismatch between individual TX elements.

Both the final power-amplifier stage and the pre-amplifier follow a cascode topology with digital bias control, but employ scaled transistor sizes, bias currents, and output matching networks to optimize cascaded output compression. Through

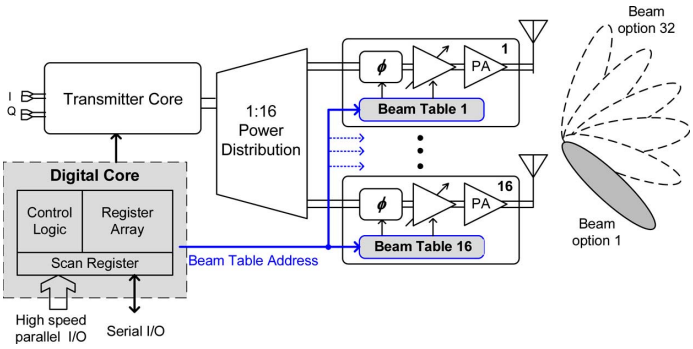


Fig. 9. Digital control architecture for fast beam-steering using local memory arrays at each element.

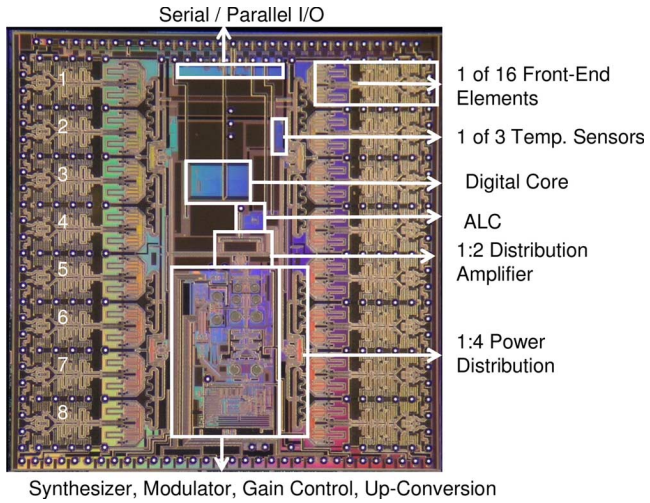


Fig. 10. Chip photo, 6.5 × 6.75 mm^2 die size.

proper choice of the inter-stage impedance (200 Ω between the first two stages and 150 Ω between the last two stages), the overall transmitter front-end circuit is capable of up to 15-dBm power delivery at 1-dB compression. Common-mode stability is ensured through the use of an *R-C* network at the biasing of the cascode devices, suppressing common-mode gain. An inductive transmission line between the transconductor and cascode devices of the driving stages also enhances gain and stability.

As illustrated in Fig. 8(d), the load network at the PA output consists of several passive elements from the IC to the antenna. The on-chip portion of the load features a power coupler/detector and short-stubs that resonate the signal pad capacitance; these components follow the design presented in [18]. The output pads follow a GSGSG configuration that shares the outer ground pads between adjacent elements in the array. Controlled Collapse Chip Connect (C4) bumps are employed for the flip-chip interconnects to the package which includes the antenna and its feedline. The impedance looking into the antenna feedline is 100 Ω in differential mode and close to an ideal open in common mode. The transition between the on-chip pads and the antenna feedline was designed using full-wave EM simulation. A distributed *RLC* model for this transition was created to facilitate co-simulation with the front-end. From EM simulations, the estimated insertion losses in the flip-chip transition and antenna feedline (∼8 mm in length) are 0.6 dB and 1.2 dB, respectively.

B. Digital Control Architecture for Fast Beam Steering

Maintaining link QoS over varying NLOS conditions (e.g., unexpected blocking of the transmitted signal by moving obstacles) demands prompt beam-direction switching. To change the beam direction requires an update of the phase-shift settings (and corresponding gain settings for amplitude equalization) of every element. This procedure will be unacceptably slow if executed through a serial interface. To address this issue, an independent local memory array (beam table) is integrated within each front-end and 32 different combinations of phase and gain can be preprogrammed in each memory. Each address in the memory stores information corresponding to a different beam direction. As shown in Fig. 9, the digital core unit in the array features a parallel digital I/O interface that directly communicates with the common memory address bus. To perform beam switching, all of the local beam tables are simultaneously pointed to the address that corresponds to the desired beam pattern. At any given time, fast switching (<50 ns) can occur among any of the 32 different preprogrammed directions, and, when desired, any subset of directions can be updated in the memory array through the serial or parallel interface. This infrastructure and approach allows the implementation of a progressive beam discovery algorithm that starts with relatively low-gain beams and moves towards highly directional beams as recommended in the 802.15.3c standard [12].

VI. On-Wafer Measurement Results

The phased-array TX IC integrates approximately 2200 NPNs, 320 000 FETs, and hundreds of transmission lines and is fabricated in the IBM 8 HP 0.12 μm SiGe BiCMOS process ($ft = 200$ GHz). Fig. 10 depicts the die photo illustrating the placement of the different system components. In addition to the full system, replicas of all the major building blocks were fabricated for independent testing and all of these ICs have been fully characterized on-wafer. Fig. 11 shows one of these ICs which includes two independent front-ends and a two-element front-end with a passive power splitter at the input.

A. RF Front-End Performance

The RF phase-shifting front-end was characterized as a breakout. Differential s-parameter measurements were performed using a 4-port VNA across all gain and phase settings and also at different temperatures and die locations. Some relevant examples these tests are presented. Fig. 12(a) shows the measured S_{21} and S_{11} for constant VGA settings across three different phase settings (10, 24, and 40) and Fig. 12(b) shows a comparison between measured and simulated results at maximum gain. Fig. 13 presents the measured phase variation across the 6 bits of phase control (128 different settings). A phase-shift range >360° is achieved in the four frequency channels of interest. Measurements on different die locations

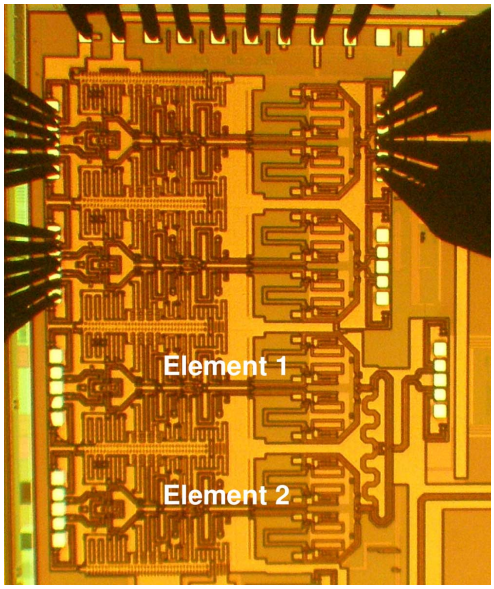


Fig. 11. Chip micrograph of IC with replicas of the front-end and a two-element front-end with power splitter.

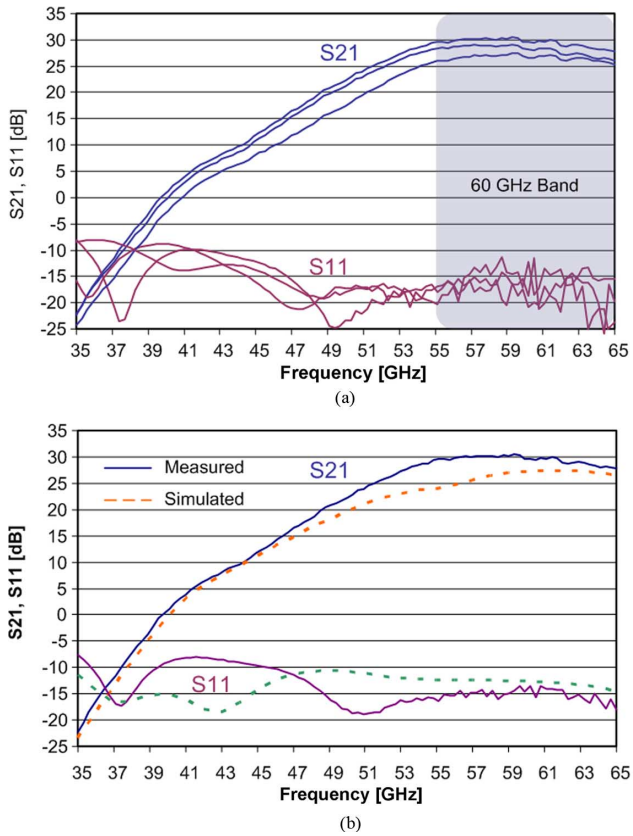


Fig. 12. Differential s-parameters for the RF phase-shifting front-end. (a) Measurement results at constant VGA settings for three different phase settings. (b) Comparison between measured and simulated results.

across a wafer indicate that the rms error in relative phase shift is less than 5°, which is expected due to the passive nature of the phase shifter.

Fig. 14 shows the measured S_{21} variation in the RF front-end across gain settings (4 bits) for four different frequency channels

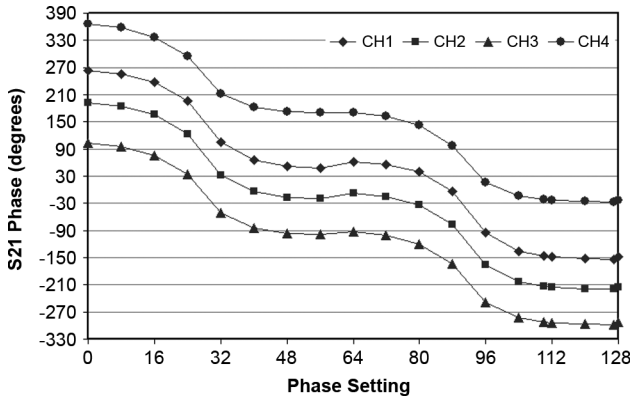


Fig. 13. Measured phase variation in the RF front-end across 128 settings (6 bits) for four different frequency channels.

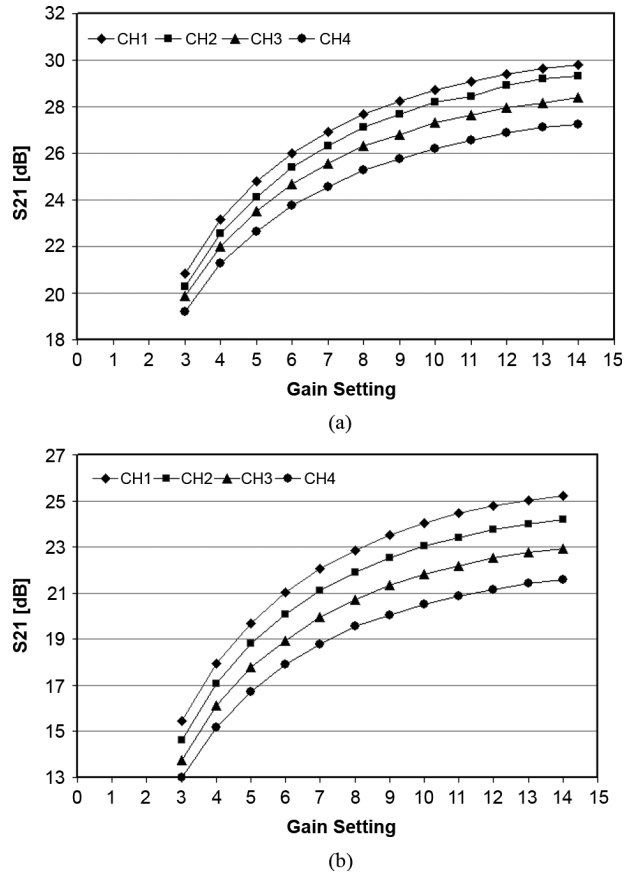


Fig. 14. Measured S_{21} variation in the RF front-end across gain settings (4 bits) for four different frequency channels at (a) 25 °C and (b) 85 °C.

at (a) 25 °C and (b) 85 °C. Note that while the absolute gain decreases by about 5 dB in channel 1 and 6 dB in channel 4 within this temperature range, the relative gain variation with respect to gain settings is practically invariant to temperature.

From the s-parameter measurements, a vector of VGA gain settings that compensates for the RTPS loss variation across the 128 phase settings is defined, and this vector is valid across temperature. Under equalized conditions, the front-end features a gain of 26 dB at 22 °C and 22 dB at 65 °C. In the range of 55-65 GHz and across all phase settings, the front-end has a

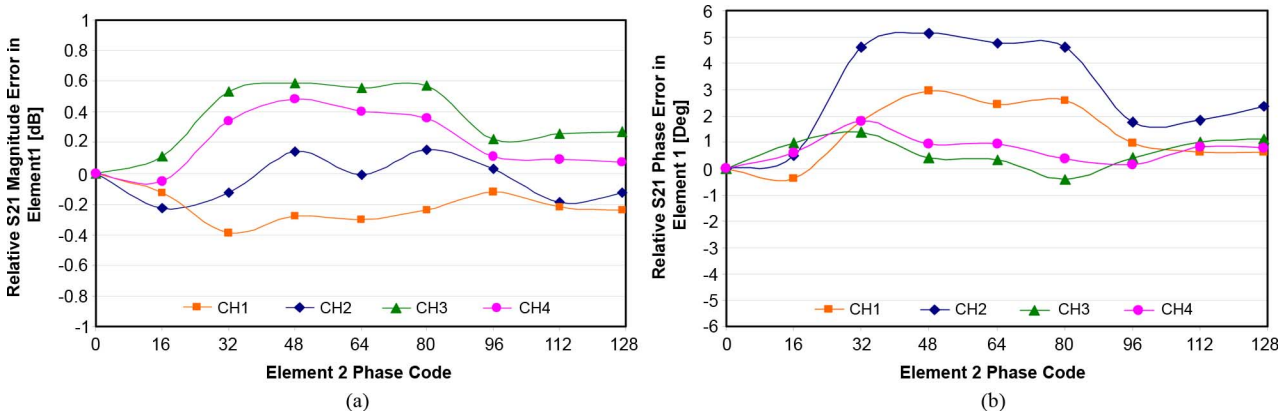


Fig. 15. Change in gain (a) and phase (b) of Element 1 due to coupling, as phase settings in Element 2 change. Measured through differential s-parameters on a two-element front-end breakout (Fig. 11).

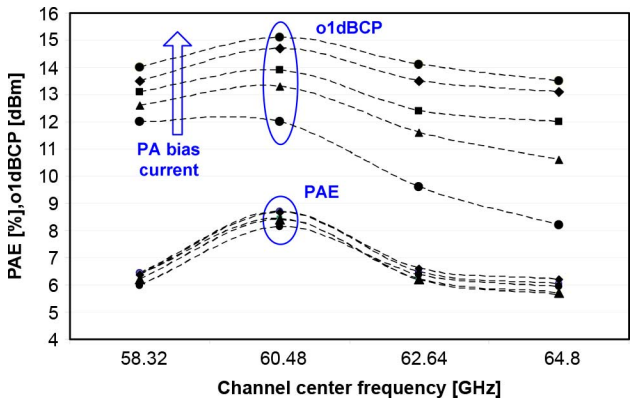


Fig. 16. Measured RF front-end o1 dBCP and peak PAE for different bias settings in the final PA stage.

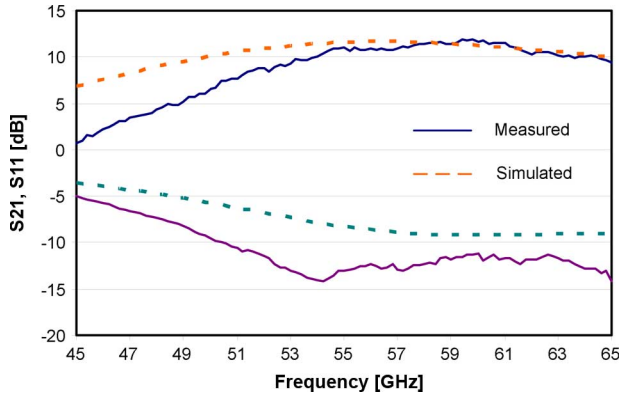


Fig. 17. Measured differential s-parameters for the distribution amplifier.

S_{21} variation <3 dB, $S_{11}<-10$ dB and common-mode rejection ratio (CMRR) $>$ 10 dB.

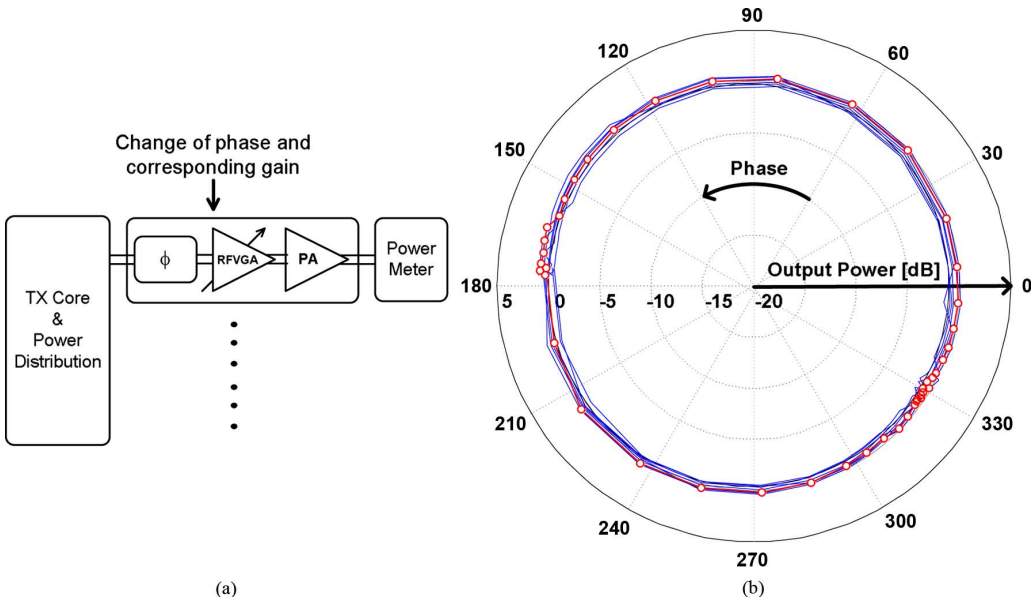
Coupling measurements between two adjacent elements are performed using the two-element replica IC shown in Fig. 11. The phase and gain settings of Element 1 are held constant and differential s-parameters (from the input of the common power splitter to the output of Element 1) are measured as the phase settings of Element 2 are varied. During the measurements, the output of Element 2 is also terminated by using an RF probe than contacts two elements simultaneously. The results of this experiment are shown in Fig. 15. Across the four frequency channels of interest, the gain and phase deviations in Element 1 due to coupling from Element 2 are less than 0.6 dB and 5°, respectively.

Differential large-signal measurements are also performed on a breakout of the RF front-end. With increasing bias current in the last stage PA, the front-end has a measured $\mathrm{oP_{1dB}}$ in channel 2 (60.48 GHz) that can vary from $+12$ dBm to $+15$ dBm with a nearly constant peak PAE of 8-9%. The large-signal measurement results for the four different frequency channels at ambient temperature are shown in Fig. 16.

The 1:2 active distribution amplifier employed in the distribution tree has also been measured as a breakout. Differential s-parameter results for this block are presented in Fig. 17 showing good agreement with simulations. A gain >9 dB (from input to each output port), CMRR >8 dB, and isolation between output ports >11 dB are obtained from 55 to 65 GHz.

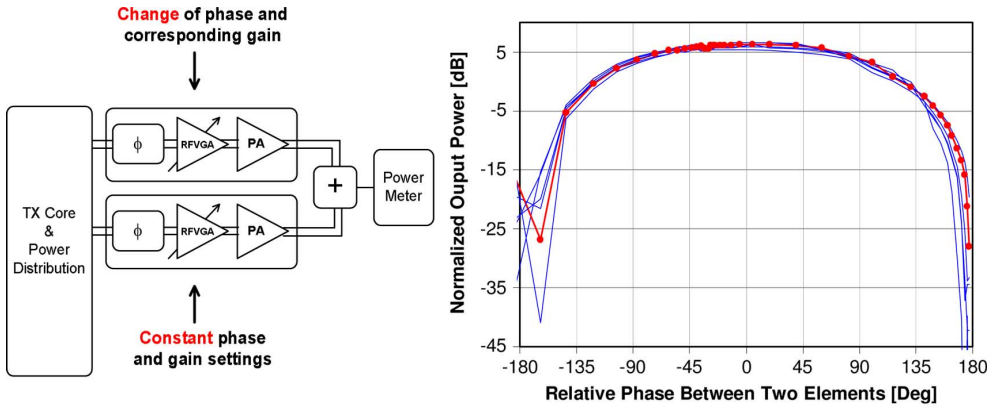
B. *Full TX IC Measurements*

The output power from an individual element was measured, for CW input, for different phase (and corresponding VGA gain) settings as described in Fig. 18(a). This experiment was repeated across seven adjacent elements. An identical vector of VGA settings was applied in all cases. The resulting polar plot in Fig. 18(b) indicates that the output power variation across 360° of phase and adjacent elements is less than ± 1 dB. Two adjacent elements were then probed simultaneously and their outputs were summed in an external output combiner according to the setup shown in Fig. 19(a). The phase of one element was swept 360° while keeping the other constant and the aggregated output power was measured. This procedure was repeated for seven different pair of elements on the right side of the IC and the results are shown in Fig. 19(b). The output power is normalized to the output power from a single element. In all cases the output signals combine with a peak-to-null ratio >25 dB across elements, confirming the desired phase resolution and matching between elements.



(a) (b)

Fig. 18. Single-path phase shifting measurements. (a) Simplified measurement setup. (b) Measured equalized output power over phase shifter settings for seven adjacent elements.



(a) (b)

Fig. 19. Two-element phase shifting measurements. (a) Simplified measurement setup. (b) Power-combined response with one element swept while the other is held constant.

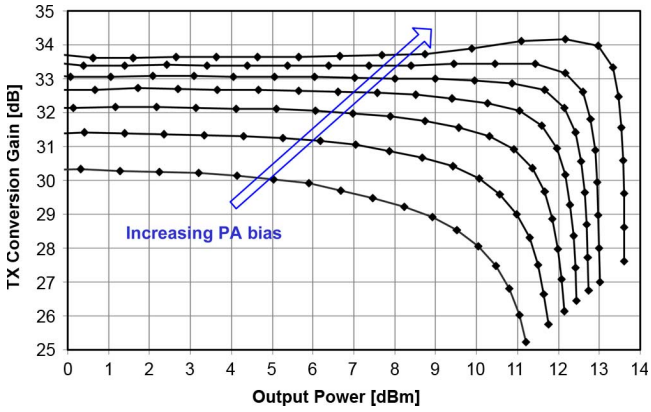


Fig. 20. Single-path TX compression curves at different bias setting in the final PA. For this measurement, through the IF VGA, the TX gain is set 5 dB below maximum.

The TX conversion gain from an individual element at 60.48 GHz (channel 2) was measured for different bias settings in the final PA stage of the measured element. The resultant compression curves are shown in Fig. 20, demonstrating the output power programmability of the TX. This experiment was repeated for each IEEE channel frequency at ambient temperature (22 °C) and at 65 °C. The results are summarized in Fig. 21. Under nominal bias conditions (60 mA per front-end, 3.8-W total power), the single-element $\mathrm{oP_{1dB}}$ in CH 2 is 9 dBm, corresponding to a 16-element total generated power of 21 dBm. With increased PA bias conditions (120 mA per front-end, 6.2-W total array power) the $\mathrm{oP_{1dB}}$ per element and total generated power increase to 13.5 dBm and 25.5 dBm, respectively. To the best of the authors' knowledge, this is the highest reported output power for a monolithic mmWave TX (single-output or phased-array) in silicon. The $\mathrm{oP_{1dB}}$ has a measured variation of ± 0.25 dB across different phase settings and adjacent elements. At constant bias settings, the measured $\mathrm{oP_{1dB}}$ varies across frequency channels. However, thanks to the output power programmability in the front-end, it is possible to attain a constant $\mathrm{oP_{1dB}}$ across all channels with different PA bias settings depending on the channel to be used. Fig. 22 shows the total TX power consumption required to deliver $\mathrm{oP_{1dB}} = 9.5$ dBm (corresponding to 21.5 dB total generated

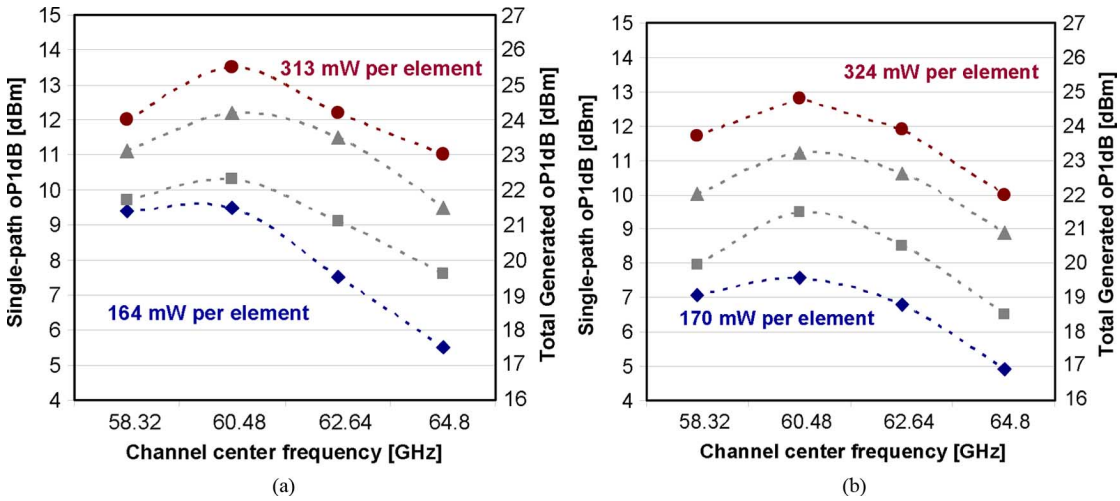


Fig. 21. Measured single-path $\mathrm{oP_{1dB}}$ across the four IEEE channels and for different PA bias conditions. (a) At 22 °C. (b) At 65 °C.

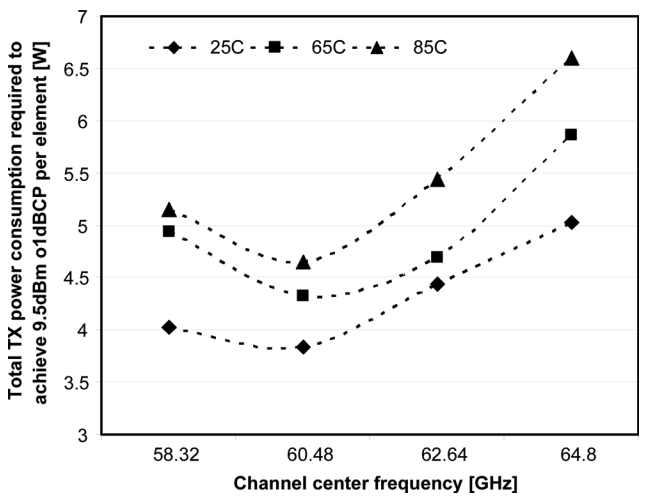


Fig. 22. Measured TX power consumption required to attain $\mathrm{oP_{1dB}}$ of 9.5 dBm per element at the four IEEE frequency channels and three different temperatures.

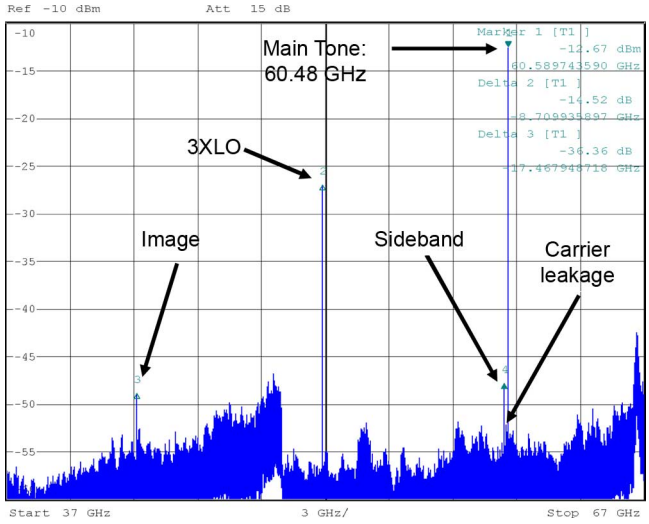


Fig. 23. Measured 30–67 GHz transmitter output spectrum.

power) at each element, for different frequency channels and at different temperatures.

Fig. 23 shows the full (30–67 GHz) output spectrum from the TX measured with a spectrum analyzer. High suppression ($>$ 35 dB) of side-band tones and carrier leakage was achieved. Full-chain TX operation was also evaluated by applying a 1.6-Gb/s OFDM signal (MCS2 transmit mode in 802.15.3c) to the IC using an external AWGN. As seen in Fig. 24, the resultant spectrum has low out-of-band spectral regrowth, meeting the output spectral mask requirements from the IEEE 802.15.3c standard. Table II summarizes the measurements performed on the TX phased-array IC by wafer probing. The TX performance was also evaluated at 65 °C to emulate a potential elevation in temperature when the chip is packaged. The observed increased power consumption at a higher temperature is due to the use of temperature-adaptive biasing in the front-ends. Note that the actual temperature of the packaged IC for a given application will depend on the ambient temperature and other factors (such as the design and attachment of a heat sink) that are beyond the scope of this work.

VII. Measurement Results From a Packaged TX IC

The TX IC has been packaged with 16 antennas in a 288-pin (28×28 mm^2) organic BGA package and placed on an evaluation board as shown in Fig. 25. The employed antennas are balanced-fed aperture-coupled patch designs and their differential input impedance is matched to 100 Ω. Measurement results for individual antenna elements show peak gain of 8 dBi, 10 dB return loss bandwidth $>$10 GHz and radiation efficiency $>$ 80% in the range of 57 to 66 GHz [31]. The package consists of 16 antenna elements arranged in a circular configuration, an open cavity for housing the flip-chip attached TX IC, and multiple interconnects operating at DC-60 GHz. The design and characterization details of this low-cost mmWave package design are beyond the scope of this work but they are provided in [32].

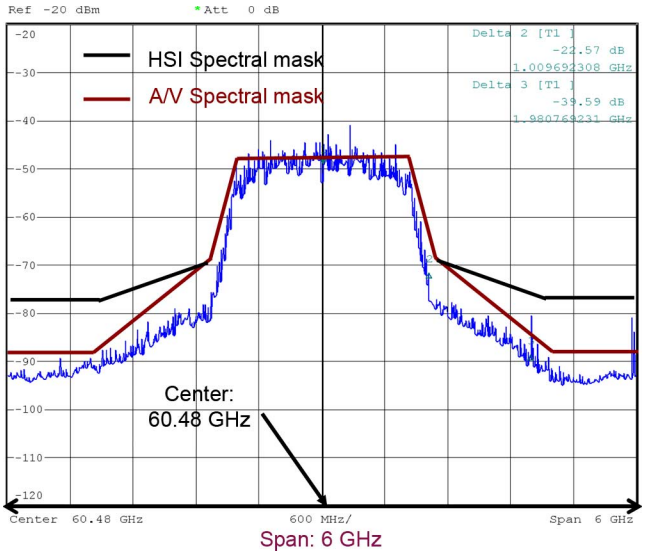


Fig. 24. Measured transmitter output spectrum in channel two (60.48 GHz) when applying a 1.6 Gb/s OFDM signal (MCS2 802.15.3c transmit mode).

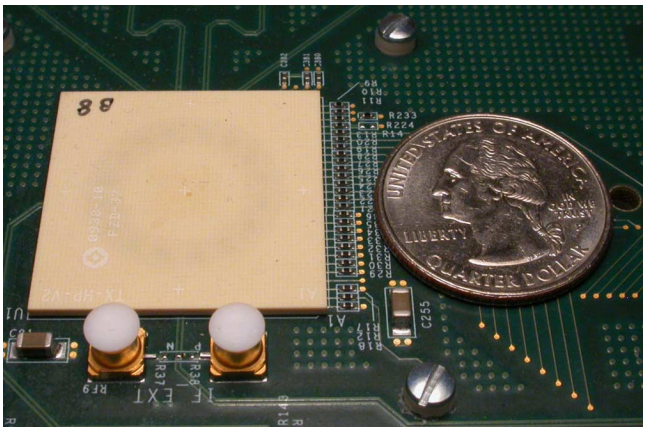


Fig. 25. Organic BGA package with TX IC and 16 antennas mounted on evaluation board.

Two important features of a phased-array transmitter, spatial power combining and beam steering, were evaluated in an antenna chamber. For these measurements, a horn antenna (with 14 dBi gain) was placed at a distance of 54 cm (62.5 dB propagation loss) from the TX evaluation board and a spectrum analyzer was employed to measure the power received by the horn antenna. All of the results presented in this section were obtained under the same nominal bias settings (3.8 W total power consumption) employed for the on-wafer measurements presented in Table II.

The phase settings for all elements were first set so that their outputs combine at a given point in space, in the direction of the horn antenna. The set of complex weights applied to the elements to form the beam include a single-pass correction for systematic amplitude and phase offsets between elements that are introduced by the package and antennas. The radiated from each element was then measured separately. Residual variations in the radiated power from individual elements are observed since no iterative calibration was applied to make them equal. Next,

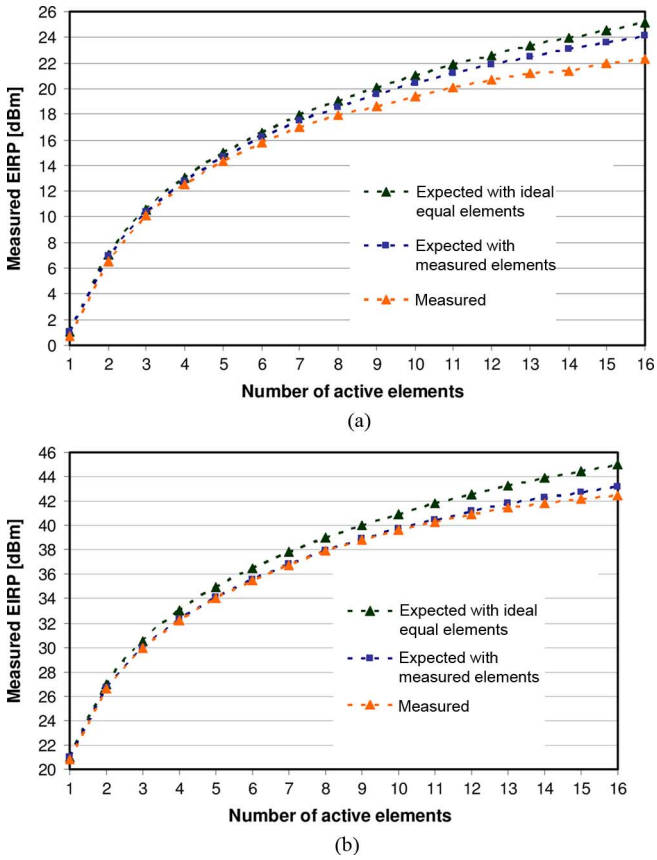


Fig. 26. TX EIRP at 60.48 GHz (channel 2) as a function of active elements. (a) In the linear region of the TX. (b) With TX at saturation. Measured from a packaged TX IC in an antenna chamber.

the 16 elements from the array were turned on sequentially in descending order of their relative strength (i.e., starting from the element with the highest radiated power), and the measured EIRP was recorded at every step.[2] The results of this experiment are shown in Fig. 26(a). As the number of active elements increases from 1 to 16, the measured radiated power increases by 22 dB. The measured spatially combined power as a function of the number of active elements can be compared against an expected result for two different sets of assumptions: 1) ideal power combining [as in (3)] with all elements equal to the one with the highest radiated power; and 2) ideal power combining considering the measured individual radiated powers. The measured spatial power combining behavior is in good agreement with these theoretical expectations [see (3)]. The result presented in Fig. 26(a) was taken in the linear range of the TX, at approximately 20-dB back-off. The experiment was repeated for the TX at saturation and the result is presented in Fig. 26(b). The packaged TX attains more than 40-dBm EIRP. It is important to note that between the measurements presented in Fig. 26(a) and (b) no adjustment in the phase settings was made, which shows that the relative phases between elements were maintained at saturation.

[2]The measured EIRP corresponds to: $EIRP_{TX} = P_H - G_H + L_P$[dBm], where P_H is the power measured at the horn antenna in dBm, G_H is the gain of the horn antenna in dBi and L_P is the propagation loss in dB.

TABLE II
SUMMARY OF PHASED-ARRAY TX PERFORMANCE OVER THE FOUR IEEE STANDARD CHANNELS AT 22 °C AND 65 °C. MEASURED BY WAFER PROBING

IEEE 802.15.3c channel number	1		2		3		4	
Center frequency [GHz]	58.32		60.48		62.64		64.8	
Temperature [ºC]	22	65	22	65	22	65	22	65
Single-path conversion gain [dB]	35	28	35	28	34	27	32	25
TX oP1dB at each element [dBm]	9.0	7.0	9.3	7.5	7.5	6.5	5.0	4.5
TX phase noise @1MHz [dBc/Hz]	90	88	89	88	89	86	87	87
Phase tuning per element	> 200º fine (5-bit) + 180º discrete (1-bit)							
Amplitude mismatch	+/- 1dB (Across elements)							
Carrier leakage	< -31 dBc							
I/Q gain error	< 1 dB							
I/Q phase error	< 1º							
-3dB IF channel BW	+/- 1GHz							
Output noise floor [dBm/Hz]	<-130dBm							
Total power consumption	3.8W @ 22ºC, 4.0W @ 65ºC							
Total area	6.5 x 6.75 mm^2							

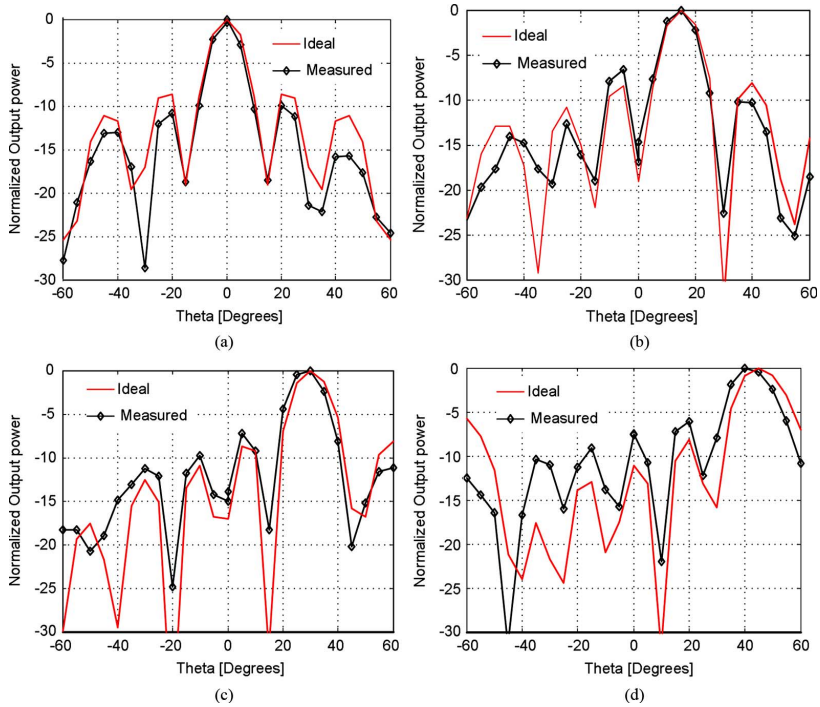


Fig. 27. 16-element radiation patterns at 60.48 GHz (channel 2) for (a) 0°, (b) 15°, (c) 30°, and (d) 45°. Measured from a packaged TX IC in an antenna chamber.

Fig. 27 shows four different 16-element radiation patterns measured in an antenna chamber; this measurement demonstrates beam-steering along Theta. Two-dimensional radiation pattern measurements, along the Theta and Phi spherical coordinates, have also been performed. Fig. 28 shows how a beam steered 18° in Theta rotates from 0° (a) to 90° in Phi (b). The ideal radiation patterns employed for comparison to these measurements assume 16 identical elements and isotropic antennas. It is also important to mention that these exemplary beams are general and were designed without any special considerations for sidelobe suppression or notch in a particular direction.

Finally, link experiments with the packaged TX IC and companion RX IC [26] have been performed. Beam-steered, non-line-of-sight wireless links with data rates up to 5.3 Gb/s have been achieved using 16-QAM single-carrier and OFDM modulations with a measured end-to-end EVM of −19 dB in both modes.

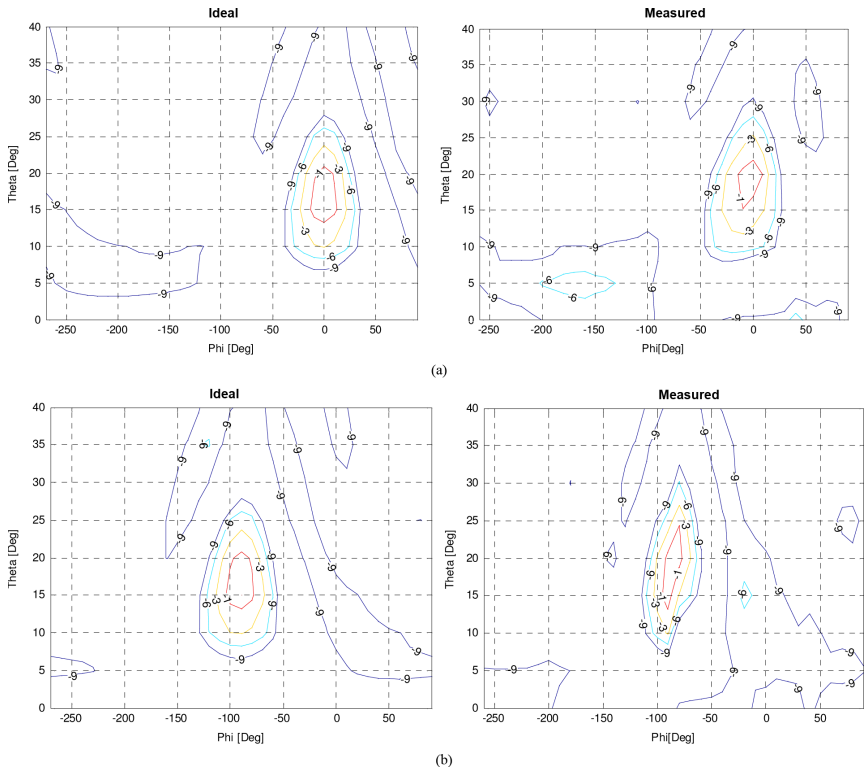


Fig. 28. Two-dimensional, 16-element radiation patterns at 60.48 GHz in spherical coordinates for (a) Theta $=$ 18° and Phi $=$ 0° and (b) Theta $=$ 18° and Phi $=$ −90°. Measured from a packaged TX IC in an antenna chamber.

TABLE III
STATE-OF-THE-ART IN SILICON MMWAVE PHASED-ARRAY TRANSMITTERS AND TRANSCEIVERS

Reference	This work	[6]	[7]	[8]	[9]	[10]
# of elements	16	4	16	4	6	4
Phase shifting	Passive RF	Active LO	Active RF	Active LO	Passive BB	Passive RF
oP1dB per element [dBm]	9-13.5	10.2	-5	11	0	-0.5
Total TX ouput power @ 1dBCP [dBm]	21-25.5	16.2	7	17	7.8	5.5
Center freq.[GHz]	-	77	-	60	60.48	-
RF 3dB BW [GHz]	51-65	-	39.9-45.6	5	-	56.6-59.5
Baseband BW [GHz]	1	-	-	-	0.6	-
Total DC power dissipation [W]	3.8-6.4	2 (TX)	3.6	0.590	0.96	0.078
Total area (mm^2)	6.5x6.75	6.8x3.8	2.6x3.2	2.9x1.4	5 x 2.5	1.6x1.0
Level of integration	Beamformer + superhet. upconversion + synthesizer + digital control + MSK modulator + IQ calibration	Antenna + TX and RX beamforming + superhet. up and down conversion	Beamformer	Beamformer + superhet. upconversion	Beamformer + direct upconversion + synthesizer	Bidiretional TX/RX beamformer + IF upconversion
Package	Organic BGA	-	-	-	LTCC	-
Technology	0.12um SiGe BiCMOS (200GHz f_T)	0.12um SiGe BiCMOS (200GHz f_T)	0.18um SiGe (150GHz f_T)	65nm CMOS	90nm CMOS	90nm CMOS

VIII. SUMMARY

A 16-element phased array TX for multi-Gb/s 60-GHz communication has been fully integrated in SiGe BiCMOS, achieving first pass success. A hybrid active/passive 1:16 power distribution design, the use of front-end beam tables, and a fully programmable (in terms of phase-shift, gain and output power) 60 GHz TX front-end have been introduced. The TX supports the main specifications of the 60-GHz IEEE 802.15.3c standard, including operation in four frequency channels, common-mode

signaling, and channel bandwidth, as well as the linearity and I/Q balance required to support Gb/s data rates with SC and OFDM modulation formats. Both beam steering and spatial power combining have been demonstrated with a packaged IC, and a NLOS wireless link has been established. To place the achieved results in perspective, Table III summarizes the current state of the art in silicon integrated phased-array transmitters and transceivers operating at mmWave (>30 GHz) frequencies.

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REFERENCES

[1] S. Reynolds, A. Valdes-Garcia, B. Floyd, B. Gaucher, D. Liu, and N. Hivik, "Second generation transceiver chipset supporting multiple modulations at Gb/s data rates," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2007, pp. 192–197.

[2] J. M. Gilbert, C. H. Doan, S. Emami, and C. B. Shung, "A 4-Gbps uncompressed wireless HD A/V transceiver chipset," *IEEE Micro*, pp. 56–64, Mar.-Apr. 2008.

[3] C. Marcu *et al.*, "A 90 nm CMOS low-power 60-GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, Dec. 2009.

[4] N. Fourikis, *Phased Array-Based Systems and Applications*. New York: Wiley, 1997.

[5] H. Krishnaswamy and H. Hashemi, "Integrated beamforming arrays," in *mm-Wave Silicon Technology: 60 GHz and Beyond*. Berlin, Germany: Springer, 2008.

[6] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local LO-path phase-shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[7] K.-J. Koh, J. W. May, and G. M. Rebeiz, "A millimiter-wave (40–45 GHz) 16-Element phased-array transmitter in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[8] W. L. Chan, J. R. Long, M. Spirito, and J. Pekarik, "A 60-GHz-band 2×2 phased-array transmitter in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 42–43.

[9] S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, and K. Maruhashi, "A 60-GHz band CMOS phased array transmitter utilizing compact baseband phase shifters," in *IEEE RFIC Symp. Dig.*, Jun. 2009, pp. 215–218.

[10] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four element phased-array at 60-GHz with RF-IF conversion block in 90 nm process," in *IEEE RFIC Symp. Dig.*, Jun. 2009, pp. 207–210.

[11] A. Valdes-Gacia *et al.*, "A SiGe BiCMOS 16-Element phased-array transmitter for 60-GHz communications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 218–219.

[12] *802.15.3c-2009, IEEE Standard for Information Technology—Telecommunications and Information Exchange Between Systems—Local and Metropolitan Area Networks—Specific Requirements. Part 15.3: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for High Rate Wireless Personal Area Networks (WPANs) Amendment 2: Millimeter-Wave-Based Alternative Physical Layer Extension*, .

[13] N. Onizawa, T. T. Hanyu, and V. C. Gaudet, "Design of high-throughput fully parallel LDPC decoders based on wire partitioning," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 3, pp. 482–489, Mar. 2010.

[14] A. Maltsev, R. Maslennikov, A. Sevastyanov, A. Khoryaev, and A. Lomayev, "Experimental investigations of 60 GHz WLAN systems in office environment," *IEEE J. Sel. Areas Commun.*, vol. 27, no. 8, pp. 1488–1499, Oct. 2009.

[15] FCC, Code of Federal Regulation, Title 47 Telecommunication, pt. 15.255, 2004.

[16] V.-H. Do *et al.*, "A 60 GHz SiGe-HBT power amplifier with 20% PAE at 15 dBm output power," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 3, pp. 209–211, 2008.

[17] C. Wang *et al.*, "A 60 GHz transmitter with integrated antenna in a 0.18 μm SiGe BiCMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 186–187.

[18] U. R. Pfeiffer and D. Goren, "A 20 dBm fully integrated 60 GHz SiGe power amplifier with automatic level control," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1455–1463, Jul. 2007.

[19] A. Valdes-Garcia, S. Reynolds, and T. Beukema, "Multi-mode modulator and frequency demodulator circuits for Gb/s data rate 60 GHz wireless transceivers," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2007, pp. 639–642.

[20] B. A. Floyd, "A 16–18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1076–1086, May 2008.

[21] M. Lei *et al.*, "Hardware impairments on LDPC coded SC-FDE and OFDM in multi-Gbps WPAN (IEEE 802.15.3c)," in *Proc. IEEE Wireless Communications and Networking Conf.*, Mar.-Apr. 2008, pp. 442–445.

[22] S. Suyama, H. Suzuki, K. Fukawa, and J. Izumi, "Iterative receiver employing phase noise compensation and channel estimation for millimeter-wave OFDM systems," *IEEE J. Sel. Areas Commun.*, vol. 27, no. 8, pp. 1358–1366, Oct. 2009.

[23] A. Natarajan, B. Floyd, and A. Hajimiri, "A bidirectional RF-combining 60-GHz phased-array front-end," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 202–203.

[24] E. Wilkinson, "An N-way hybrid power divider," *IRE T-MTT*, vol. MTT-8, no. 1, pp. 116–118, Jan. 1960.

[25] J. W. May and G. M. Rebeiz, "A 30–40 GHz 1:16 internally matched SiGe active power divider for phased array transmitters," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2007, pp. 765–768.

[26] S. Reynolds *et al.*, "A 16-element phased-array receiver IC for 60-GHz communications in SiGe BiCMOS," in *IEEE RFIC Symp. Dig.*, Jun. 2010, pp. 461–464.

[27] U. H. Gysel, "A new N-way power divider/combiner suitable for high-power applications," *IEEE MTT-S IMS Dig.*, pp. 116–118, May 1975.

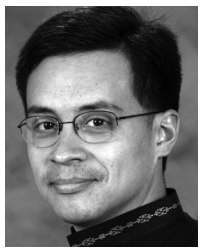
[28] H. Krishnaswamy, A. Valdes-Garcia, and J. W. Lai, "A silicon-based, all-passive, 60-GHz, 4-element, phased-array beamformer featuring a differential, reflection-type phase shifter," in *IEEE Int. Symp. Phased Array Systems and Technology*, Waltham, MA, Oct. 2010.

[29] R. N. Hardin *et al.*, "Electronically variable phase shifter utilizing variable capacitance diodes," *Proc. IRE*, vol. 48, pp. 944–945, May 1960.

[30] M.-D. Tsai and A. Natarajan, "60-GHz passive and active RF-path phase shifters in silicon," in *IEEE RFIC Symp. Dig.*, Jun. 2009, pp. 223–226.

[31] D. Liu, J. Akkermans, H. Chen, and B. Floyd, "Packages with integrated 60-GHz aperture-coupled patch antennas," *IEEE Trans. Antennas Propagat.*, to be published.

[32] D. G. Kam, D. Liu, A. Natarajan, S. Reynolds, and B. Floyd, "Development of low-cost organic packages with embedded phased-array antennas for 60-GHz wireless chipsets," *IEEE Trans. Microw. Theory Tech.*, submitted for publication.



Alberto Valdes-Garcia received the B.S. degree in electronic systems engineering from the Monterrey Institute of Technology (ITESM), Campus Toluca, Mexico, in 1999 (highest honors as best score from all majors), and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, in 2006.

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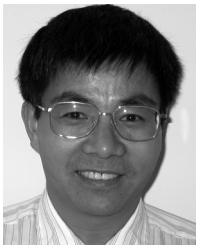

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