A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications

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***Abstract*—A fully-integrated 16-element 60-GHz phased-array receiver is implemented in IBM 0.12-μm SiGe BiCMOS technology. The receiver employs RF-path phase-shifting and is designed for multi-Gb/s non-line of sight links in the 60-GHz ISM band (IEEE 802.15.3c and 802.11ad). Each RF front-end includes variable-gain LNAs and phase shifters with each front-end capable of 360° variable phase shift (11.25° phase resolution) from 57 GHz to 66 GHz with coarse/fine gain steps. A detailed analysis of the noise trade-offs in the receiver array design is presented to motivate architectural choices. The hybrid active and passive signal-combining network in the receiver uses a differential cross-coupled Gysel power combiner that reduces combiner loss and area. Each array front-end has 6.8-dB noise figure (at 22 °C) and the array has −10 dB to 58 dB programmable gain from single-input to output. Sixteen 60-GHz aperture-coupled patch-antennas and the RX IC are packaged together in multi-layer organic and LTCC packages. The packaged RX IC is capable of operating in all four IEEE 802.15.3c channels (58.32 to 64.8 GHz). Beam-forming and beam-steering measurements show good performance with 50-ns beam switching time. 5.3-Gb/s OFDM 16-QAM and 4.5 Gb/s SC 16-QAM links are demonstrated using the packaged RX ICs. Both line-of-sight links (∼7.8 m spacing) and non-line-of-sight links using reflections (∼9 m total path length) have been demonstrated with better than −18 dB EVM. The 16-element receiver consumes 1.8 W and occupies 37.7 mm^2 of die area.**

***Index Terms*—Beamforming, BiCMOS, millimeter-wave, noise, phased array, power combiners, power splitter, receiver, RF-path phase-shifting, SiGe, WiGig, 60 GHz, 802.11 ad, 802.15.3 c.**

I. Introduction

EMERGING mass-market applications such as wireless high-definition video links and wireless data transfer between hard drives and computers require multi-Gb/s data rates. The 60-GHz band has 9 GHz of available bandwidth and can support short-range high data rate wireless links. Therefore, over the last five years there has been increasing research and commercial development of integrated circuits for 60-GHz wireless links. At 60 GHz, the 5-mm wavelength implies a path-loss of 82 dB (assuming path-loss exponent of 2) for a 5 m wireless link and the signal is attenuated further by any obstructions between the transmitter (TX) and receiver (RX). This attenuation is material dependent, e.g., the signal is attenuated by more than 20 dB when a person stands between the TX and RX and ∼10 dB when there is a 1-cm-thick wooden barrier between TX and RX. Fig. 1 outlines an example link budget for a 60-GHz system with obstructions, assuming typical integrated RX performance [1]–[4]. The desired signal-to-noise ratio (SNR) is assumed to be 25 dB. With the line-of-sight (LOS) signal attenuated by 20 dB, the required transmitter EIRP for a 5 m link is 53 dBm (assuming RX noise figure of 7 dB). Using high-gain antennas in the TX and RX can reduce the required TX output power to achieve desired EIRP—for example, 20 dB gain antennas in the TX and RX reduces the required PA output power to 13 dBm, which has been achieved on-chip [5]–[7]. However, 20-dB antenna gain corresponds to a beam width of 17°, which can be insufficient for applications where the location of the transmitter or receiver is not fixed. Increasing the beam width implies lower antenna gain, and therefore, higher TX output powers to achieve the same EIRP, making it difficult to integrate the power amplifier on silicon.

Phased arrays are an excellent solution to this challenge since they emulate a high-gain antenna by providing array gain, while also allowing for the directional beam to be steered using on-chip phase shifters. Using a phased-array RX and TX, the wireless link can be established by using reflections from features such as walls and ceilings. In this case, the reflective loss for the first reflection is assumed to be 10 dB based on measurements in a typical office environment [8]. Assuming that a 16-element phased-array transmitter provides 24-dB improvement in EIRP (due to spatial power combining) and that a 16-element phased array receiver has 12 dB higher SNR at the output, the target 25-dB SNR can be achieved for the geometry in Fig. 1 when each TX element in the 16-element TX array generates 11 dBm. The required power can be generated by on-chip PAs, making full silicon integration of transmitter and receiver possible.

Phased-array beam-steering capability requires multiple-element RX and TX array with on-chip variable phase shifters,

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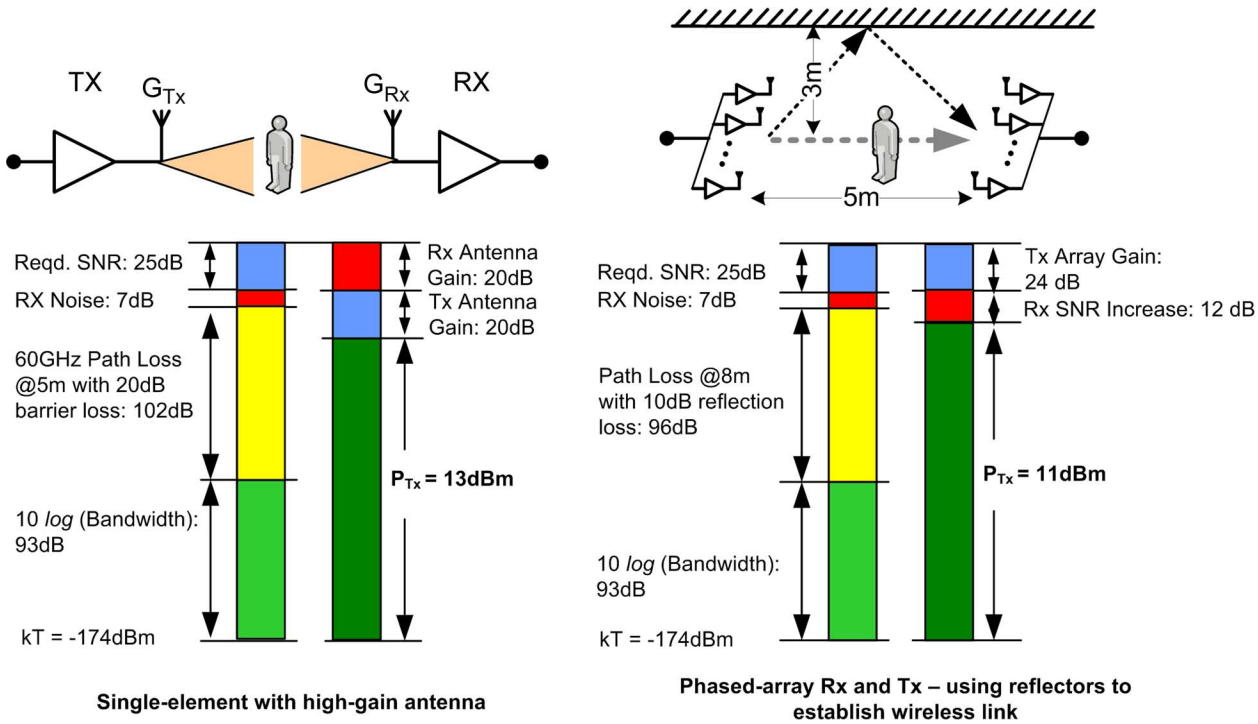

Fig. 1. An example link budget for single-element and phased-array 60-GHz wireless links.

variable gain stages, and combining and distribution circuits, leading to system and circuit complexity. Such mm-wave phased arrays have been demonstrated at 24 [9], 77 [5], 40 [10], and 60 GHz [6], [7], [11]. Silicon integration allows the complex system to be realized with high-yield and enables high-volume applications such as wireless high-definition video links and multi-Gb/s data transfer.

In the following sections, a 60-GHz phased-array receiver targeted for multi-Gb/s wireless links is described. (A companion fully-integrated 16-element phased-array transmitter was also designed and is described in [6]). The IC is designed in the 0.12-μm IBM SiGe BiCMOS technology ($f_{\mathrm{T}} \sim 200$ GHz; $f_{\mathrm{MAX}} \sim 285$ GHz) and supports non-line-of-sight (NLOS) wireless communication in all four channels in the 60-GHz band, in accordance with the IEEE 802.15.3c standard [12]. Section II describes the architecture of the 60-GHz 16-element phased-array RX, focusing on array output noise and SNR. Section III discusses the circuits in the array RX and includes block-level measurements. Probe-based full-chip measurements are detailed in Section IV. The RX IC was packaged with 16 patch antennas on organic and LTCC substrates [13] and beam-pattern and beam-steering measurements were performed in an antenna chamber. The packaged RX array IC was also tested in conjunction with the packaged phased-array transmitter IC to demonstrate line-of-sight and reflection-based links using single-carrier (4.5 Gb/s) and OFDM (5.3 Gb/s) modulation. The results of these phased array beam-pattern and link measurements are presented in Section V.

II. Architecture

A. Double Down-Conversion Architecture

The 60-GHz receiver architecture is shown in Fig. 2. The frequency plan is similar to the sliding-IF super-heterodyne architecture in [1]. The on-chip PLL, described in [14], generates the LO signals for the channel frequencies specified in IEEE 802.15.3c [12] (58.32 GHz, 60.48 GHz, 62.64 GHz, and 64.8 GHz) from a reference at 308.5714 MHz. The receiver frequency plan is also compatible with other 60-GHz standards such as ECMA [15], WiGig, and WirelessHD, all of which mandate the same channel frequencies. The on-chip 16-to-18.6-GHz tuning-range VCO drives a frequency-tripler that provides the LO signal for the first downconversion (specifically at 49.99 GHz, 51.84 GHz, 53.69 GHz, and 55.54 GHz). The sliding-IF frequencies are 8.33 GHz, 8.64 GHz, 8.95 GHz, and 9.26 GHz, and a programmable resonant load in the IF amplifier (with fixed inductor and variable capacitors), keeps its performance centered. A divide-by-two frequency divider generates in-phase and quadrature-phase LO signals which are applied to programmable phase rotators that drive the downconversion mixers, allowing for quadrature phase error correction. Finally, baseband channel-select filters were not included in this design, but were fabricated stand-alone for evaluation.

B. RF-Path Phase-Shifting

Integrated mm-wave phased-arrays have been demonstrated using RF-path [6], [10], [16], LO-path [9] and IF/baseband phase-shifting architectures [17]. Low power consumption and area motivate the selection of RF-path phase shifting and RF combining, since it requires the least number of parallel circuit blocks per phased-array element; however, RF phase shifters do result in potential performance degradation due to phase-shifter loss, noise, and linearity. Both active interpolator-based and passive reflection-type RF-path phase shifters were considered for this design, as detailed in [18]. Key considerations were noise figure, power consumption, and insertion loss versus

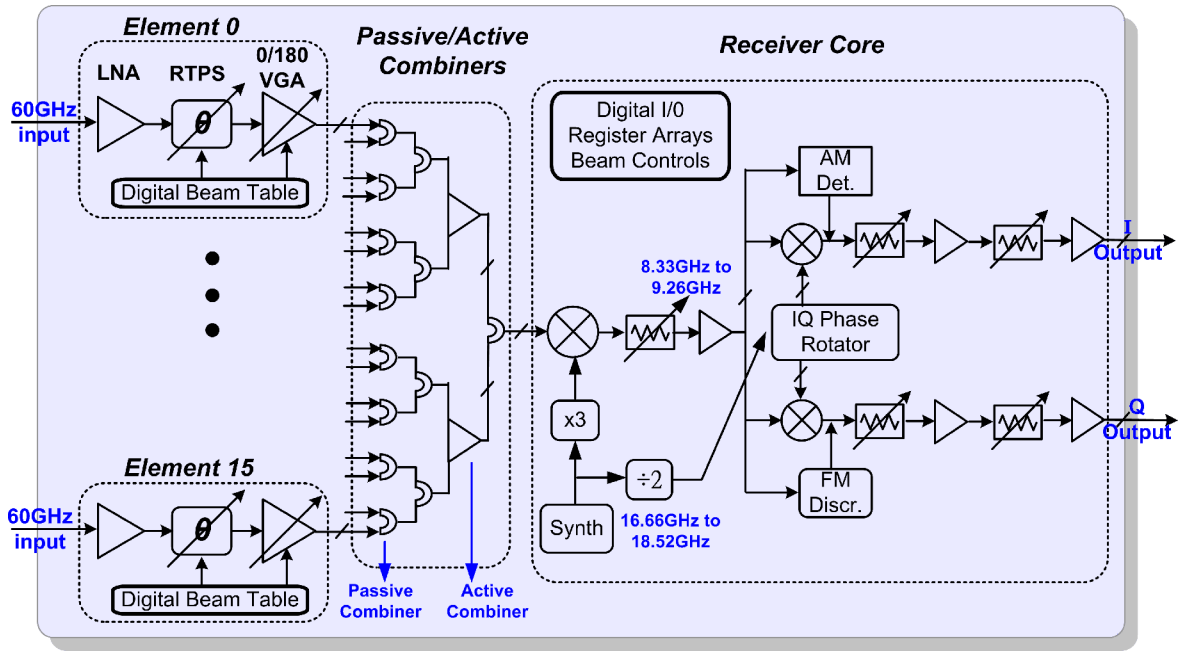

Fig. 2. Fully-integrated 60-GHz phased-array receiver architecture and frequency plan.

phase shift. It was found that with LNA gain of ~22 dB and noise figure of 6 dB, subsequent cascaded blocks with noise figure (NF) of 15 dB degrade the front-end noise figure by less than 0.25 dB. This means that either passive reflection-type phase shifters (with insertion loss of 8 dB) or active vector interpolators (with noise figure of 15 dB) can be used in the system. Though the noise trade-off between active and passive phase shifters was not significant, the power consumption is lower with the passive approach, ultimately leading to its selection for the phased array presented herein.

One challenge with the passive reflection-type phase shifter, though, is the dependency of phase-shifter loss on phase-shift setting. This variation of loss with phase shift arises from the use of a varactor in the passive phase shifter which has a relatively low and variable quality factor (3 to 8 @ 60 GHz). Ideally, amplitude and phase shift would be independently adjustable in the array, allowing for simple pattern synthesis. In this work, a variable-gain amplifier (VGA) was added following the passive phase-shifter to compensate for the insertion-loss in the phase shifter and to allow additional amplitude control for pattern synthesis. Furthermore, a discrete 180° phase shift can be easily achieved in the VGA, which has the benefit of reducing the variable phase-shift range required from the passive phase-shifter to 180°. The lower variable phase-shift range reduces phase-shifter loss. Therefore, a hybrid passive-active RF-path phase shifting approach was adopted as shown in Fig. 2.

C. Array Noise and RF-Combining

In the following, the SNR at the output of the array and array output noise are used to analyze the RX array performance. The SNR at the output of an ideal N-element phased-array with unit antenna gain G_{ant}, perfect isolation between elements, and noiseless combining, is N times higher than the SNR at the output of an equivalent single-element receiver with antenna gain G_{ant}. Physically, this improvement occurs because the noise from different elements adds incoherently while the phase-shifted signals from all the elements add coherently [9]. Correspondingly, if there is a correlation in the noise sources in the elements, e.g. through antenna coupling [19], biasing circuits or through LO phase-noise (in the case of IF/Baseband phase shifting), the improvement in SNR is degraded.

The noise factor F of a receiver is defined as

$$F = \frac{\mathrm{SNR_{IN}}}{\mathrm{SNR_{OUT}}}. \tag{1}$$

In the case of an N-element phased-array receiver, the application of (1) is not straightforward, as it depends on whether the input SNR is defined for a single-element or for the complete array. A single-element definition for $\mathrm{SNR_{IN}}$ is applied to the noise factor equation, as follows:

$$F_{1:N} = \frac{\mathrm{SNR_{IN,SINGLE\_ELEMENT}}}{\mathrm{SNR_{OUT,ARRAY}}} \tag{2}$$

where the *1:N* subscript refers to the fact that a single element input is taken with respect to an N-element output. Following the coherent-combining argument in the previous paragraph, the output SNR can be N times higher than the single-element output SNR, potentially leading to $F_{1:N} < 1$ (negative noise figure in dB). For example, if the noise is dominated by front-end noise

$$F_{1:N} = \frac{F_{\mathrm{FE}}}{N} \tag{3}$$

where F_{FE} is the front-end noise figure. In this case, $F_{1:N} < 1$, when $F_{\mathrm{FE}} < N$. In (2), the numerator ignores the multiple receive elements that form the array. In order to consider the inputs to all receiver elements, the concept of total array aperture is leveraged. In [20], a formulation for the SNR improvement in an array is developed using the effective aperture area of the

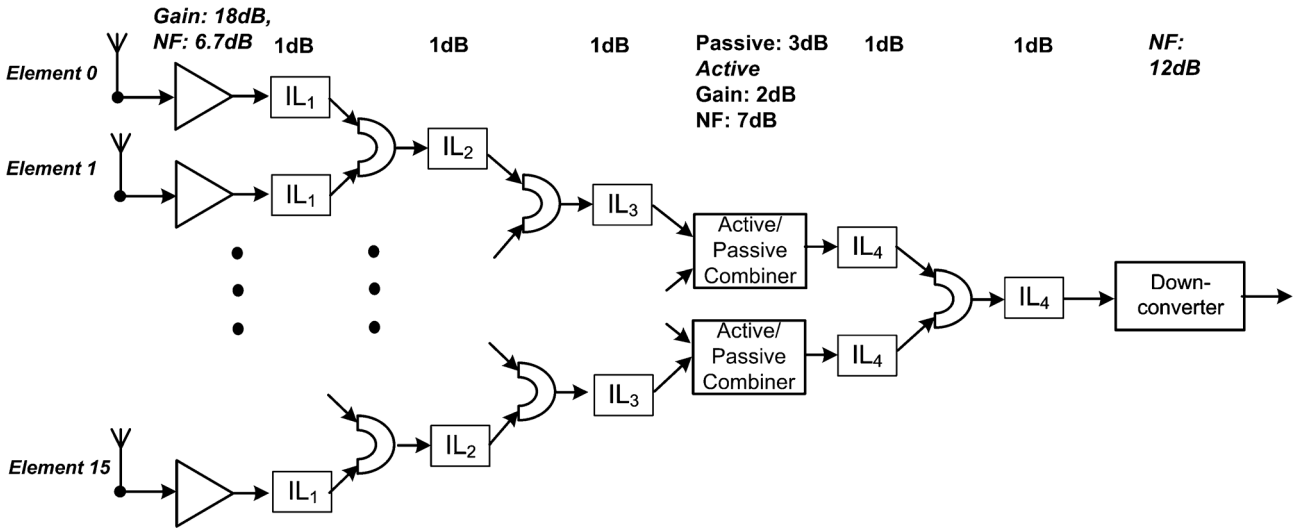

Fig. 3. Simplified block diagram of a phased-array receiver with gain, noise and loss of receive chain blocks.

N-element phased array. With N elements in the array, the antenna aperture is N times that of a single-element and the noise factor of the array, $F_{\rm RX}$ is defined as

$$F_{\rm RX} = \frac{N \cdot {\rm SNR}_{\rm IN,SINGLEELEMENT}}{{\rm SNR}_{\rm OUT,ARRAY}} = N \cdot F_{1:N}. \quad (4)$$

The total noise at the output of the array will include (ideally) uncorrelated contributions from the N front-ends in the array, noise due to losses in the combination network, and correlated noise arising after the combination and downconversion network (e.g., in the mixer for an RF-combined array). If LNA gain is high, the SNR at the output of the phased array is close to but less than $N \cdot {\rm SNR}_{\rm OUT,FE}$ where ${\rm SNR}_{\rm OUT,FE}$ is the SNR at the output of each front-end. The effects of downstream loss and correlated noise can be encapsulated in an "array efficiency term", η_A, as follows:

$${\rm SNR}_{\rm OUT,ARRAY} = N \cdot \eta_A \cdot {\rm SNR}_{\rm OUT,FE} \quad (5)$$

where $\eta_A \leq 1$. Combining (4) and (5) results in

$$F_{\rm RX} = \frac{N \cdot {\rm SNR}_{\rm IN,SINGLEELEMENT}}{N \cdot \eta_A \cdot {\rm SNR}_{\rm OUT,FE}} = \frac{F_{\rm FE}}{\eta_A}. \quad (6)$$

In this formulation, as the gain of the RF front-end in each element increases, the array efficiency increases and hence $F_{\rm RX}$ approaches the RF front-end noise figure (ignoring antenna-coupling). In practice, power consumption trade-offs and device performance limit the RF front-end gain at 60 GHz, resulting in smaller η_A as the array noise figure is sensitive to the loss and noise in the combining network and the downconversion chain. One benefit of the approach detailed above is that system-level noise analysis is handled by considering the phased array as being equivalent to a single receiver with noise factor $F_{\rm RX}$, and antenna gain of $NG_{\rm ant}$. It must be noted that the gain of the equivalent receiver is N times the gain from each element to the output. Compared to a single-element receiver with small unit antenna gain, using multiple elements provides a technique to achieve better sensitivity in the receiver while the beam steering capability allows for a wide field-of-view.

The RF-combining network in the array can be passive or active—power dissipation and linearity constraints favor a full passive-combining approach. Isolation between the inputs to the combiner is preferable to accommodate array operation with a subset of elements turned on and to ensure that the phase-shift settings of each element are independent of the state of other elements. Fig. 3 shows a simplified block diagram of the array with gain, noise figure and insertion loss of different blocks in the array with the passive combiner loss lumped into the loss of the interconnect t-lines. In an ideal 3 dB combiner (e.g. an ideal 3-dB Wilkinson-type combiner), when an input is applied to only one of the input ports with the other input port terminated in a matched load, the output is 3 dB lower than the input. For a 16-element array receiver, with passive combiners at each of the four stages of combining, the downconverter noise represents more than 60% of the output noise when only one array element is on, leading to poor noise performance (array efficiency of 0.27). Noise from the RF front-ends starts to dominate the output noise as more elements are turned on; however the array efficiency for the cascade of blocks in Fig. 3 is 0.75 with eight elements on and 0.86 with all 16 elements on.

In this work, an active combiner was used in the third stage of combining to improve array efficiency with a subset of elements on. With an active combiner gain of 2 dB and noise figure of 7 dB from each input to the output, the array efficiency improves to 0.51 with one element on, 0.90 with eight elements on, and 0.95 with all 16 elements on. The differential cross-coupled Gysel passive-combiner network (described in Section III) adopted also reduces passive combining loss by reducing the length of the signal-routing t-lines, improving array efficiency across different operation modes.

III. Circuits and Block-Level Measurements

A. RF Front-end

In the RF-path phase shifting architecture, each element must be able to achieve 360° variable phase shift across the frequencies of interest (57.2 to 65.9 GHz), while providing low noise

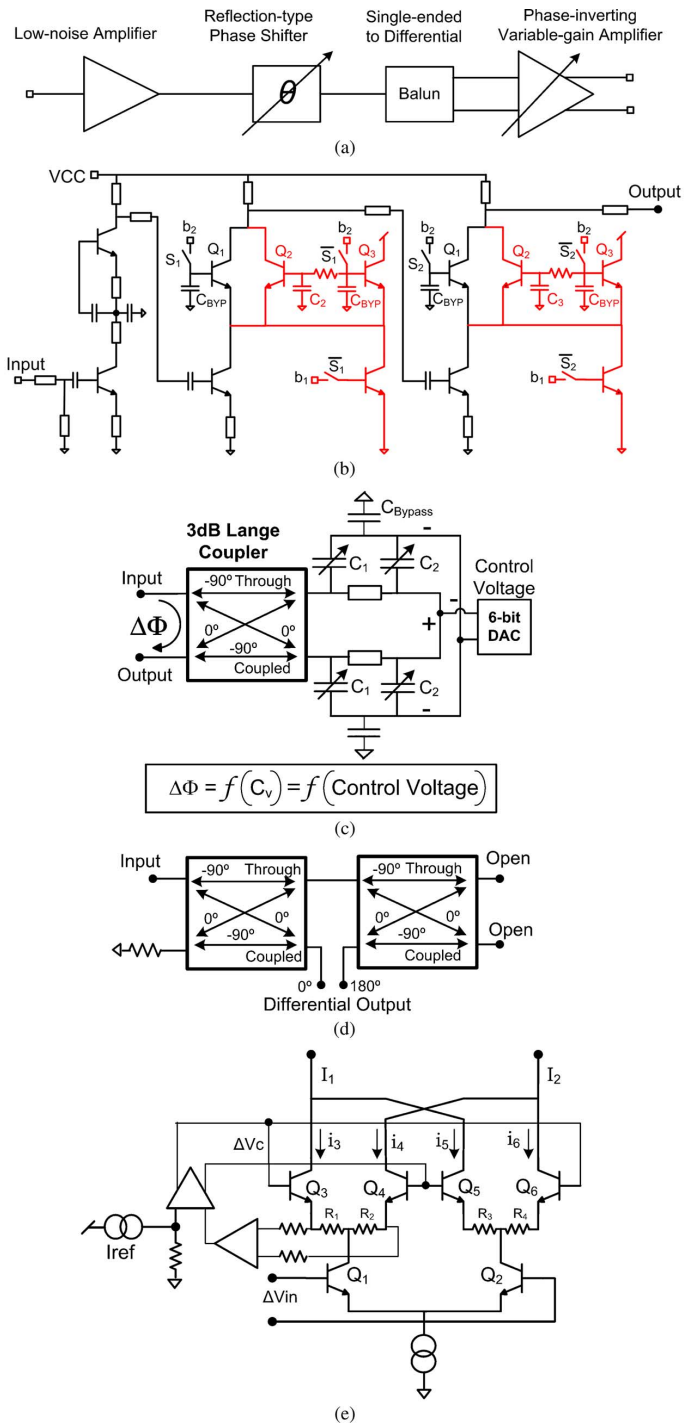

Fig. 4. Schematics of 60-GHz phased-array RF front-end circuits. (a) 60-GHz phased-array RF front-end. (b) 60-GHz LNA with switched-gain. (c) Reflection-type phase shifter. (d) 60-GHz Lange-Lange balun. (e) Phase-inverting variable-gain amplifier.

figure and sufficient linearity. The RF front-end in each element consists of a 60-GHz variable-gain low-noise amplifier (LNA) followed by a reflection-type phase shifter (RTPS) that provides 180° of phase shift (Fig. 4). The phase-inverting variable-gain amplifier (PIVGA) following the RTPS provides a discrete 0/180° phase shift as well as variable gain in fine steps. Each RF front-end element occupies 1.7 mm by 0.65 mm.

1) 60-GHz Low-Noise Amplifier: The single-ended 60-GHz LNA (Fig. 4) has four stages and provides 2 bits of coarse gain control. In the packaged system, the antennas are connected to the LNAs through 50Ω traces on the package and controlled-collapse chip connection (C4) flip-chip interconnect. Therefore, the LNA input match is designed using models for the C4 solder bump interconnect that were developed with EM simulations. The simulations demonstrate ∼0.5 dB loss for the single-ended ground-signal-ground C4 interconnect between the IC and traces on the package. The LNA employs current reuse in Stage 1 and Stage 2 similar to the design in [1]. Stage 3 and Stage 4 provide coarse gain step using an alternate signal path [21]. When switch S_1 is high, Stage 3 of the LNA is in high-gain mode. In this mode, the transistor Q_1 is activated and the path through transistor Q_2 and Q_3 is deactivated. In this case, the transconductance of the combination of Q_0 and Q_1, $G_{\mathrm{m,HG}}$, is

$$G_{\mathrm{m,HG}} = \frac{\mathrm{g_{m,Q0}}}{\mathrm{g_{m,Q1}} + sC_{\pi,\mathrm{Q1}}} . \mathrm{g_{m,Q1}} \tag{7}$$

where $\mathrm{g_{m,Q0}}$ and $\mathrm{g_{m,Q1}}$ are the transconductances of Q_0 and Q_1 and $C_{\pi,\mathrm{Q1}}$ is the base-emitter capacitance of Q_1. In low-gain mode, switch S_1 is low which disables Q_1 and enables transistors Q_2 and Q_3. The RF current from Q_0 is divided between Q_2 and Q_3. Furthermore, in the case of Q_2, there is a voltage division between the capacitor at the base, C_2, and the base-emitter capacitance, C_π. Ignoring parasitics, the admittance looking into the cascode node in the low-gain mode, Y_{casc}, is the sum of the parallel admittances looking into the emitters of Q_2 and Q_3

$$Y_{\mathrm{casc}} = \frac{\mathrm{g_{m,Q2}} + sC_{\pi,Q2}}{1 + \frac{C_{\pi,Q2}}{C_2}} + \mathrm{g_{m,Q3}} + sC_{\pi,Q3} \tag{8}$$

where $\mathrm{g_{m,Q2}}$ and $\mathrm{g_{m,Q3}}$ are the transconductances of Q2 and Q3 respectively and $\mathrm{C}_{\pi,\mathrm{Q2}}$ and $\mathrm{C}_{\pi,\mathrm{Q3}}$ are the base-emitter capacitances of Q_2 and Q_3. The effective transconductance of the combination of Q_0, Q_2, and Q_3 in low-gain mode is given by

$$G_{\mathrm{m,LG}} = \frac{\mathrm{g_{m,Q0}}}{Y_{\mathrm{casc}}} . \frac{\mathrm{g_{m,Q2}}}{1 + \frac{C_{\pi,Q2}}{C_2}} . \tag{9}$$

When compared to (7), the RF current division between Q_2 and Q_3, along with the capacitive division at the base of Q_2 result in lower gain in (9). This switched-gain technique is implemented in Stage 3 as well as Stage 4 and provides nearly a dB-for-dB trade between gain and compression point for each stage. The dummy transistor, Q_3, also reduces the difference between Y_{casc} in the high gain and low modes, which was necessary in versions of the LNA that included a notch filter in the cascade node for image rejection (used in single-element Rx). Measurements show that across the LNA gain settings the LNA gain is 24, 16, 7, and −1 dB and the noise figure is 5.6, 6.8, 5.8 and 9.4 dB. When the LNA gain is reduced from 24 dB to 16 dB, the measured $\mathrm{iP_{1dB}}$ improves from −28 dBm to −21 dBm. For the lowest LNA gain setting of −1 dB, the $\mathrm{iP_{1dB}}$ is −9 dBm. The LNA consumes 12 mA from 2.7 V.

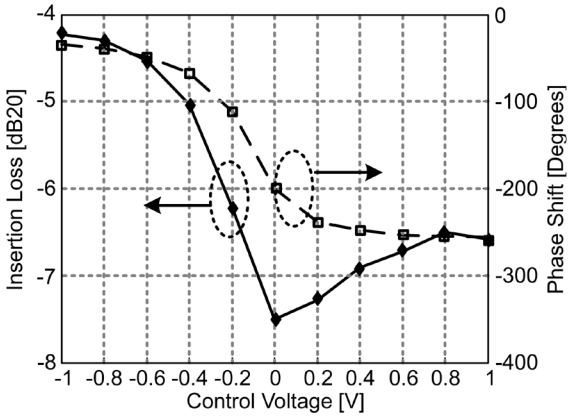

Fig. 5. Measured 60-GHz reflection-type phase-shifter loss and phase shift across control voltage [20].

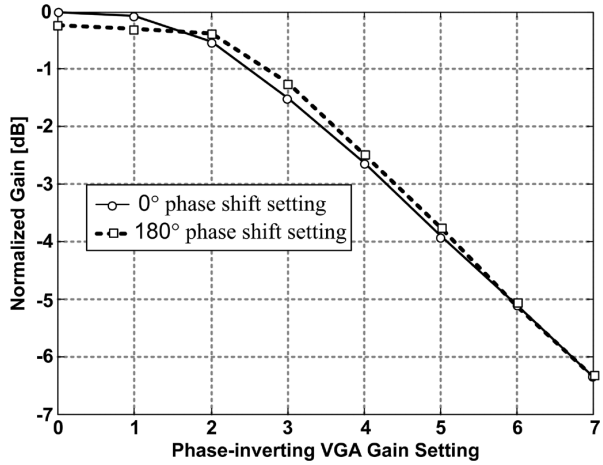

Fig. 6. Measured PIVGA gain variation—PIVGA is capable of providing ~6 dB of gain variation in 0o and 180o modes.

2) Reflection-Type Phase-Shifter (RTPS): The passive RTPS at 60 GHz incorporates a Lange coupler with an optimized reflective load (Fig. 4) [18], [22]. The phase shift from input to output is varied by varying the varactors, C_1 and C_2, jointly. As mentioned in Section II, the RTPS must provide 180° phase-shift variation across the band. Fig. 5 shows the measured RTPS phase shift and loss across control voltage settings [18]. The RTPS phase resolution is limited by the resolution of the DAC providing the control voltage across the varactors. In this receiver, a 6-bit voltage DAC was used to generate the control-voltage. The nonlinear relationship between control-voltage and phase-shift (Fig. 5) results in 11.25° phase resolution in the RTPS with <4° max error (The PIVGA following the RTPS provides 1 bit phase control (0° or 180° phase shift), resulting in overall 5-bit phase resolution in the array). The quality factor of the varactors in RTPS varies from 3 to 8 at 60 GHz. The resulting loss variation across phase shift settings in the RTPS (Fig. 5) is undesirable as it results in amplitude mismatch between elements (each element of the array will have a different phase shift setting to steer the beam in a particular direction). The loss also implies that cascading two RTPS to achieve 360° phase variation leads to phase-shifter loss varying from 8 dB to 15 dB depending on phase-shift setting. Therefore, a phase-inverting VGA was designed to achieve both 180° phase shift and fine variable gain to compensate for RTPS loss. Measurements on the RTPS across a wafer show rms phase shift variation of 2.7°, while the maximum relative phase-shift variation from 10°C to 85°C is 9°. These measurements indicate repeatable RTPS performance, allowing for the relative phase shift in an element to be set without any need for chip or element calibration.

3) Phase-Inverting Variable Gain Amplifier (PIVGA): The LNA and the RTPS are single-ended, hence a broadband passive Lange-Lange balun is used to generate a differential signal (Fig. 4). It consists of two Lange couplers in series with an open at the through and coupled ports of the second coupler. The Lange-Lange balun is larger than a transformer (it occupies $480\ \mu\text{m} \times 180\ \mu\text{m}$) but was chosen because of its large bandwidth and to reduce the sensitivity of the design to EM modeling errors. Following the balun, the PIVGA uses cascode current steering to achieve variable gain (at least 4 dB to compensate for RTPS gain variations) as well as a discrete phase shift of 180° (Fig. 4). An earlier implementation of the PIVGA used a tanh stage to generate the cascode transistor base voltages from the control voltage, thereby linearizing the gain response with respect to control voltage [21]. This technique, however, displayed temperature and process sensitivity in simulation. Therefore, the PIVGA in this work uses a negative-feedback control scheme to linearize the gain response with respect to the control voltage. The scheme senses the dc current difference between transistor Q_3 and Q_4 and forces it to be equal to $k\text{I}_{\text{control}}$ using a negative feedback loop. $\text{I}_{\text{control}}$ is generated from a 3-bit current DAC with one extra bit that ensures maximum gain by making all the RF current flow through Q_3 or Q_4. The measured variable gain control in the PIVGA at 60.18 GHz in 0° and 180° mode is shown in Fig. 6. The negative-feedback scheme reduces the impact of mismatch between Q_3 and Q_4, thereby reducing the sensitivity of the gain control to temperature and process variations. Note that all circuits in the receiver following the PIVGA, i.e. the combiners, RF mixer, IF mixer, and baseband circuits are differential.

B. RF Combining

The signals from 16 elements are combined in a binary scheme in four stages: two stages of passive combining using a cross-coupled Gysel combiner, followed by an active combiner, with a final passive combiner driving the differential RF mixer.

1) Differential Cross-Coupled Gysel Combiner: The signals from all 16 elements in the receiver must be combined before the RF mixer. In addition to small area and insertion loss, the combiner must also provide isolation between different elements to ensure that the output of an element is independent of any other element state and to allow the array to operate with only a subset of elements on. Passive transmission-line (t-line) based power combiners such as Wilkinson (single-ended and differential) [23] have been used at mm-wave frequencies. While the Wilkinson combiner satisfies loss, isolation and bandwidth criteria, in a practical Wilkinson combiner layout, the two inputs have to be close to each other to allow the isolation resistor to be connected between them. This leads to long signal routing

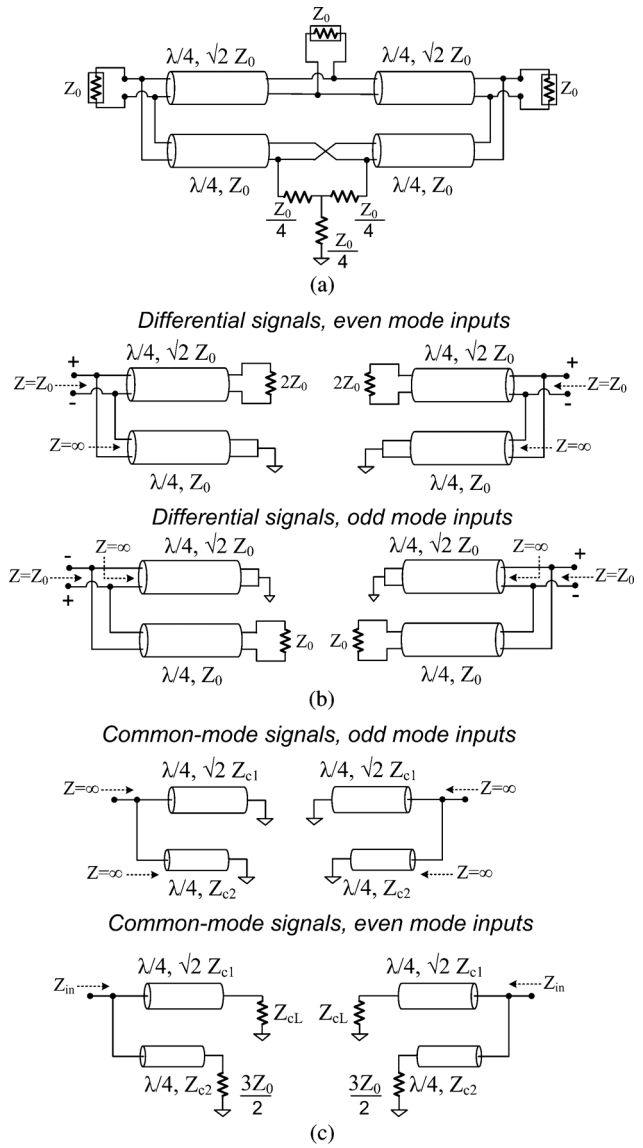

Fig. 7. Differential cross-coupled power combiner. (a) Differential cross-coupled-Gysel power combiner. (b) Analysis for differential input. (c) Analysis for common-mode input.

in a corporate tree-combining structure, resulting in larger area and higher loss.

In this design, we use a differential cross-coupled Gysel power-combiner [Fig. 7(a)]. This combiner is based on the Gysel power combiner that allows the two inputs to be located far from each other [24] which allows the signal routing t-lines to be folded into the combiner structure, significantly reducing loss and the area required for the combining network area.

In a traditional Gysel combiner, isolation is provided between the two inputs by connecting a t-line which is one wavelength long at the frequency of operation together with two absorbing loads $2Z_o$ in value located at the $\lambda/4$ and $3\lambda/4$ positions along the isolation arm. When differential signals and transmission lines are used, the length of this isolation arm can be reduced to only $\lambda/2$ by introducing a cross-connection (or "twist") in the t-line between the inputs, achieving a 180° phase shift. The load-absorbing resistor is placed across the "twist" connection—a resistor of value Z_o provides matching for differential inputs but is effectively open for common-mode inputs. Therefore, a more complex network is used to present a load impedance for common-mode inputs as well.

Fig. 7(b) and (c) show an analysis of the structure for differential and common-mode inputs, demonstrating matching in odd-mode and even-mode. Here, differential and common-mode are used to describe the local phase relationship between the positive and negative *signals* on the differential transmission line, whereas even and odd-mode are used to describe the global phase relationship between the two *inputs* to the combiner. There are therefore four cases to consider, as follows: even-mode inputs with differential signaling (the "normal" operational mode in the phased-array receiver), even-mode inputs with common-mode signaling, odd-mode inputs with differential signaling, and odd-mode inputs with common-mode signaling.

For differential signaling, the structure is matched for both odd and even mode inputs as shown in Fig. 7(b). For common-mode signaling and odd-mode inputs, as shown in Fig. 7(c), there is effectively an open-circuit input impedance. Since the output of the PIVGA is differential, the common mode signals are small and mismatches between PIVGA common-mode output impedance and the combiner common-mode impedance have minimal impact on performance.

Fig. 8 shows the simulated and measured performance of the cross-coupled Gysel combiner. Port 1 and Port 2 are the differential input ports while Port 3 is the differential output port. The measurements in Fig. 8 were performed on a breakout and include the loss of the pads and t-lines feeding the combiner.

2) Active Combiner: As shown in the analysis in Section II, the array noise performance is adversely affected if only passive combiners are used in the array. Therefore, an active combiner is used in the third stage of combining. The combiner consists of two differential cascode transconductance stages (Fig. 9). The output currents from the two transconductance stage are added after the cascode transistors to achieve signal combining. The output of the combiner is matched to 100Ω differential load. The bias of each of the transconductance stages can be varied (not shown in Fig. 9). In addition, each of the branches can be independently turned off by making S1 or S2 low, dividing the array into blocks of four elements. The combiner consumes 17 mA from a 2.7-V supply. Fig. 10 shows the measurement S-parameters for the active combiner. The combiner 1-dB compression point with respect to each input was simulated to be -10 dBm.

C. RF-to-IF Mixer

The combined output power from 16 front-ends is theoretically 12 dB higher than in the case of a single-element Rx, assuming ideal passive combining. In the present RX, considering both the passive combiner losses and the gain of the single active combining level, the input power to the RX core can be higher than -10 dBm. At the same time, the RF-to-IF mixer can contribute to the overall RX NF, particularly if not all elements are in use. Thus, the RF-to-IF mixer and the RX core are designed to have wide dynamic range. A simplified schematic of the RF-to-IF mixer is shown in Fig. 11; it is a double-balanced Gilbert cell with a differential, common-base input stage.

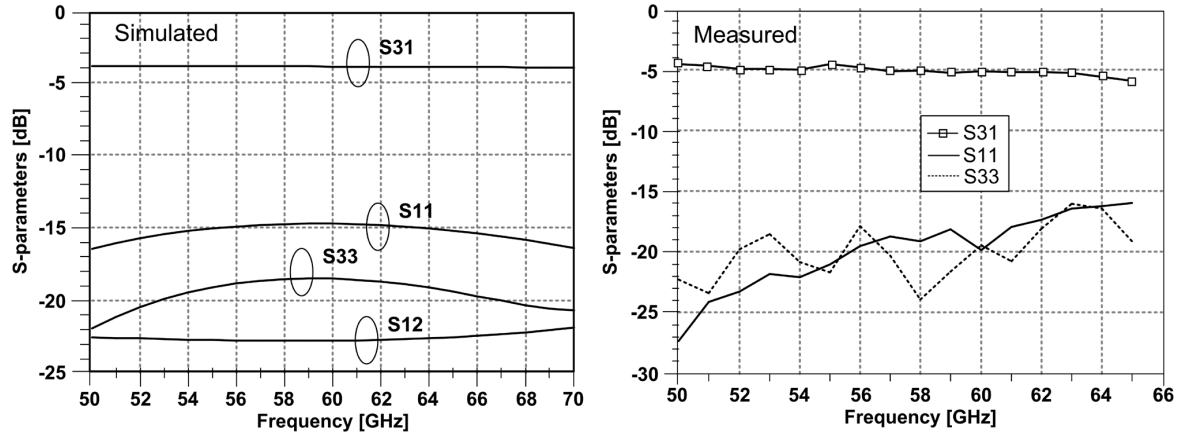

Fig. 8. Simulated and measured differential modified-Gysel S-parameters from one input to output.

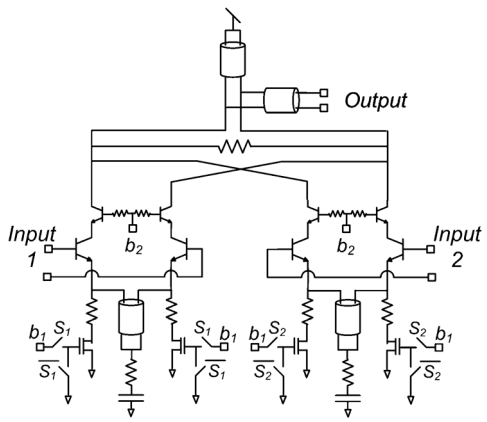

Fig. 9. Schematic of 60-GHz active combiner used in the third stage of combining.

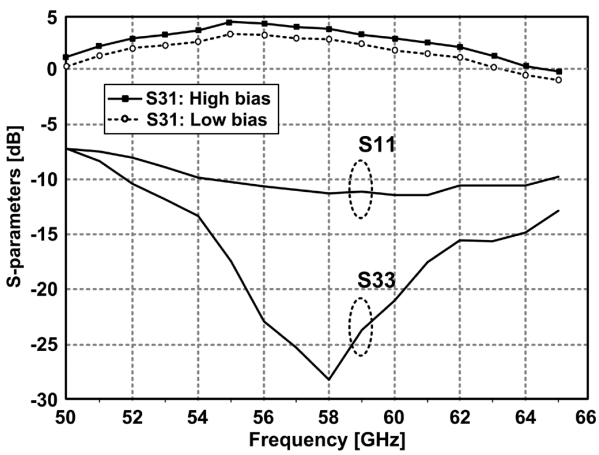

Fig. 10. Measured active combiner differential S-parameters from one input to output (including t-line and pad losses).

The bias current through each of the legs is nominally 7 mA and is made adjustable by switch-selecting various values of emitter resistors in the common-base stage. The IF-output RLC load is tuned to the IF in the 8.3–9.3-GHz range, and the center frequency is made adjustable with selectable capacitors. The nominal voltage conversion gain is 15 dB, and the IF output can be attenuated in 6-dB steps by switch-selecting the appropriate tap on a resistive voltage divider. The inset in Fig. 11 shows the IF switch, which is implemented as a switched emitter-follower. The RF-to-IF mixer achieves a measured SSB NF of 10.4–11.5 dB over the four IEEE channels, and an input-referred 1-dB compression point of -4 dBm. The LO power requirement is -4 dBm for optimum performance.

D. IF and Baseband

The IF-signal from the RF-to-IF mixer passes through a second set of quadrature mixers and is converted to a baseband signal. A phase rotator between the LO divide-by-two and the quadrature mixers allows adjustment of the quadrature LO phases to achieve quadrature accuracy of $\pm 1^{\circ}$. The baseband signal passes through a series of coarse (6 dB) and fine (1 dB) step attenuators and 16-dB fixed gain amplifiers to provide the required gain range. The attenuation sequence (using the baseband and IF attenuators, and the RF gain control) is selected to avoid compressing any internal stages, such that the input compression point of the overall Rx rises monotonically as the gain is reduced. The phased-array receiver includes a frequency discriminator for demodulating up to 2-Gb/s FSK/MSK signals and an AM detector for demodulating up to 2-Gb/s ASK modulated signals. The circuits are described in detail in [25].

IV. On-Wafer Phased-Array Receiver IC Measurement Results

The fully-integrated 60-GHz phased-array receiver occupies 6.08 mm by 6.2 mm and the chip includes $\sim$1900 NPN and $>$330K CMOS transistors (Fig. 12). Each of the 16 Rx front-ends occupies 1.7 mm by 0.65 mm. The chip has extensive digital programmability and the on-chip digital interface can be read and written in serial and parallel modes. The RF front-ends include a 32-word register array that can store gain and phase settings for all elements corresponding to 32 beam directions, enabling fast beam switching. The RX IC also includes three temperature sensors located at the eastern edge, western edge and center of the chip. Two variants of the chip were designed: one with pads compatible with probe-based testing and another with pads that have solder-bumps for flip-chip packaging. The circuits in the array were also characterized using breakouts containing particular blocks (the individual block-

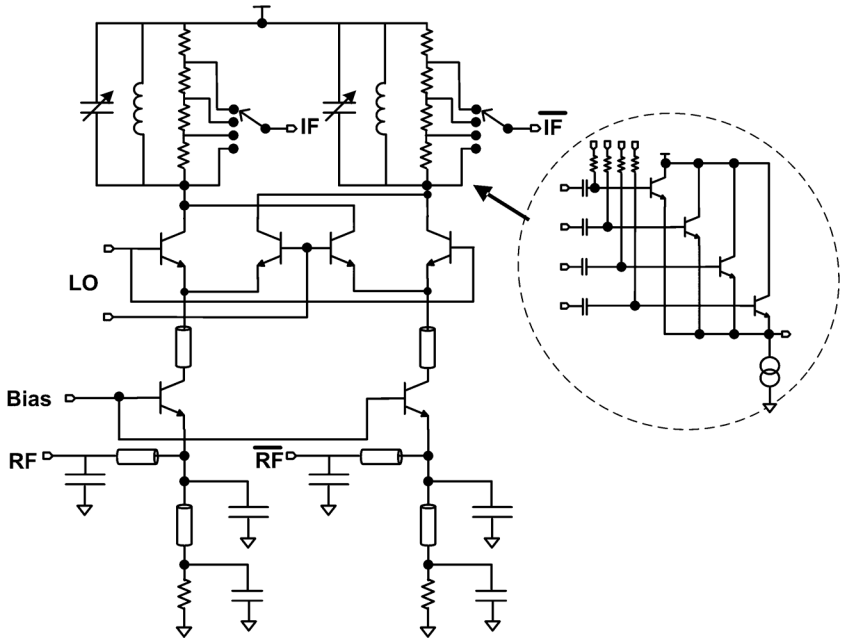

Fig. 11. Simplified schematic of the high-linearity RF-to-IF mixer, with an inset showing implementation of the multiplexer used in the output attenuator.

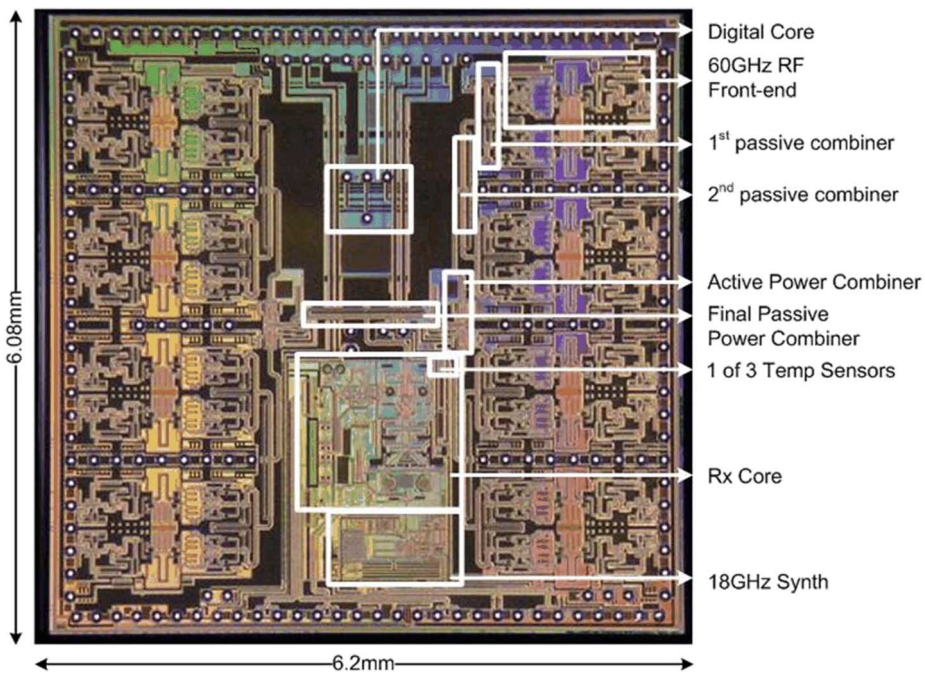

Fig. 12. Fully-integrated 60-GHz 16-element phased-array receiver implemented in IBM BiCMOS 8HP.

level measurements were described in Section III). In this section, on-wafer Rx IC measurements are presented.

Fig. 13 shows the Rx gain across frequency for the four IEEE channels. The gain is measured by providing an input to a single element and taking the output using the differential I signal. These four curves are swept-IF measurements, obtained for a constant LO frequency and varying RF frequency. Superimposed on this plot is the measured RF front-end frequency response, measured by varying RF and LO together to keep the IF signal frequency constant. The front-end gain is sufficiently broadband to cover all four channels of interest from 57.2 GHz to 65.9 GHz. The cascaded 9-GHz IF amplifier and baseband amplifiers result in a net channel bandwidth of ± 1 GHz.

The input and output compression points of the receiver across different gain settings are shown in Fig. 14. The data were obtained by performing $\mathrm{P}_{1\mathrm{dB}}$ compression measurements at each of the gain attenuation settings. The input power levels refer to a single input, but the compression is plotted based on calculations that assume that all 16 inputs are driven at the same power level; total input power from all 16 inputs is therefore 12 dB higher than shown. The measurements were carried out in IEEE channel 2 at 60.48 GHz, where the RX has the highest

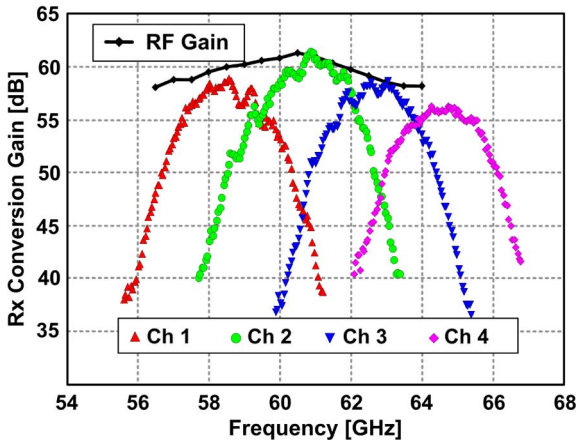

Fig. 13. Rx conversion gain in the four IEEE channels and performance of RF front-end.

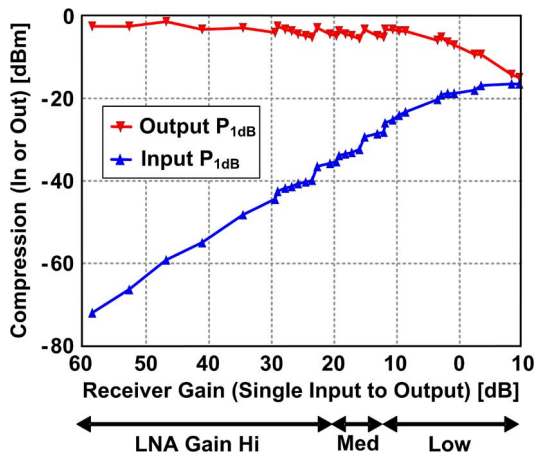

Fig. 14. Receiver input and output compression for different Rx gain settings.

gain and poorest compression performance. The RX has an input-referred compression point of -59 dBm @ 47 dB gain and -37 dBm @ 20 dB gain.

The RX IIP3 has been measured for both in-channel and adjacent-channel intermodulation. The in-channel IIP3 measurements are consistent with the RX compression characteristics presented in Fig. 14. Adjacent-channel measurements were performed by applying tones in channels 2 and 3 at 60.58 GHz and 62.74 GHz, and looking for intermodulation products appearing in channels 1 and 4. Such a measurement quantifies the receiver's ability to reject adjacent-channel interference in a multi-channel WPAN environment. The present receiver's adjacent-channel IIP3 is limited by the absence of explicit channel-select filters in the baseband. However, the limited bandwidth of the baseband amplifiers and IF-filters does provide 10–15 dB of adjacent-channel rejection. Fig. 15 shows an adjacent-channel IIP3 of -26.5 dBm with the Rx gain (single-input-to-output) set to 35 dB.

Fig. 16(a) shows the noise figure of the RF front-end across frequency and temperature. In the case of array noise measurements, the noise at the output of the array is estimated from noise figure measurements of front-end and downconversion chain breakouts, along with the noise figure measured when only one element is active. This noise figure is plotted in Fig. 16(b) for

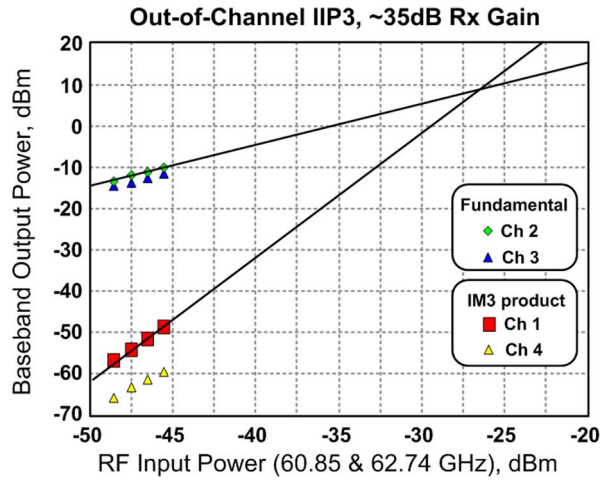

Fig. 15. Adjacent channel IIP3, measured by applying tones in channels 2 and 3, and looking for intermodulation products in channels 1 and 4.

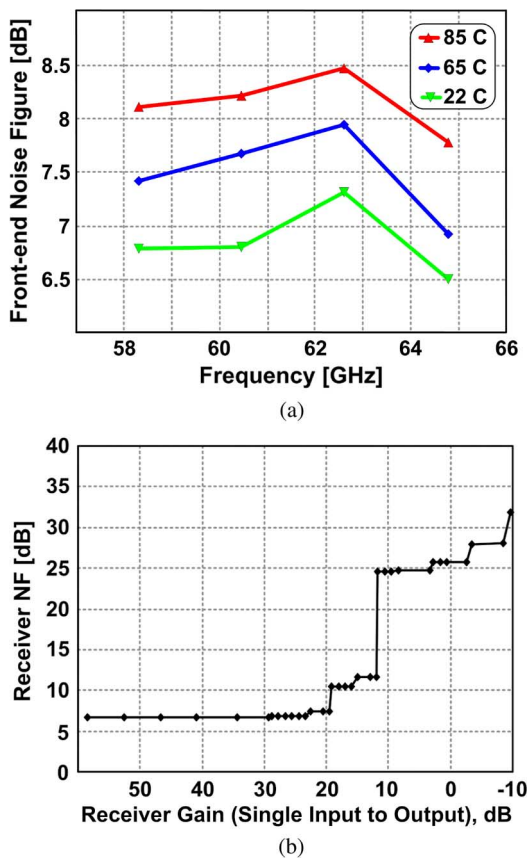

Fig. 16. (a) Noise figure of the 60-GHz RF front-end. (b) Receiver noise figure across gain settings.

different gain settings. The noise figure is 7.4 dB at the highest gain setting, and 11.6 dB when the receiver gain is set to 15 dB. Thus, both the range of gain and the location of the gain programmability allow the Rx array to operate under different gain, linearity and noise figure requirements. The dynamic range of the Rx array, under different gain conditions, can be determined from Fig. 14 and Fig. 16(b). Assuming 2 GHz noise bandwidth, the sensitivity at 30 dB Rx gain setting is ~ -86 dBm (assuming a 12 dB improvement in SNR) while the input-referred P_{1dB} is

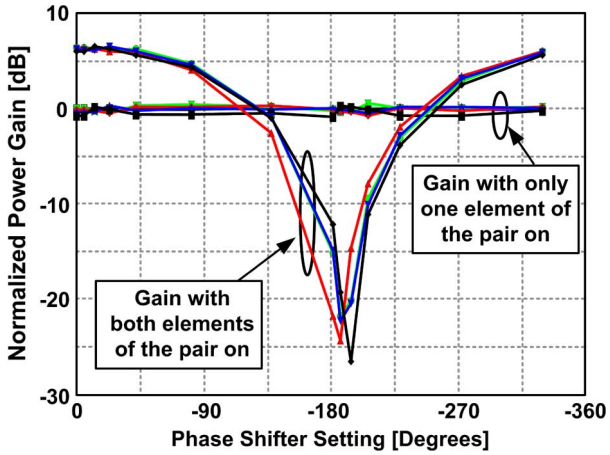

Fig. 17. Two-element array measurements at 60 GHz.

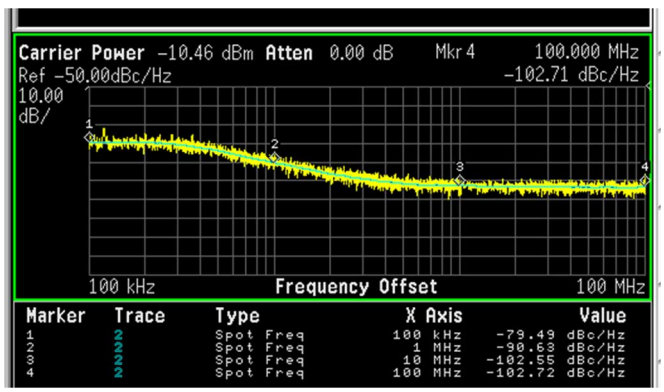

Fig. 18. Rx phase noise, taken in Channel 2 (60.48 GHz) with 60.38 GHz input signal at −57 dBm, resulting in 100 MHz output tone. Phase noise at 1 MHz offset is −90.6 dBc/Hz.

−44 dBm. Similarly, for Rx 10 dB gain setting, the sensitivity is −68 dBm and the input-referred P_{1dB} is −24 dBm.

Fig. 17 demonstrates the phase-shift and gain equalization performance of the array. In order to measure the phase-shift performance of the array, the elements are activated in pairs. The phase and gain setting of one element are kept constant while the phase of the other element is varied. Fig. 17 shows a measured 6 dB increase in output power when the signals from the elements add in phase. The signals are attenuated by more than 20 dB when the signals are combined out-of-phase.

The phase noise of the receiver was measured by providing a CW tone (at 60.38 GHz) to the receiver and measuring the phase noise of the baseband output (at 100 MHz). Fig. 18 shows the measured phase noise of −90 dBc/Hz at 1 MHz offset. Detailed measurements of the synthesizer are described in [14]. Measurements at phase shifter setting 31 (where the slope of the phase shift with respect to control voltage is high) and phase shifter setting 0 (where the slope of the phase shift with respect to control voltage is low) confirmed that array phase shift settings have no impact on the total phase noise.

The chip includes programmable phase rotators in the I and Q LO-path for the second downconversion that allow for compensation for IQ phase mismatch (Fig. 2). Independent gain control in the I and Q baseband amplifiers enable IQ gain mismatch compensation as well. Fig. 19 shows the measured IQ phase and gain mismatch for four different RX samples before and after compensation. The mismatch was measured at 10 MHz offset from carrier in each of the channel frequencies. The phase rotator and baseband amplifier gain settings that achieved lowest IQ mismatch varied from sample to sample.

TABLE I
RX POWER CONSUMPTION BY BLOCK (AT 2.7 V)

16 RF Frontends	900mW
2 Active Combiners	100mW
Receiver Core	250mW
Baseband 50Ω Output Buffers	280mW
Synthesizer	150mW
Frequency Tripler and LO Buffer	120mW
Total	1800mW

TABLE II
60-GHz PHASED-ARRAY RECEIVER PERFORMANCE SUMMARY

	Ch 1 58.32 G	Ch 2 60.48 G	Ch 3 62.64 G	Ch 4 64.80 G
Maximum Rx Gain	70 dB	71 dB	70 dB	68 dB
Front-end NF, max phase-shifter loss	6.8 dB	6.8 dB	7.3 dB	6.5 dB
Rx NF, max phase-shifter loss	7.4 dB	7.4 dB	7.9 dB	7.6 dB
iP_{1dB}, 0 dB Rx gain	-16 dBm			
oP_{1dB}, max. Rx gain	-1 dBm			
Phase tuning range, resolution	> 360°, 11.25° ± 4°			
IQ Gain and Phase Error	± 1 dB, ±1°			
Rx Phase Noise, 1MHz offset	< -90dBc/Hz			
Power 22°C, 65°C	1.8 W, 2.0 W (2.7V supply)			
Size, Device Count	6.08 x 6.2 mm^2 1.94k NPNs, 330K FETS			

Table I shows the total 1.8 W power consumption of the Rx broken down by block. Each of the 16 RF front-ends consumes about 57 mW, and the two active power combiners 50 mW each, for a total of 1.0 W in the RF front-end and power combining network. The frequency synthesizer consumes 150 mW, and the frequency tripler and associated LO buffer 120 mW. The Rx core (exclusive of the synthesizer and tripler) consumes 250 mW. Finally, the 50Ω matched output buffers for the differential I and Q baseband outputs consume a total of 280 mW. The phased-array receiver performance is summarized in Table II.

V. BOARD-LEVEL MEASUREMENTS OF PACKAGED RX IC

1) 60-GHz Antenna Testbed Measurements for Beam-steering: The 60-GHz RX array IC is packaged using both multilayer-organic (MLO) and LTCC packages that included 16 antennas [13]. Aperture-coupled patch antennas that included an air-cavity between the antenna and ground plane were used to achieve the desired 9 GHz of bandwidth and high efficiency. The measured input return loss of all 16 antennas is better than 10 dB in the band of interest. A detailed description of the 60-GHz patch antennas can be found in [26]. The MLO

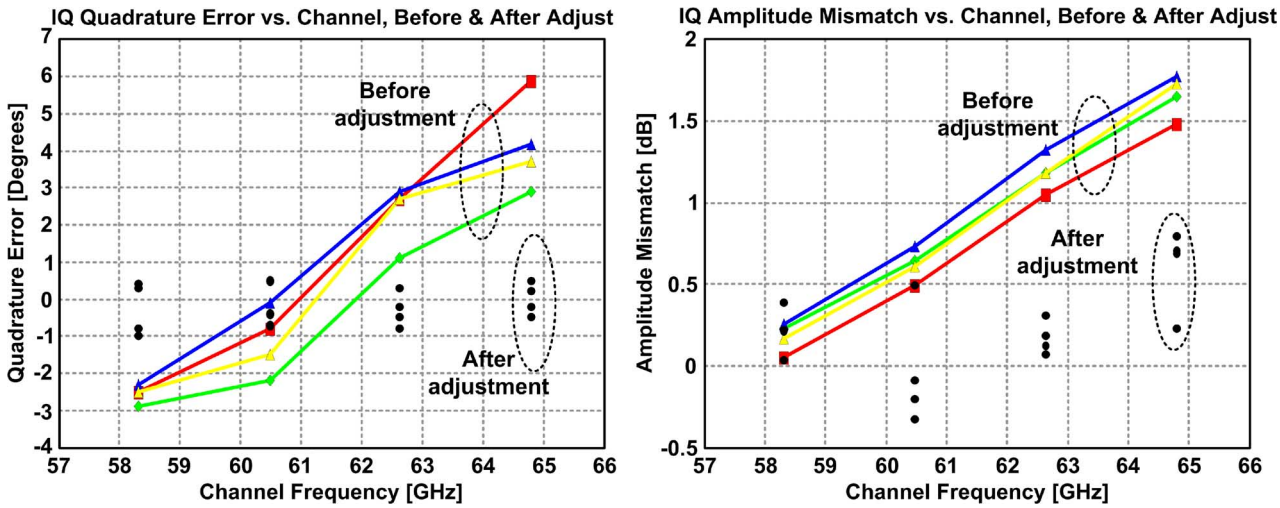

Fig. 19. Measured IQ phase and amplitude mismatch before and after on-chip compensation.

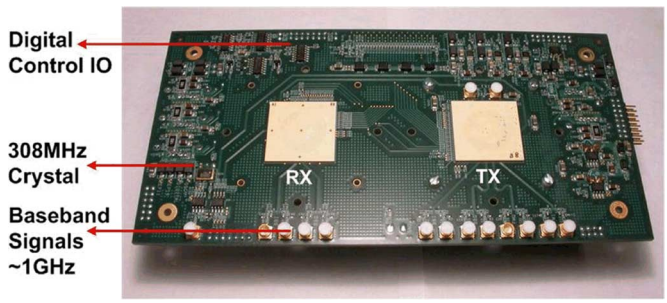

Fig. 20. Packaged phased-array receiver and transceiver on evaluation board. This board was used for pattern and link measurements.

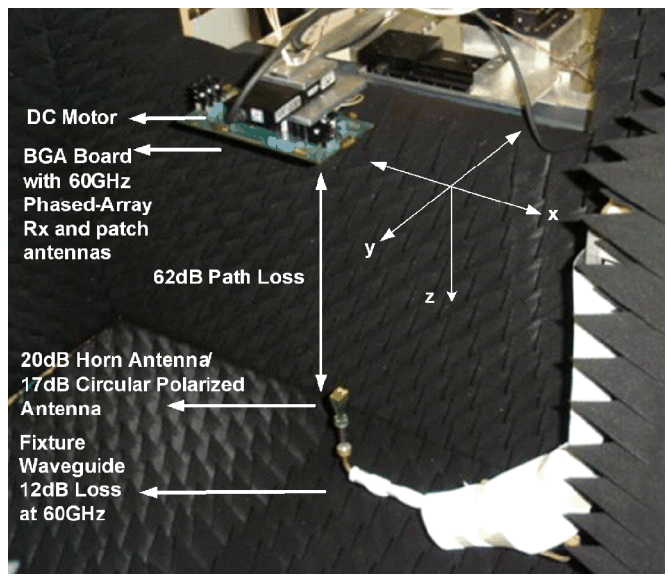

Fig. 21. 60-GHz antenna test chamber—the Rx array evaluation board can be rotated in θ and Φ for pattern measurements.

and LTCC packages include 60-GHz microstrip t-lines connecting the ICs to the patch antennas. The TX and RX ICs are attached to the packages using flip-chip technology. Each of the 28 mm x 28 mm 288-pin BGA packages is then attached to transceiver evaluation boards (Fig. 20). On-chip temperature sensors indicate that the IC temperature is $\sim 20^{\circ}$C higher than that of the environment. The packaged RX IC was tested in a 60-GHz antenna chamber that is capable of performing two-dimensional antenna pattern measurements (Fig. 21). The test-fixture loss was determined using S-parameter measurements and a path-loss exponent of 2 is assumed to determine the path loss between the board and the horn antenna (or circular-polarized antenna in the case of 2D pattern measurements). While on-wafer tests show insignificant gain and phase offsets between elements, the flip-chip interconnect and the 60-GHz traces on the package can introduce systematic phase offsets between elements. Furthermore, coupling between antennas leads to both antenna pattern and gain mismatch between elements (in the case of the RX LTCC antennas there is ± 2.5 dB variation in the antenna gain perpendicular to the array between the 16 antennas [13]). Gain and phase calibration of the packaged IC is done by orienting the array perpendicular to the antenna in the test-bed. In this position, gain offsets are calculated by measuring the elements one at a time and phase offsets are calculated by determining the null in the baseband output across phase shift settings with two elements on, as shown in Fig. 17.

Fig. 22 shows the improvement in output SNR as a function of number of active elements. In this measurement, the phased-array beam is pointed towards the horn antenna which is normal to the array. The phase settings of each element compensate for the offset measured in the calibration step, while the gain settings compensate for gain variation due to antenna coupling and phase shift setting. As expected, the output SNR increases as more elements are activated. Based on equation 5 in Section II-C, the SNR improvement is a function of the number of elements as well as the array efficiency factor, which increases with number of elements. Therefore, the expected SNR improvement with all 16 elements active (array efficiency: 0.95) relative to the case when only 1 element is active (array efficiency: 0.5), is 14.8 dB. Fig. 22 shows a 14.2 dB improvement

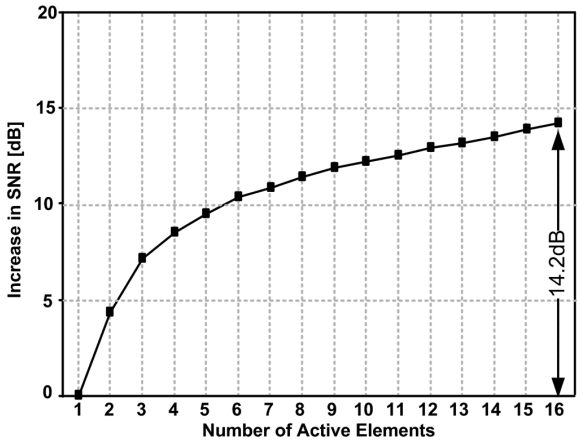

Fig. 22. Measured SNR as a function of number of active elements.

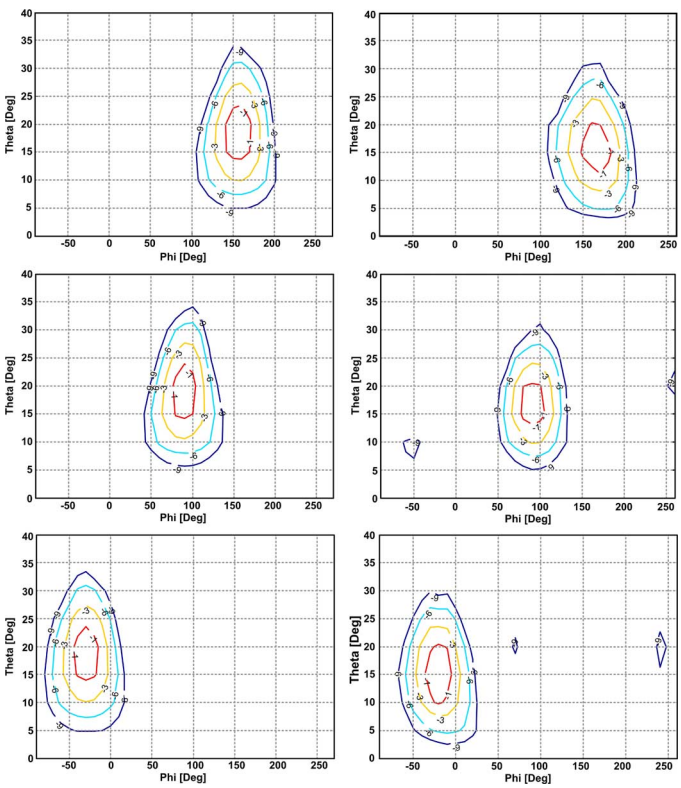

Fig. 23. Contour plots of theoretical and measured phased-array patterns show good correlation.

in SNR, showing >12 dB improvement as expected. The measured SNR improvement is limited by the mismatches between the antennas and the accuracy of gain calibration and phase offset compensation.

For beam pattern measurements, the element weights (gain and phase) necessary to achieve desired array patterns are calculated (taking gain and phase offsets into account) and applied to the packaged IC in the testbed. Fig. 23 shows the expected and measured 2D pattern measurements for different sets of element weights. The theta and phi coordinates in Fig. 23 are polar coordinates corresponding to the Cartesian coordinates in Fig. 21. Multiple antenna patterns corresponding to narrow as well as broad beams were measured and very good correlation was seen

Fig. 24. Measured phase-shifter transient response.

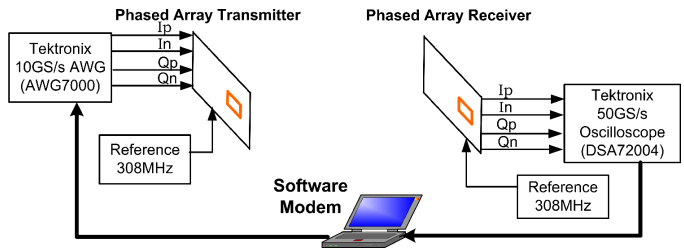

Fig. 25. Setup for 60-GHz link measurements using phased-array receiver and companion phased-array transmitter.

between the measurements and theoretical predictions, similar to the correlation shown in Fig. 23.

As discussed in the companion TX paper [6], the digital core can be read and written in serial and parallel I/O mode. To determine the response time of the chip to changes in phase and gain settings, a 60-GHz input is provided to two of the front-ends in the Rx IC. Fig. 24 shows the baseband output as the phase shifter in one of the elements is varied such that the signals first combine constructively and then destructively. The on-chip phase-shifter settings change at the rising edge of the Parallel I/O clock and it can be seen that the baseband output changes from high (constructive addition) to low (destructive addition) in 50 ns.

2) 60-GHz Wireless Link Measurements: Fig. 25(a) shows the 60-GHz wireless link measurement setup using the packaged phased-array RX and companion phased-array TX. In this setup, the digital baseband is implemented in software (MATLAB) and includes modulator, demodulator, forward error correction and carrier recovery. The link testing was done by creating data frames using the software, that were provided to the high-speed Arbitrary Waveform Generator (Tektronix AWG7000) which drives the I and Q inputs to the transmitter. The output of the receiver was sampled using a high-speed oscilloscope (Tektronix DSA72004) which emulates A/D converter. The captured frame was provided to the software demodulator which includes algorithms to correct for frequency offset between TX and RX. The link was evaluated using both 16-QAM OFDM (5.3 Gb/s) and Single-Carrier (4.5 Gb/s) modulation formats. Initial measurements on the link were performed with TX and RX 4 m apart (limited by laboratory space). Fig. 26 shows the constellations for 5.3 Gb/s OFDM

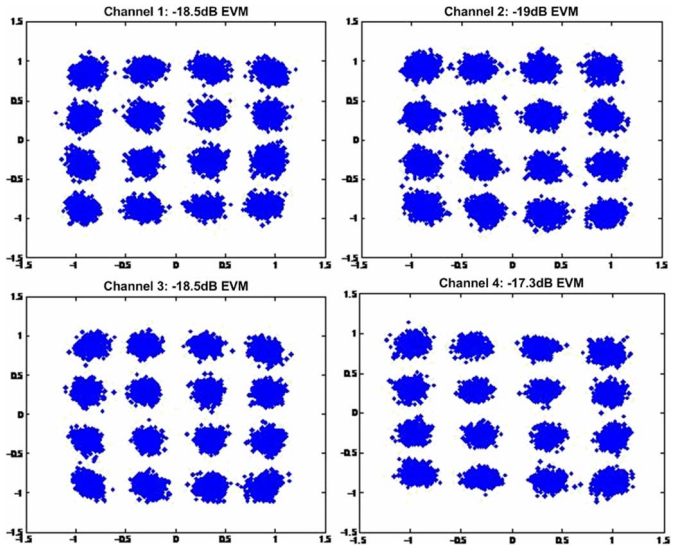

Fig. 26. Constellation in each of the IEEE channels for array Tx-array Rx wireless link. (OFDM modulation, 5.3 Gb/s, at 4 m Tx-Rx separation).

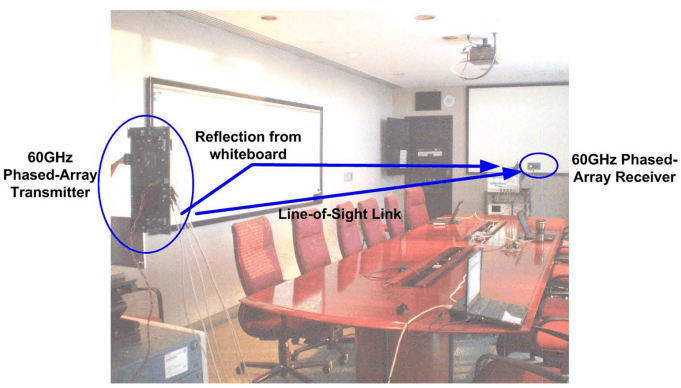

Fig. 27. 60-GHz wireless link in conference room—7.5 m to 8 m separation between TX and RX. Whiteboard is 2.2 m from the line-of-sight.

link in each of the four IEEE channels with 4 m TX-RX separation with only 6 TX elements and 12 RX elements activated [4]. The link shows lower than −18 dB EVM in channels 1, 2, and 3.

Fig. 27 shows the photograph of an experimental setup in a conference room with a whiteboard along one of the walls. During the line-of-sight tests, the TX and RX phased array beams are pointed at each other and for non-line-of-sight links, the beams are steered towards the whiteboard which acts as the reflector. The TX and RX were 7.5 m to 8 m apart and the distance to the reflector was 2.2 m. Fig. 28(a) shows the constellation for line-of-sight link with 5.3 Gb/s OFDM and 4.5 Gb/s SC modulations with all 16 elements active in the TX and RX. Fig. 28(b) shows the OFDM and SC constellations when the phased-array TX and RX beams are steered towards the whiteboard. In this case, the total path length is 9 m. The EVM in all cases was lower than −18 dB. The beam-steered links demonstrate the ability of the phased-array TX and RX to establish a 60-GHz link when the LOS is blocked.

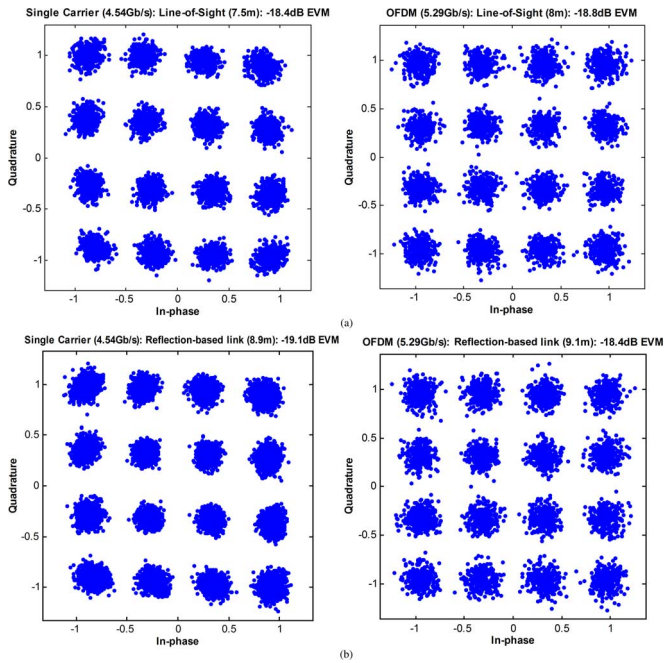

Fig. 28. Measured constellations for 60-GHz multi-Gb/s wireless links using phased-array TX and RX. (a) SC (4.54 Gb/s) and OFDM (5.29 Gb/s) line-of-sight links. (b) SC (4.54 Gb/s) and OFDM (5.29 Gb/s) NLOS link using reflection from whiteboard.

VI. Conclusion

A 16-element 60-GHz phased-array receiver was successfully implemented in a 0.12 μm SiGe BiCMOS process technology. RF-path phase shifting was adopted in the array, leading to reductions in area and power consumption. Each front-end uses a combination of active and passive phase-shifting to minimize phase shifter loss and ensure 360° of phase variation from 57 to 65 GHz with 11.25° phase step. The LNA and discrete phase shifter in the front-end also provide coarse and fine gain variation. The low variation in phase shift across process and temperature implies that each element can be set to desired phase-shift without any calibration for on-chip variations. The relative noise contributions of different array blocks was analyzed, and the RF signal combining network was designed using both passive and active combiners to improve output SNR. A differential cross-coupled Gysel combiner was implemented to reduce passive combiner loss and area. Each RF front-end has a NF of 6.8 dB at 22°C and 7.5 dB at 65°C. The array has 58 dB gain from single-element input to output at 60 GHz. There is extensive digital programmability on the chip and the gain can be varied from 58 dB to −10 dB. The phased-array receiver IC was packaged in LTCC and MLO packages that included 16 60-GHz antennas. Beam pattern and steering tests on the packaged receiver IC show good match between theory and measurements and the array is capable of switching beam directions in 50 ns. The packaged receiver was used in conjunction with the companion phased-array transmitter IC to demonstrate line-of-sight and reflection-based links capable of multi-Gb/s data transfer (5.3 Gb/s OFDM and 4.5 Gb/s SC).

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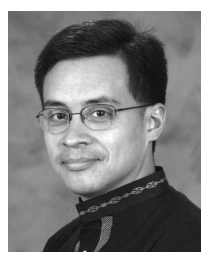

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