Nanoscale CMOS Transceiver Design in the 90–170-GHz Range

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***Abstract*—This paper reviews recent research conducted at the University of Toronto on the development of CMOS transceivers aimed at operation in the 90–170-GHz range. Unique nanoscale CMOS issues related to millimeter-wave circuit design in the 65-nm node and beyond are addressed with an emphasis on transistor and top-level layout issues, low-voltage circuit topologies, and design flow. A Doppler transceiver and two receivers fabricated in a 65-nm GPLP CMOS technology are described, along with a single pole, double throw antenna switch with better than 5-dB insertion loss and 25-dB isolation in the entire 110–170-GHz band. The first receiver has an IQ architecture with a fundamental frequency voltage-controlled oscillator, and is intended for wideband passive imaging applications at 100 GHz. The measured noise figure and downconversion gain are 7–8 and 10.5 dB, respectively, while the 3-dB bandwidth extends from 85 to 100 GHz. The second receiver has double-sideband architecture, operates in the 135–145-GHz range (the highest for CMOS receivers), and features an 8-dB gain LNA, a double-balanced Gilbert cell mixer, and a dipole antenna. The 90–94-GHz Doppler transceiver, the highest frequency reported to date in CMOS, is intended for the remote monitoring of respiratory functions. A Doppler shift of 30 Hz, produced by a slow-moving (4.8 cm/s) target located at a distance of 1 m, was measured with a transmitter output power of approximately $+2$ dBm and a phase noise of -90 dBc/Hz at 1 MHz offset. The range correlation effect is demonstrated for the first time in CMOS by measuring the phase noise of the received baseband signal at 10-Hz offset, clearly indicating that $1/f$ noise has been canceled and it does not pose a problem in short-range applications, where neither a phase-locked loop nor a frequency divider are needed.**

***Index Terms*—CMOS millimeter-wave integrated circuits (ICs), low-noise receivers, millimeter-wave imaging, millimeter-wave Doppler sensor, nanoscale MOSFETs.**

I. Introduction

FOR THE first time, with measured f_T/f_{MAX} values of 300 and 400 GHz for p-channel and n-channel devices [1], the speed of a 45-nm CMOS technology has become superior to that of all other semiconductor technologies in production. This has been accomplished despite the poorer transport properties of silicon, as a result of aggressive scaling, atomic layer deposition techniques, mechanical strain engineering, and the adoption of a larger number of compound materials than any III–V transistor technology. Beyond the 22-nm node, what we now call CMOS is expected to include both SiGe- and InAs-based heterostructures, feature cutoff and oscillation frequencies in excess of 500 GHz, and record low noise figure (NF), as required for products operating near 200 GHz. Furthermore, and most significantly, the fine geometrical control of nanoscale CMOS technologies provides the opportunity to introduce multibit frequency, phase, and amplitude control into every millimeter-wave circuit topology while maintaining a very compact layout, with little or no additional capacitive parasitics. This capability is not available to the same degree of precision in other competing millimeter-wave technologies such as coarser lithography SiGe BiCMOS or III–V technologies. It has the potential to revolutionize millimeter-wave ICs by providing a means for low-cost reconfigurability and on die, at speed self-test, self-calibration, and self-correction.

While the application space below 100 GHz is fairly well chartered, above 100 GHz, the picture is very sketchy. Possible applications include: 1) industrial sensors; 2) active imagers for biomedical applications; 3) passive imagers for remote sensing, night vision, security; and 4) 10–40 Gb/s wireless I/Os for chip-to-chip communication within 3-D electronic systems [2].

This paper addresses CMOS transceiver and receiver architectures, millimeter-wave IC design flow, and physical implementations at 90–170 GHz. Compared to [2], we have expanded the description of possible millimeter-wave transceiver architectures and the circuits inside the transceivers, added a millimeter-wave design flow and design issues section, a description of a new transceiver and Doppler effect demo at 93 GHz in CMOS, and demonstrate the highest frequency antenna switch in silicon operating over the entire D-band. The paper is organized as follows. Section II describes system architectures suitable for integration in nanoscale CMOS technologies. A discussion of the layout issues and the design flow for silicon ICs operating in the upper millimeter-wave portion of the spectrum follows in Sections III and IV, respectively. Examples of receivers and a Doppler transceiver are described in detail in Section V.

II. Transceiver Architectures

Active imaging transceivers are in many ways similar to those encountered in wireless data communication. In the transmitter,

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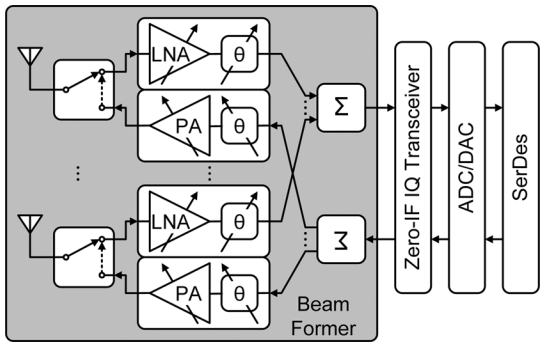

Fig. 1. Active imager/radio transceiver array with beam forming.

output power levels of 0–10 dBm, within the reach of nanoscale CMOS technologies, appear to be sufficient for short-range industrial and biomedical sensors [3].

One of the more sophisticated architectures that become economically feasible for single-chip integration in CMOS at frequencies above 100 GHz is illustrated in Fig. 1. It features a multilane transceiver beamformer with gain control, 360° phase control, and individual loop back in each transceiver lane. The latter is critical for large-volume inexpensive on-chip self-test, and is made possible by a three-way antenna switch. A dc to 110-GHz variable gain attenuator and antenna switch with less than 1.6-dB loss and over 28-dB isolation at 94 GHz has been already demonstrated in a 65-nm CMOS [4]. Simulations indicate that it can be readily scaled to 200 GHz in more advanced CMOS nodes. Furthermore, in Section V, a D-band single pole, double throw (SPDT) switch designed and fabricated in the 65-nm CMOS will be described. This wireless system architecture, with separate transmit and receive antennas and without loop back, is apparently already implemented in a 60-GHz high-definition multimedia interface (HDMI) wireless video area network (WVAN) CMOS product [5].

For precise remote detection of low-velocity movement ($v <$ 1 cm/s) and position, such as the patients' breathing, pulse [3], and other more complex cardiorespiratory functions, the array in Fig. 1 needs to operate in a frequency-modulated continuous-wave (FMCW) mode only, with a simplified double-sideband zero-IF receiver. In this application scenario, as (1) and (2) indicate, detection of small Doppler shifts Δf_d, in the hertz range, and changes in position, Δr, of a few millimeters at a distance r of a few meters, are of particular interest

$$v = \frac{c\Delta f_d}{2f_{\rm OSC}} \tag{1}$$

$$r = \frac{1}{2}c\tau = \frac{c\Delta f_d T}{2\Delta f_{\rm OSC}} \tag{2}$$

where c is the speed of light, τ is the time-of-flight delay of the signal to the target and back, $f_{\rm OSC}$ is the transceiver frequency, $\Delta f_{\rm OSC}$ is the tuning range of the transmit frequency, and T is the repetition period of the saw-tooth signal that is typically applied at the control node of the voltage-controlled oscillator (VCO).

In an FMCW transceiver, the VCO frequency is swept over $\Delta f_{\rm OSC}$ during period T. From (1) and (2), it is immediately apparent that transceiver array operation above 100 GHz and a large tuning range are beneficial for improving the precision with which velocity and position are detected, while beamforming can help in removing ambiguity due to motion artifacts and identifying the direction of movement and location. The transmit-receive link budget and phase noise are important in resolving fine Doppler shifts. The received signal power must rise above the phase noise level $L(\Delta f_d)$ of the VCO at the offset frequency Δf_d when it reaches the mixer. This is concisely captured by the radar equation

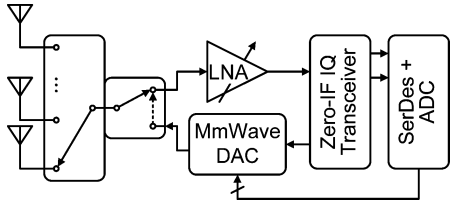

Fig. 2. Switched-antenna, active imager/radio transceiver.

$$L(\Delta f_d) \le 10\log_{10}\left(\frac{\lambda^2\sigma G_{\rm PA}G_{\rm TX}G_{\rm RX}G_{\rm LNA}}{(4\pi)^3 r^4}\right) \tag{3}$$

where $G_{\rm PA}, G_{\rm TX}, G_{\rm RX}$, and $G_{\rm LNA}$ are the gains of the power amplifier (PA), transmit antenna, receive antenna, and LNA, respectively, and σ is the radar cross section of the target.

For example, in a system with a combined LNA and PA gain of 20 dB, 25-dB antenna gain, a VCO center frequency $f_{\rm OSC} =$ 100 GHz, a tuning range $\Delta f_{\rm OSC} = 5$ GHz, and a sweeping time of 10 ms, a moving target with a velocity of 1 cm/s and a cross section of 0.1 m^2 results in a 6.6-Hz Doppler shift. If this is to be detected at a distance of 1 m, then the overall phase noise of the transmit-receive link must be better than -23.4 dBc/Hz at 6.6-Hz offset. The same Doppler frequency shift ensures a displacement measurement accuracy of 2 mm at a distance of 1 m.

In a Doppler radar, partial phase noise cancelation occurs over short distances due to range correlation [6]. Therefore, in some velocity-detection applications, no PLL and divider chain may be required to "tether" the VCO frequency to a stable reference. This also becomes possible in the case of precise position detection if the transceiver VCO can be realized as a digitally controlled oscillator (DCO), with precisely controlled tuning curve, leading to considerable power savings associated with a 100+-GHz divider chain.

A significantly lower power transceiver based on switched antennas and direct modulation at millimeter waves [1] is illustrated in Fig. 2. Although electronic beam-steering or a "zoom-in" function are not possible with this architecture, when properly oriented, the multiple antennas allow communication, remote monitoring, or imaging in virtually all directions, with only a small penalty in NF and output power compared to the transceiver in Fig. 1.

Perhaps the most attractive application for CMOS is in portable passive imaging cameras for low-visibility conditions [7]. A typical system, shown in Fig. 3, similar to a video camera, requires massive integration levels of millions of pixels, achievable only in CMOS technology. Its temperature

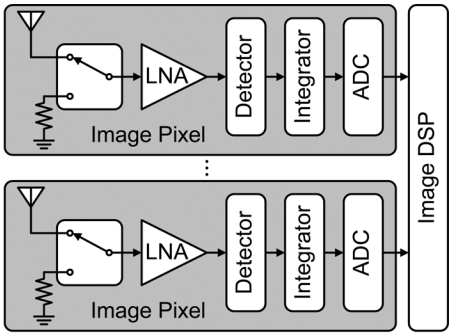

Fig. 3. Traditional detector array for passive imaging [7].

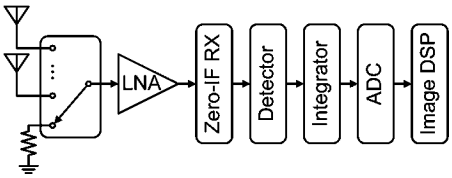

Fig. 4. Switched-beam zero-IF receiver architecture for passive imaging.

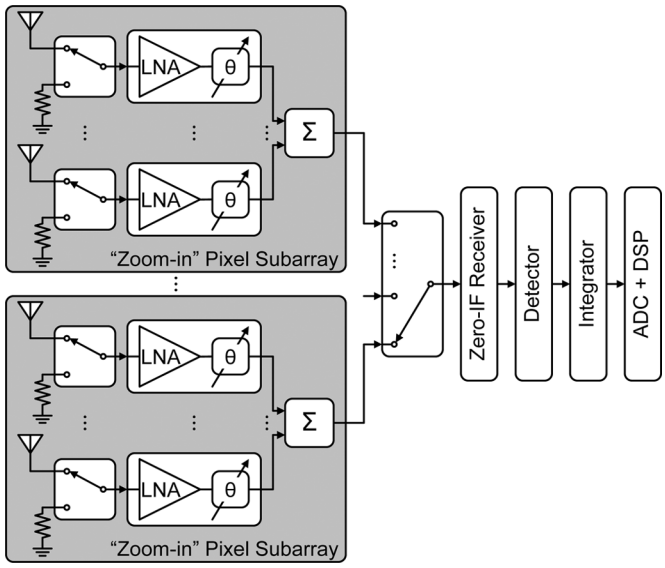

Fig. 5. Switched-beam zero-IF receiver architecture for passive imaging with zoom-in capability.

resolution ΔT should be lower than 0.5 K and is given by the following equation:

$$\Delta T = 2(T_B + T_R)\sqrt{\frac{1}{B\tau_i} + \left(\frac{\Delta G}{G}\right)^2} \tag{4}$$

where T_B is the brightness temperature of the object, T_R is the receiver noise temperature, B is the 3-dB bandwidth of the receiver, τ_i is the integration time of the baseband integrator, and G and ΔG are the gain and the rms short-term gain variations of the LNA [8]. The factor of 2 arises from the fact that half of the integration time is used for calibration.

The low receiver noise temperature (<600 K), high gain (>30 dB) and gain stability, large bandwidth (>10 GHz), and low power are formidable challenges for nanoscale CMOS at frequencies above 90 GHz [9]. Here too, by cleverly exploiting new architectures based on switched antennas (Fig. 4) and downconversion, power dissipation can be reduced, and gain and NF can be more judiciously partitioned.

Fig. 5 combines the beamformer concept with passive imaging to illustrate how "zoom-in" functions could be added to a moderate power, night-vision, and all-weather camera. At 150 GHz and above, the distance between antennas, 1.5 mm or lower, becomes comparable to the physical width of a transceiver lane. This makes it possible to integrate a massive 30 000 pixel array at the 300-mm wafer scale. The array could consume less than 10 W when groups of 300 pixels are electronically scanned every 20–30 ms.

Finally, to conclude the discussion on architectures, it should be noted that it is possible to combine the Doppler sensor, radio, and radiometer functions in a single transceiver (array). Not only does this make sense from a technical (the Doppler function is ideal for self-test) and application perspective (i.e., assume that we want to monitor a patient's/infant's temperature and cardiorespiratory functions remotely and transmit the collected information to a base station), but is also imposed by the economics of 32-nm CMOS fabrication. Few companies and few millimeter-wave products have the volumes, and can justify the cost of multiple fabrication runs and mask sets at over 2 million dollars per production tapeout.

III. Nanoscale Technology Design Issues in the Upper Millimeter-Wave Spectrum (90–300 GHz)

During the last three years, a number of publications have addressed the characterization and scaling of inductors, transformers, varactors, [10], [11], and low-voltage single-transistor-stacked topologies [12], [13]. They indicate that nanoscale millimeter-wave CMOS ICs, not unlike today's 2–6-GHz ones, could be scaled in performance and reduced in size to operate at 200 GHz, and made insensitive to bias current, supply voltage, and threshold voltage variation if n-MOSFETs are biased at drain current densities of 0.2–0.5 mA/μm. In this region of operation, $\mathrm{NF}_{\mathrm{MIN}}, g_m, f_T, f_{\mathrm{MAX}}, C_{gs}$, and C_{gd} are practically bias independent, and reach their optimal values in all technology nodes and foundries [14]. While this bodes well for the yield of millimeter-wave CMOS ICs, how are important functions such as gain and phase control, and digital calibration of analog blocks going to be implemented if high-frequency performance becomes insensitive to bias current and supply voltage?

A possible solution is to build on the foundations of "digital-RF" [15] and segment and group the gates of the interdigitated transistors [4] and differential pairs in a binary-weighted fashion, while keeping the source and drain nodes connected together. This approach, illustrated in Fig. 6 and which contributes little additional layout parasitics at the high-frequency nodes, allows for digital control voltages to be applied directly to the individual gate fingers of MOSFETs [4], MOSFET differential pairs, or MOSFET Gilbert cells. Essentially, in this unique-to-CMOS technique, every millimeter-wave circuit becomes a segmented or binary-weighted millimter-wave digital-to-analog converter (DAC). MOSFET channel slices biased at the optimal operating point (e.g., minimum NF bias current density in LNAs, peak linearity bias in PAs) are either turned on or off.

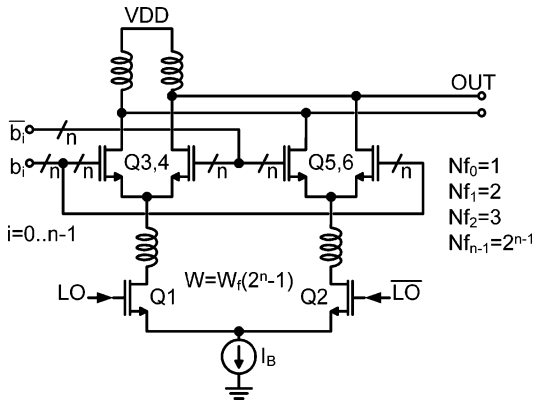

Fig. 6. Binary-weighted Gilbert-cell stage to be used as optimally biased millimeter-wave DAC or VGA.

For the binary-weighted variable gain amplifier (VGA)/DAC in Fig. 6, which consists of n binary-weighted Gilbert-cell multipliers with $1, 2, \ldots, 2^{n-1}$ gates, the expression of the voltage gain becomes

$$A_V = -g_m' W_f Z_L \sum_{i=0}^{n-1} (-1)^{b_i} 2^i \tag{5}$$

where g_m' is the MOSFET transconductance per unit gate width, W_f is the finger width, and $b_i = 0$ or 1.

It should be immediately apparent that this concept, already demonstrated in attenuators and switches [4], can be extended to millimeter-wave inphase-quadrature (IQ) modulators and digitally tuned phase rotators [16].

Although most of the millimeter-wave performance parameters improve in advanced CMOS nodes, layout parasitics become increasingly dominant. Of all high-frequency devices, the MOSFET is the most sensitive to resistive and capacitive parasitics. Layout design becomes the big differentiator in the performance of millimeter-wave CMOS circuits with identical schematics, component size, and bias point. Interdigitated differential MOSFET pairs and mixing quad layouts, for which typically there are no RF models, have been shown to produce more than 50% speed improvement in the performance of static dividers with otherwise identical transistor sizes and layout [17].

While gate resistance and parasitic capacitance have long been known to degrade MOSFET power gain and NF performance at RF frequencies, starting at the 65-nm node, dc source resistance and top-level ground resistance have become just as important and even more harmful. Source and ground resistances affect the dc g_m, and the HF current gain, power gain, and NF. Since via and contact resistances increase with the square of the technology scaling factor, and accurate transistor-level simulation with full *R–C* extraction is not feasible at the receiver or transceiver level at millimeter-wave frequencies, its impact is only going to be exacerbated in the 45- and 32-nm nodes, but will be difficult to estimate in the design phase.

One method to alleviate this problem is to employ differential topologies in all circuits. As illustrated in Fig. 7, in an interdigitated MOSFET differential pair, most of the source contact

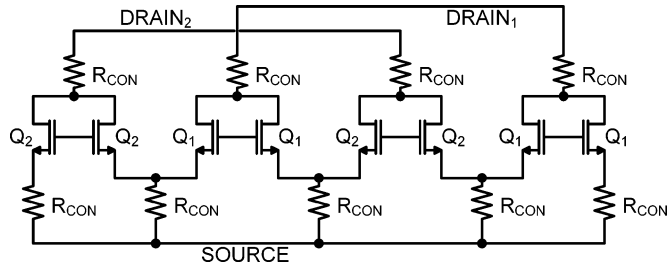

Fig. 7. Series resistive parasitics in a differential pair.

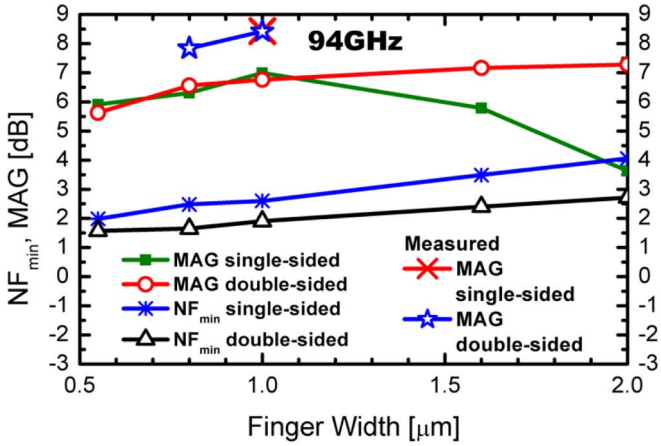

Fig. 8. Simulated gate finger width and gate contact geometry impact on the 65-nm GP MOSFET MAG and $\mathrm{NF_{MIN}}$ at 94 GHz. The measured MAG data for two MOSFET gate geometries at 94 GHz are also included.

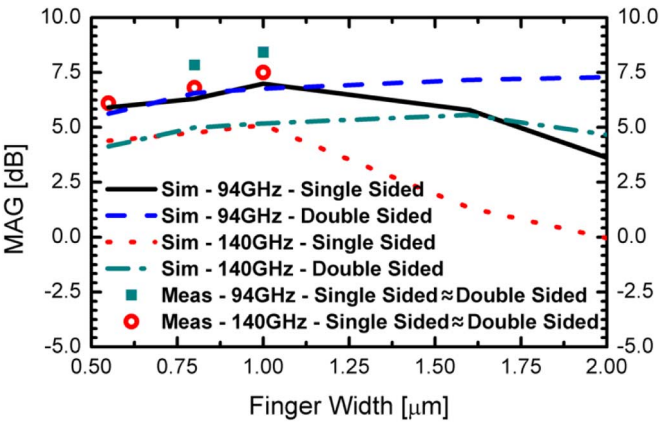

Fig. 9. Comparison of simulated gate finger width and contact geometry impact on MAG at 94 and 140 GHz.

resistance appears in common mode, and will not degrade gain and NF in differential mode.

Figs. 8 and 9 show another aspect of millimeter-wave MOSFET layout design. It has been observed in the simulated maximum available gain (MAG), minimum NF $(\mathrm{NF_{MIN}})$, and current gain $(\mathrm{H_{21}})$ after extraction of layout *R--C* parasitics that the optimal gate finger contact geometry and gate finger width depend on frequency. Furthermore, MAG, $\mathrm{H_{21}}$, and $\mathrm{NF_{MIN}}$ experience different dependencies on gate layout geometry and frequency. Measurements of transistor MAG at 94 GHz seem to confirm the simulation results.

We note that MAG is higher for single gate contact geometries for gate finger widths below 1 μm at 94 GHz, whereas at 140 GHz, double-sided gate contact provides higher gain for finger widths exceeding 0.8 μm. This information is important in PA design. In contrast, $\mathrm{NF_{MIN}}$ is always the best for double-sided gate contacts, which calls for a different transistor gate geometry in LNAs and VCOs. As a consequence of these simulation results, different transistor layouts and finger widths were employed in the design of the 94- and 140-GHz circuits, respectively, as discussed in Section V.

Most foundries typically provide RF MOSFET models for a restricted set of geometries, e.g., CS only, and only for the LP flavor of the technology. The latter does not provide the best millimeter-wave performance. Interdigitated layouts, needed in Gilbert-cells and latches to minimize parasitics and maximize operation frequency, are normally not supported by RF models. If only "RF" layouts were to be used to ensure model accuracy, interconnect would have to be added in a Gilbert cell, latch, etc. This can degrade circuit performance by as much as 50% [15]. Hence, the millimeter-wave CMOS circuit designer is faced with the dilemma: use accurate "RF" models and expect performance degradation (often as drastic as the equivalent of a backward move to an earlier node), or use "digital" models, but save circuit performance by relying on common-sense layout geometries that minimize the total circuit footprint.

IV. Millimeter-Wave Design Flow

The following design flow has been found to work reasonably well over many tapeouts of millimeter-wave circuits with moderate levels of integration in 90-, 65-, and 45-nm CMOS and 130-nm SiGe BiCMOS technologies.

1) Transistor level schematic (hand) design using the RF models as proof of concept for the transceiver architecture. Transistor sizes and bias currents are set at this stage in the design process.
2) Transistor layout and *R–C* extraction. Different transistor layouts are typically drawn for the following.
   a) Common-source stages with inductive degeneration.
   b) Grounded common-source stages.
   c) Common-gate.
   d) Latch.
   e) Gilbert cell.
   f) VCO.
   g) Differential pairs.
3) Schematic design with extracted transistors.
   a) Inductor, transformer, and capacitor values are obtained at this stage.
   b) Extracted transistors and simple *R-L-k* inductor and transformer models are employed in all simulations. Extracted transistor parasitics of the layouts listed in step 2 are added to digital transistor models (rather than RF models that are limited to SC configuration).
4) Top-level layout floor plan.
5) Inductor and transformer designs.
   a) Use 2-D/3-D EM field simulator to generate Y-parameters versus frequency from which 2-π equivalent circuits are extracted for inductors and transformers.
   b) ***Note***: More than 30 different inductors and transformers, often with several design iterations, are typically needed for a transceiver.
6) Resimulate transceiver top level and building blocks.
   a) Layout each cell.
   b) Extract *R–C* parasitics of the entire cell, without double counting for inductor/transformer parasitics that have been modeled as 2-π circuits elsewhere.
   c) Model interconnect as (coupled) lossy lines.
   d) Redesign/add passives as necessary to improve interblock matching.
7) Resimulate, redesign, and remodel inductors and transformers as necessary.
8) Layout top level.
   a) Model interconnect as (coupled) lossy lines.
   b) Redesign/add passives as necessary to improve interblock matching.

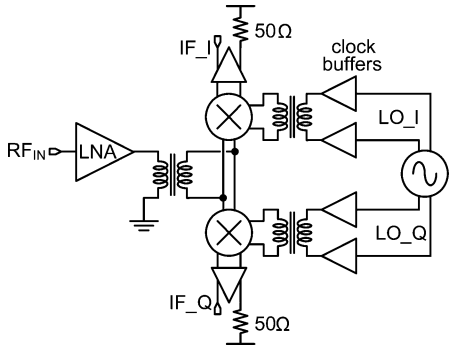

Fig. 10. Block diagram of the 90–100-GHz IQ receiver.

V. Receiver and Transceiver Examples

All circuits described next were fabricated in a 65-nm GPLP process with a seven-metal digital back end. GP stands for general purpose MOSFETs with an oxide thickness of approximately 1.25 nm and minimum physical gate length of approximately 45 nm, while LP describes low-power transistors with an oxide thickness of 1.8 nm and a minimum physical gate length of approximately 60 nm. Both GP and LP devices are available on the same die. GP MOSFETs are rated for 1.1 V and have lower threshold voltages, lower NF, and higher transconductance, current and power gain than LP MOSFETs. The measured maximum available gain for a GP n-MOSFET biased at a V_{DS} of 1 V is 8.4 dB at 94 GHz. LP MOSFETs are rated for 1.2-V operation.

A. 100-GHz IQ Receiver

Fig. 10 shows the block diagram of an 85–100-GHz IQ receiver designed for passive imaging applications. It features a modified version of the transformer-feedback LNA in [18], centered at 94 GHz, a double-balanced, Gilbert-cell IQ mixer (Figs. 11 and 12) two IF amplifiers, and a quadrature VCO with single-ended LO buffers. Three 1:1 transformers have been employed for single-ended to differential conversion at the output of the LNA, and also between the LO buffers and the mixer. The receiver, whose die photograph is shown in Fig. 13,

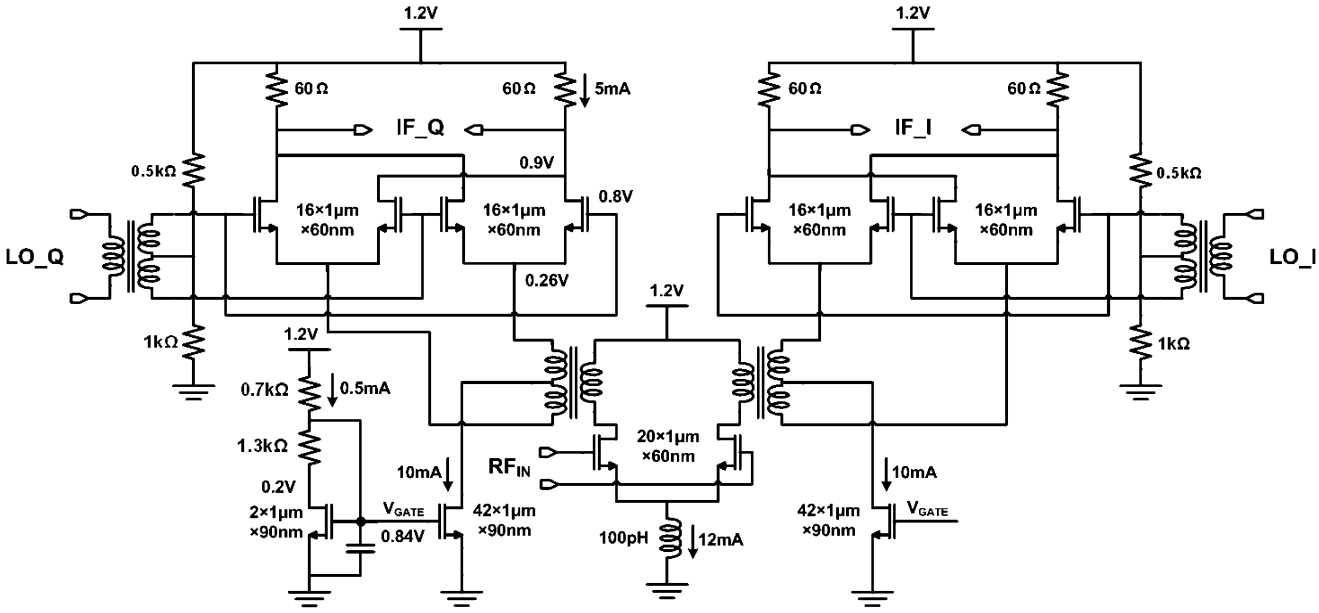

Fig. 11. Schematic of the 100-GHz IQ mixer.

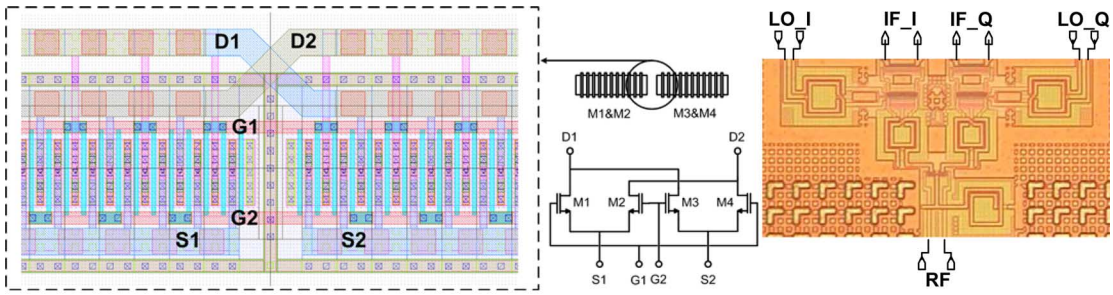

Fig. 12. Layout detail and die photomicrograph of the IQ mixer.

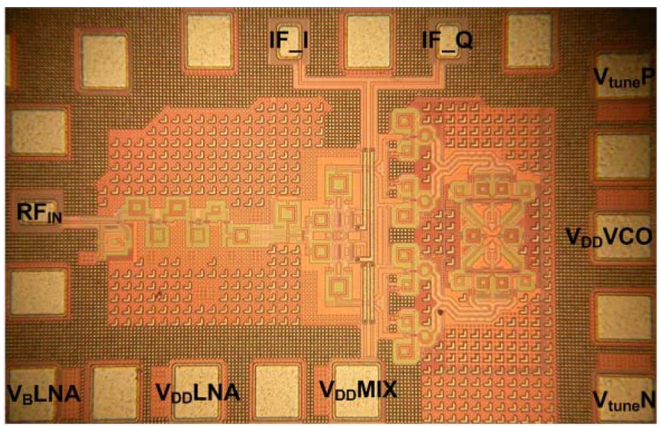

Fig. 13. Die photograph of the 85–100-GHz IQ receiver.

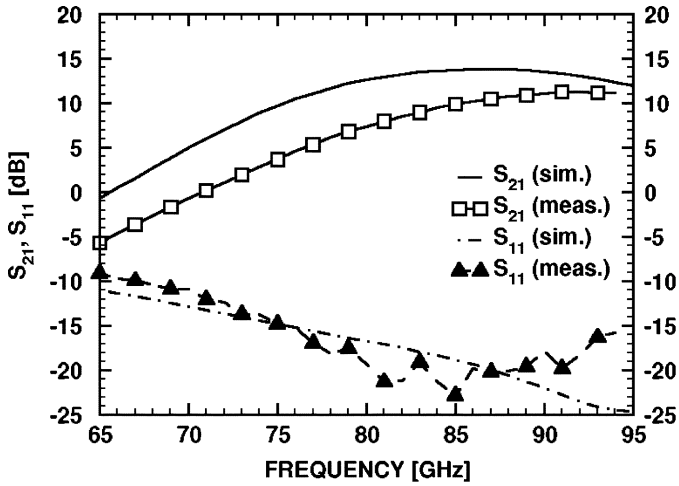

Fig. 14. Comparison of measured verses simulated LNA S_{11} and S_{21} at 1.2-V supply.

operates from 1.2-V supply, consumes 208 mW, and occupies 800 μm $\times$ 510 μm, including all pads.

To reduce mismatches in the IQ mixer and maintain the correct phase relationships between the four LO signals, the transistors in the mixer quads are laid out as a single interdigitated device. The connection of the gates, sources, and drains of the quad is illustrated in Fig. 12. A layout detail of the IQ mixer demonstrates its symmetry and the signal flow.

Measurements of the LNA breakout show a gain of 11 dB and S_{11} better that -15 dB up to 94 GHz (Fig. 14). The LNA

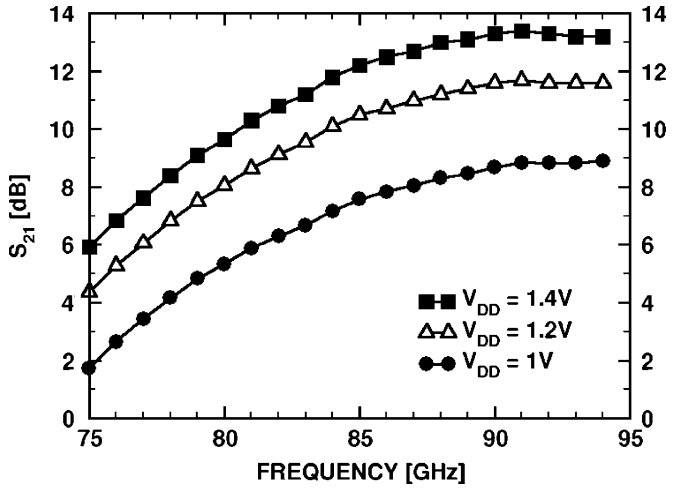

Fig. 15. Measured LNA gain versus $V_{\rm DD}$.

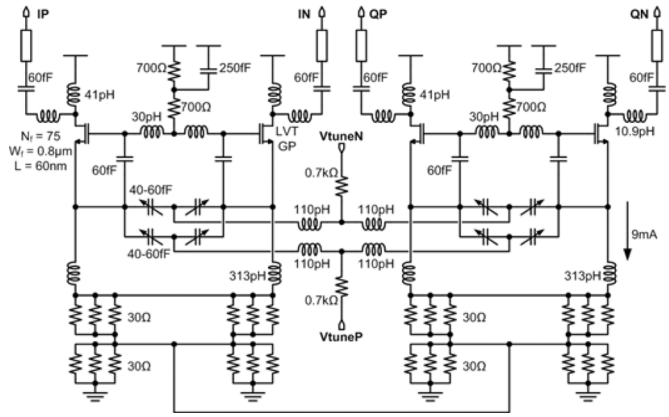

Fig. 16. Quadrature VCO schematic.

gain drops to 9 dB for a 1-V supply and increases to 13 dB when a 1.4-V supply (Fig. 15) is employed. As with all circuits described here, due to probe contact and cable resistance, the actual supply voltage at the bias pad is typically 0.1 V lower than the values indicated in the plots that represent the readings on the display of the power supply. Nevertheless, it is important to note that, because telescopic cascodes are employed, the sensitivity to $V_{\rm DD}$ variations is larger than in LNAs employing ac-coupled cascodes [13].

The schematic of the VCO employed in this receiver is shown in Fig. 16, and is based on the design described in [19]. The VCO is composed of four Colpitts suboscillators. Each pair of suboscillators oscillates differentially due the resistors that are common to the pair. Similarly, the two pairs are coupled in quadrature through resistors at the node that is common to all four suboscillators. A fourth-harmonic signal (which is around 400 GHz) is produced at this node, but not used in this application. To prevent load pulling, the VCO is followed by four identical common-source (CS) tuned buffers. To achieve higher output power, the active devices in the buffers are biased at 0.3 mA/μm.

To minimize the phase noise of the VCO, parasitic resistances must be reduced to a minimum in all active and passive components. Thus, the tank inductor was implemented as a line in-

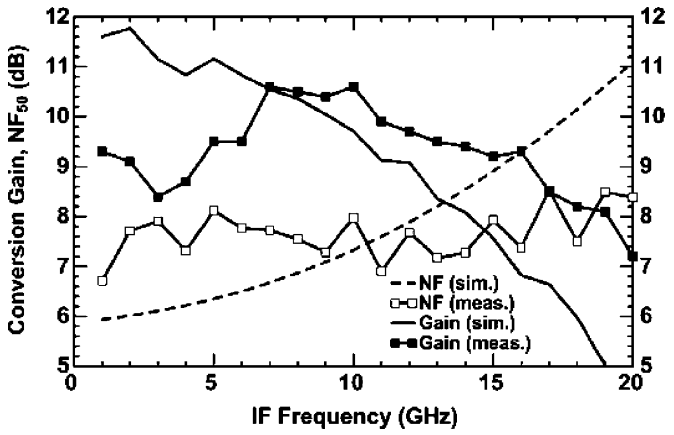

Fig. 17. Measured (lines and symbols) and simulated (lines only) receiver conversion gain and NF with the VCO at 99 GHz.

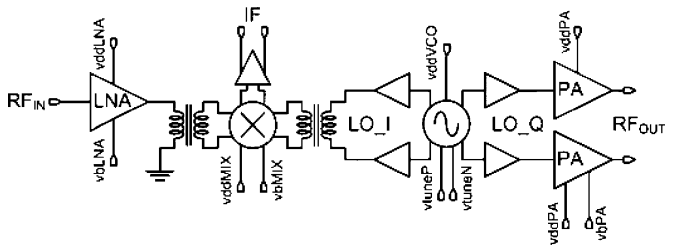

Fig. 18. 94-GHz CMOS Doppler transceiver.

ductor, which has higher Q then a spiral inductor. Furthermore, all transistors and varactors have been laid out with finger width of 0.8 μm and all gates have been contacted on both sides to reduce the gate resistance. MOSFETs in the VCO core are biased at a low-noise current density of 0.2 mA/μm.

The measured VCO tuning range extends from 97.2 to 101.2 GHz. The differential downconversion gain and double-sideband NF of the receiver are plotted versus IF frequency in Fig. 17 for a 1.2-V supply, with the LO frequency set to 99 GHz. A peak gain of 10.5 dB was achieved and the NF varies from 6.7 to 8.5 dB over the entire 3-dB gain bandwidth of 85–100 GHz. The measured conversion gain and NF of the IQ receiver differs by 1–2 dB from simulation due to the double-sideband nature of the circuit and the fact that the measurement equipment assumes equal gain for both bands.

B. 94-GHz Doppler Transceiver

The block diagram of the double-sideband Doppler transceiver is shown in Fig. 18. The transceiver employs the same quadrature VCO, LNA, and doubly balanced Gilbert-cell mixer as in [19], and also features two PAs for possible transmitter beam steering. With the help of the quadrature VCO that produces four fundamental frequency signals simultaneously at 90–94 GHz, the LO signal distribution is easily achieved without the need for an LO tree. The schematic of the PA is described in Fig. 19. It features two telescopic cascode stages at the input and an ac-coupled cascode at the output. The last common-gate (CG) transistor is an LP MOSFET to ensure reliable operation with large output voltage swing from 1.2-V supply. A breakout of the PA was characterized separately.

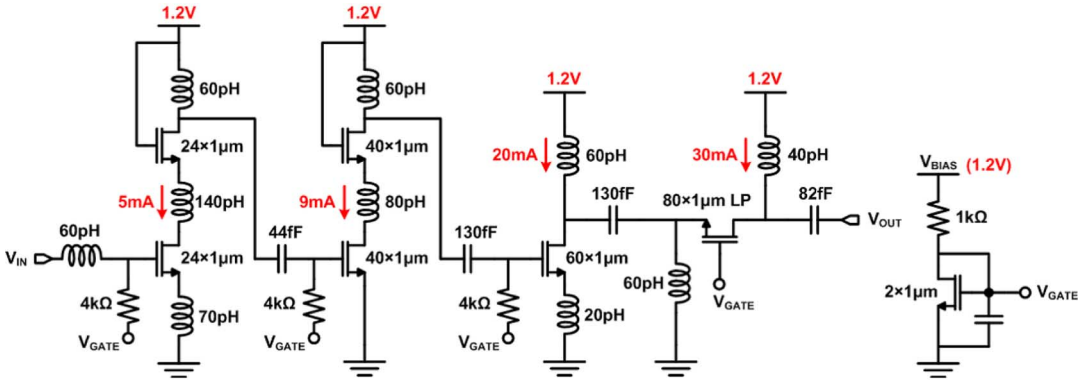

Fig. 19. 94-GHz PA schematics.

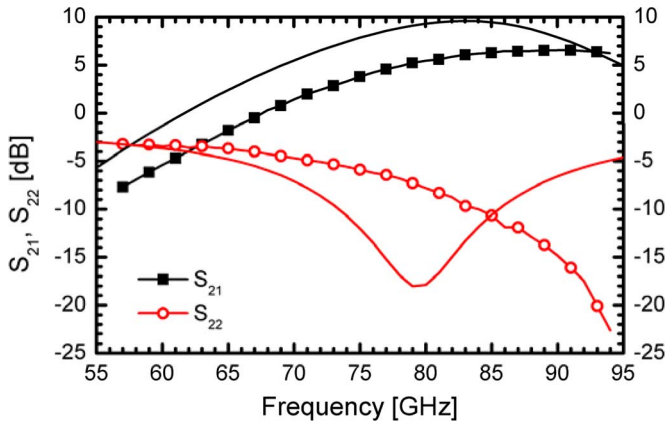

Fig. 20. Measured (lines and symbols) versus simulated (lines only) small signal gain and output return loss of the PA breakout.

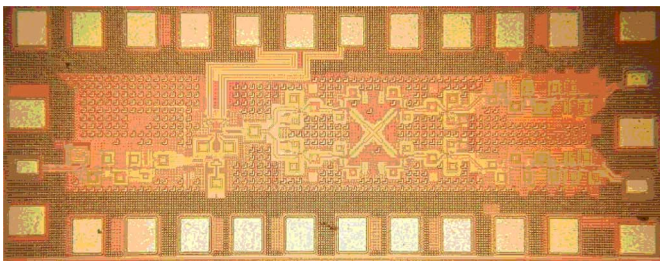

Fig. 21. Die photograph of the 94-GHz CMOS Doppler transceiver. The total chip area is 0.4 mm × 1.2 mm, including pads.

The measured and simulated S-parameters are compared in Fig. 20. Discrepancies are due to inaccurate modeling of inductors and pessimistic parasitic extraction at design time. The measured peak gain of 7 dB is centered at 90 GHz and the 3-dB bandwidth extends from 76 GHz beyond the vector network analyzer (VNA) measurement range of 94 GHz. The measured saturated output power is +4 dBm.

The die photograph of the entire transceiver is reproduced in Fig. 21, and measures 0.4 mm × 1.2 mm. The receiver part of the transceiver achieves a downconversion gain of 16 dB and an NF of 7–9 dB over an IF bandwidth of 17 GHz (Fig. 22). Here too, the discrepancy between measurement and simulation comes from differences in gain between the upper and lower sidebands. The phase noise measured at the transmitter output

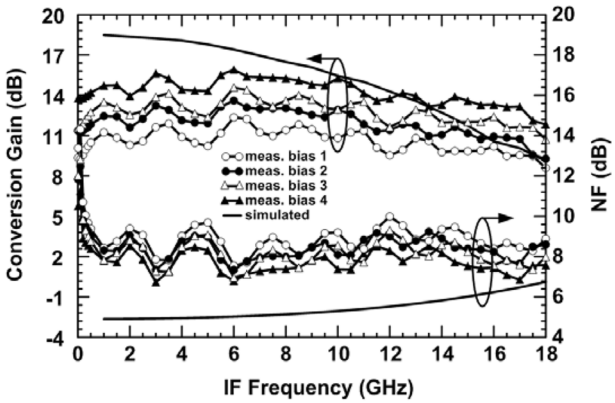

Fig. 22. Measured (lines and symbols) and simulated (lines only) transceiver downconversion gain and NF under different bias conditions. Bias 1: $\mathrm{VDD_{VCO}} = 1.5$ V, $\mathrm{VDD_{LNA}} = 1.5$ V; Bias 2: $\mathrm{VDD_{VCO}} = 1.2$ V, $\mathrm{VDD_{LNA}} = 1.2$ V; Bias 3: $\mathrm{VDD_{VCO}} = 1.5$ V, $\mathrm{VDD_{LNA}} = 1.2$ V; Bias 4: $\mathrm{VDD_{VCO}} = 1.2$ V, $\mathrm{VDD_{LNA}} = 1.5$ V.

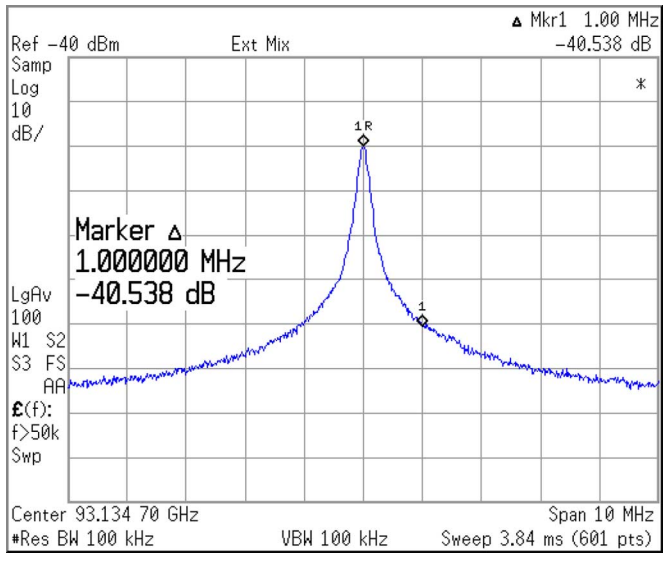

Fig. 23. Measured transmitter phase noise at 93 GHz.

is −90.5 dBc/Hz at 1-MHz offset from the 93-GHz carrier (Fig. 23). The transmitter output power, as measured at the output of one of the two PAs, varies between +1 and +3 dBm over the VCO tuning range of 90.6–93.5 GHz (see Fig. 24).

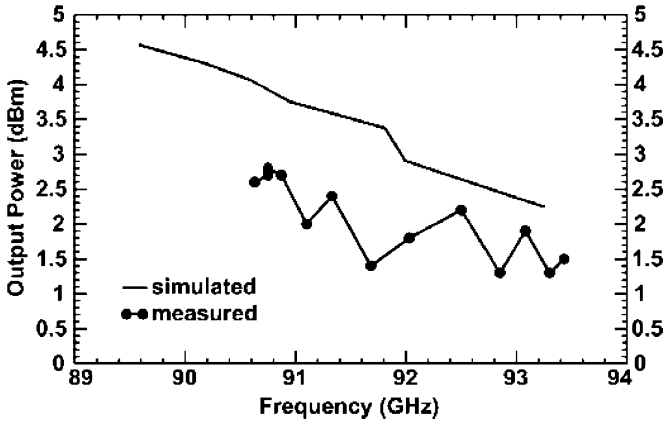

Fig. 24. Measured (line and symbols) and simulated (line only) transmitter power at the differential output.

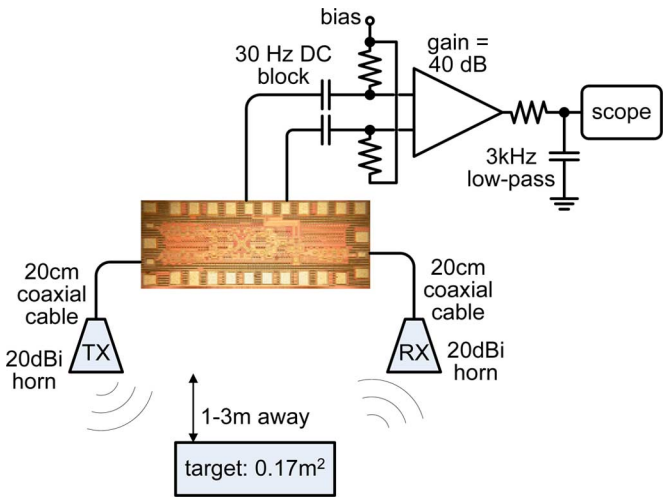

Fig. 25. 93-GHz Doppler experiment test setup.

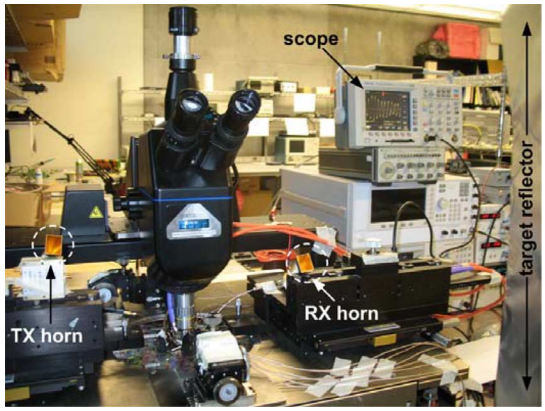

Fig. 26. Test setup for the Doppler experiment, showing the transmit horn antenna (*left*), the receive horn antenna (*center*), the target (*right*), and the oscilloscope that captures the Doppler shift signal (*upper right*).

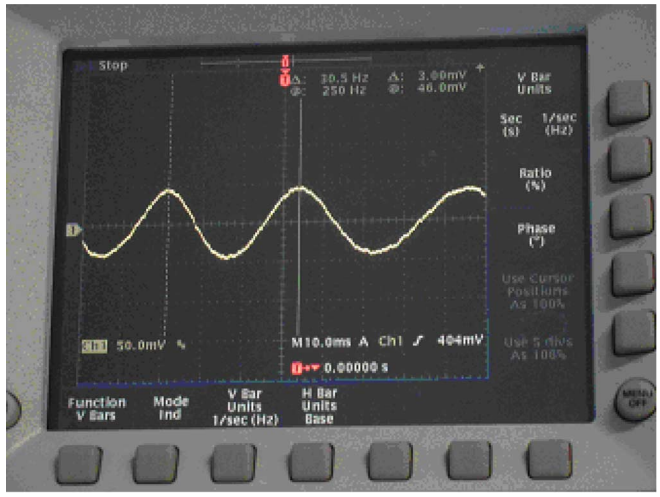

Fig. 27. Measured 30-Hz Doppler shift signal.

The transceiver was employed in the first demonstration of the Doppler effect in silicon at 93 GHz. This was achieved with a low power consumption of only 292 mW from 1.2-V supply and without a PLL. Along with the integration levels possible with a nanoscale CMOS technology, this opens the possibility for large-scale sensor arrays for position and speed measurement suitable for industrial, medical and automotive applications.

The test setup for the Doppler experiment is illustrated in Fig. 25. Horn antennas with 25-dBi gain each are connected through coaxial cables and waveguide sections to the receiver input and to one of the transmitter outputs. The distance between the transmit and receive antennas is approximately 45 cm. The differential signal at the IF output of the receiver is amplified by an off-chip low-frequency amplifier with 40-dB gain, converted to a singe-ended signal and displayed on an oscilloscope. A reflective target with an area of 0.17 m^2 is moved back and forth at varying speeds in front of the antennas at a distance of 1–3 m. A photograph of the actual setup in the laboratory is shown in Fig. 26.

A Doppler shift signal with an amplitude of 50–200 mV, depending on the distance of the target, was observed on the oscilloscope. The Doppler shift frequency varies between 30 and 300 Hz with the speed of the target. A sample 30-Hz waveform is captured on Fig. 27 and corresponds to a target velocity of only 4.8 cm/s. It should be noted that this velocity detection accuracy is comparable to that obtained with a much more complex 35-GHz system, which employs a PLL, quadrature upconversion, two downconversions, and a sophisticated DSP [20].

Although no PLL is employed, either on- or off-chip, low-noise Doppler radar operation is possible because, by sharing the VCO between the transmitter and the receiver, the noise of the delayed VCO signal received from the target is strongly correlated with and cancels out the phase noise of the VCO signal employed in downconversion. This well-documented effect [6] is known as range correlation. The actual phase noise can be easily measured at IF by connecting the transceiver in loop back, as shown in Fig. 28, or by fixing of the position of the target in Fig. 25. When the VCO control voltage is modulated with a low-frequency ramp signal, the resulting IF output is a sinusoid at the same frequency.

The results of the loop-back experiment with the target fixed at 1 m away from the antennas are illustrated in Figs. 29 and 30. The VCO frequency was modulated at 20 and 1 kHz. The corresponding phase noise observed at the IF output is −62.6 dBc/Hz at 170-Hz offset from 20 kHz and −24 dBc/Hz at 1-Hz offset

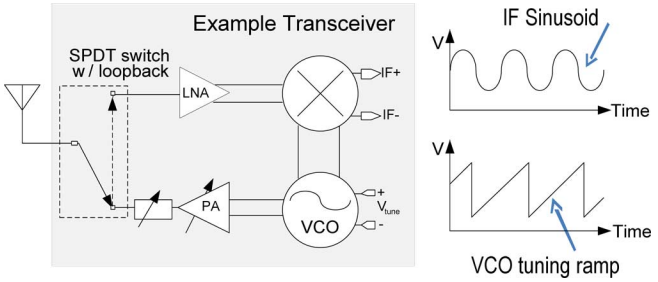

Fig. 28. Concept of speed loop back using the Doppler effect. Only low-frequency signals are applied to the VCO control pads and only the low-frequency output of the receiver needs to be measured.

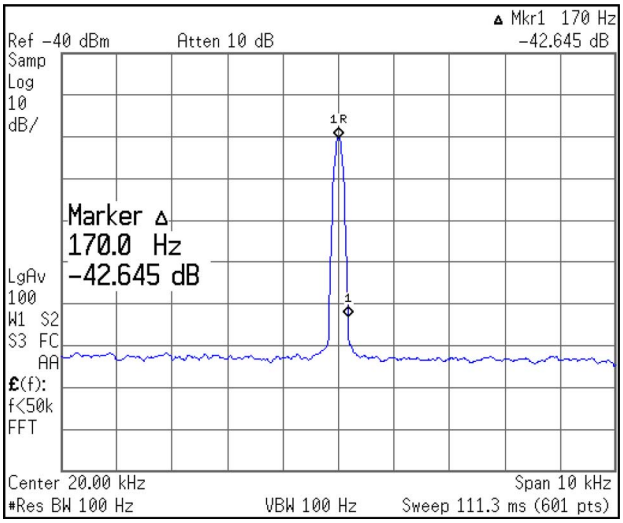

Fig. 29. Phase noise of -62.6 dBc/Hz at 170-Hz offset measured at an IF of 20 kHz with a fixed target in Doppler experiment.

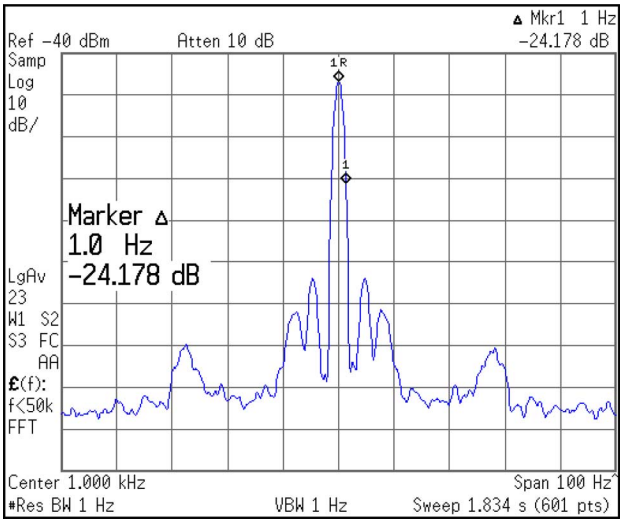

Fig. 30. Phase noise of -24.18 dBc/Hz at 1-Hz offset measured at an IF of 1 kHz with a fixed target in Doppler experiment.

from 1 kHz. These results are comparable to those obtained with an SiGe transceiver at 82 GHz [21], and provide experimental proof that $1/f$ noise is not limiting the performance of radar sensors in CMOS.

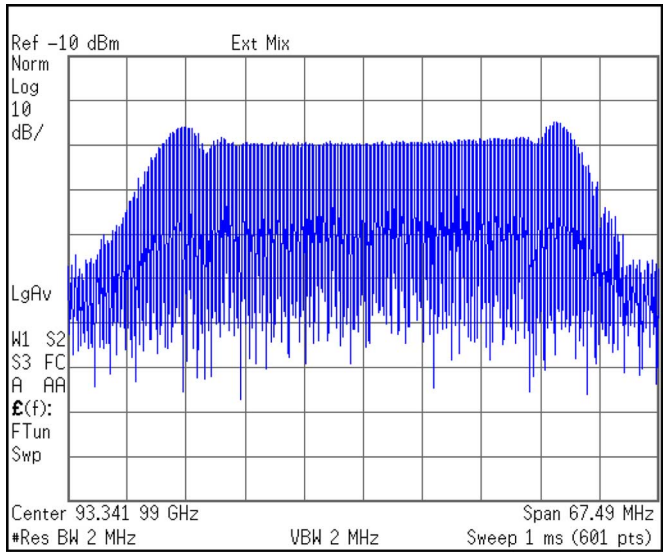

Fig. 31. Transmitted spectrum for a VCO control voltage of 400 kHz and 200-mV amplitude.

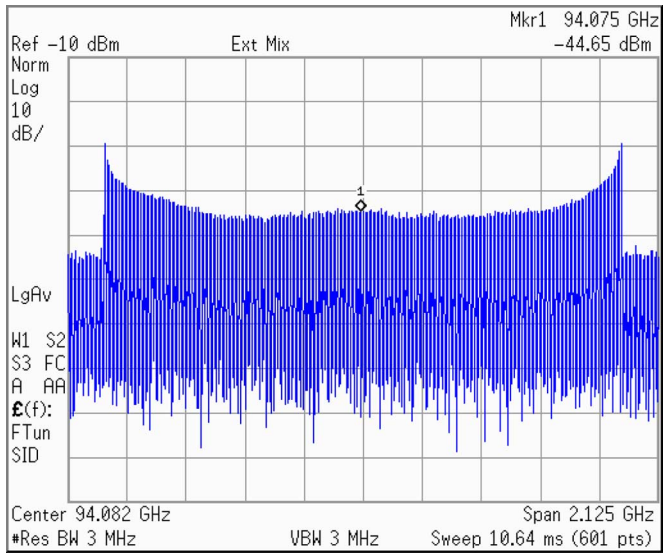

Fig. 32. Transmitted spectrum for a VCO control voltage of 100 kHz and 1.2-V amplitude.

Finally, as discussed in Section II, the linearity and frequency span of the linearly ramped transmitted VCO signal is important for precise position detection. Figs. 31 and 32 illustrate the measured transmitter output spectrum when the control voltage is modulated at 400 kHz with an amplitude of 200 mV, and at 100 kHz with an amplitude of 1.2 V.

C. 140-GHz Downconverter

A 140-GHz downconverter consisting of an LNA, a double-balanced mixer, an IF amplifier, and an on-die dipole antenna was also designed and fabricated. The receiver block diagram is reproduced in Fig. 33 and a photomicrograph of the die, which occupies 580 μm $\times$ 700 μm, is shown in Fig. 34. The on-chip antenna, a differential tapered slot design, is coupled to the single-ended LNA through a transformer, and meets all metal density fill rules.

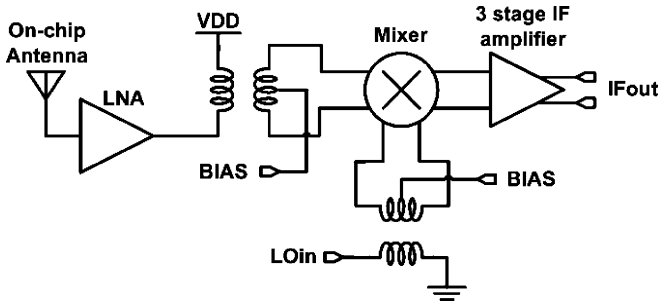

Fig. 33. Block diagram of the 140-GHz downconverter.

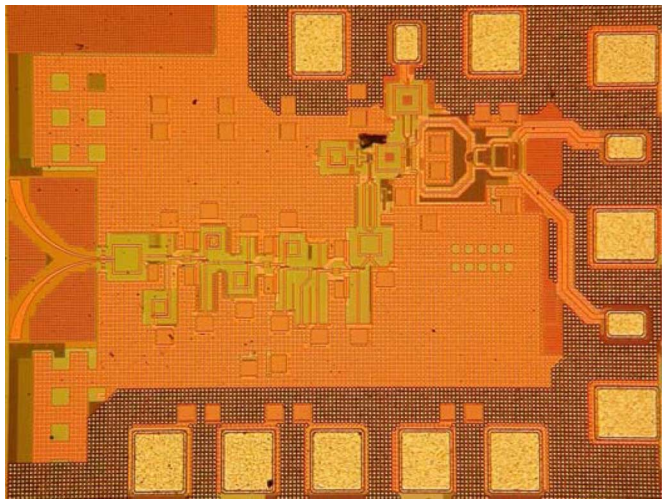

Fig. 34. Die photograph of the 140-GHz downconverter.

The schematic of the 140-GHz LNA is illustrated in Fig. 35. All transistors are biased at 0.25 mA/μm, which corresponds to the peak $f_{\rm MAX}$ current density in this 65-nm GP CMOS technology at a $V_{\rm DS}$ of 1 V. The gates of the first two CS stages (M1 and M3) are biased through 4 kΩ resistors. The final CS stage (M5) uses an inductor that instead partially tunes out its gate capacitance. The input transistor is 16 μm wide, and the width of each of the following transistor stages is scaled upward by 25%, resulting in a total current consumption of 52 mA. To obtain the highest speed operation from a 1.2-V supply, the ac-coupled cascode is used in place of conventional telescopic cascode stages to maximize the $V_{\rm DS}$ of each transistor, and therefore, circuit performance above 100 GHz. Unlike the conventional cascode amplifier, the ac-coupled cascode topology renders the $V_{\rm DS}$ of the CS transistor independent of V_T variations of the common-gate (CG) transistor.

In each stage, the series-connected inductor and capacitor between the CS and CG transistors provide dc blocking, and together represent a short circuit at the desired amplifier center frequency (f_C) of 140 GHz. Capacitance at the center node is now tuned out with the parallel drain inductor of the CS stage and the source inductor of the CG stage. The output of each stage (the drain of the CG device) is then impedance-matched to the next stage input using a standard, two component *LC* matching network. Component values for subsequent stages can be scaled from those in the first stage using transistor-size ratios. The source inductance in the first stage is selected for optimum noise matching. The same inductor is added to the CS input of subsequent stages, which improves stability and aids interstage impedance matching by raising the input impedance.

The layout of the LNA can be clearly seen in Fig. 34 (left side). Decoupling of the CG node $(V_{\rm CG})$ and at the ends of all parallel inductors is provided by interdigitated metal–oxide–metal (MoM) capacitors, indicating that a pure digital CMOS process is usable at 140 GHz. Decoupling capacitors are placed directly beside the node they decouple to minimize parasitic inductance. All inductors are modeled as lumped elements, implemented in a 2-μm-wide top metal, approximately 4.5 μm above the substrate.

The 140-GHz LNA was measured in a 110–170-GHz rectangular waveguide setup. The gain of the LNA at 1.2-V supply is 9 dB, peaking at 144 GHz with a 3-dB bandwidth of 10 GHz, Fig. 36. The measured power consumption at 1.2-V supply is 63 mW. At 1.0-V supply, the gain reduces to 5.5 dB. Compared to simulations, the LNA gain has shifted upward in frequency by 7 GHz, or 5%. This agrees with the measured transistor power gain at 94 GHz, which, as shown in Fig. 8, is about 1 dB larger than simulations. The LNA maintains 2.2 dB of power gain at 125 °C, and the center frequency has shifted downward from 144 to 140 GHz. The amplifier achieves an $\mathrm{IP}_{1\ \rm dB}$ of -12 dBm and a $\mathrm{P}_{\rm SAT}$ of at least -1.8 dBm. In this measurement, the LNA is not fully saturated because the output power of the signal source used to drive the LNA is limited to -10 dBm at 144 GHz.

It should be mentioned that a 150-GHz three-stage CS LNA with 8-dB gain was recently reported in a similar 65-nm CMOS process [22]. In the latter, the loss of the interstage matching network was cleverly prevented by dc-coupling the gates of the MOSFETs to the drain of the transistor in the preceding stage. Each MOSFET is thus biased with $V_{\rm GS} = V_{\rm DS} = V_{\rm DD}$, forming a large diode-connected transistor at dc. Compared to the ac-coupled cascode topology, a potential drawback of this scheme is the increased sensitivity to power supply variation.

The receiver conversion gain was measured on receivers with and without an on-chip antenna, using a 1.2-V supply, and an external LO-signal of $+1$ dBm (at the LO probe tip) at 102 GHz, as shown in Fig. 37. The conversion gain is expected to improve when a 140-GHz LO is used, but could not be measured because a second 140-GHz signal source was not available. A low-phase noise VCO, with adequate output power to drive the mixer at its optimum NF and conversion gain remains one of the challenging goals that need to be met above 100 GHz in CMOS.

Finally, a 140-GHz SPDT switch, whose schematic is shown in Fig. 38, was designed, fabricated, and tested in the same 65-nm GPLP process. It employs 14×3 μm $\times$ 60 nm high-threshold voltage GP devices. The use of a larger (3 μm) finger width permits the reduction of parasitic metallization capacitance without compromising performance. The high-threshold voltage devices improve the linearity of the switch. Lumped, series-connected spiral inductors placed at each port form a distributed transmission line in conjunction with the pad and switch capacitance to improve bandwidth and matching. An on-chip 50-Ω termination was placed at port 3 and the S-parameters were measured in the D-band with two OML VNA test heads for the two switch states.

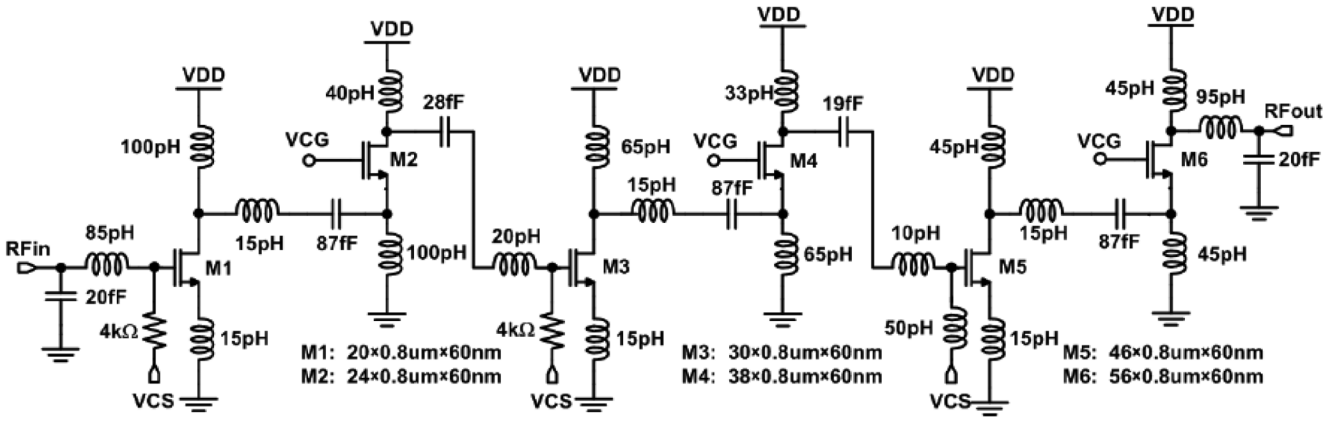

Fig. 35. Schematic of the 140-GHz LNA.

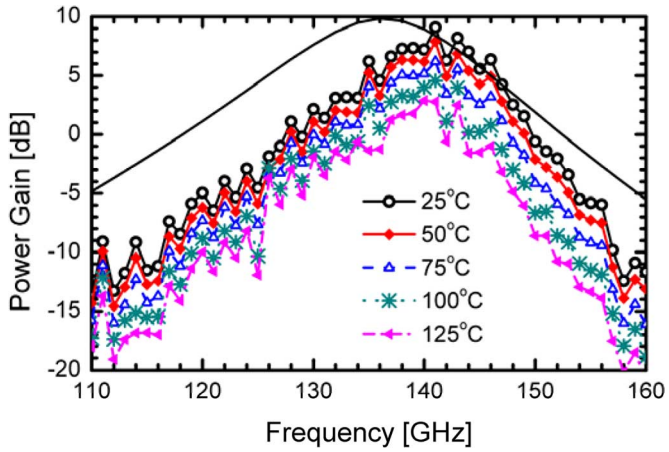

Fig. 36. Measured (lines and symbols) versus simulated (solid black line, 25 °C only) LNA gain versus frequency and temperature.

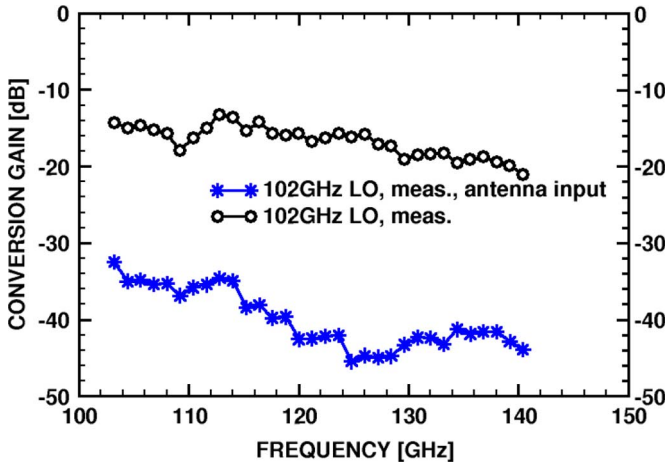

Fig. 37. Measured receiver gain versus frequency with and without on-die antenna.

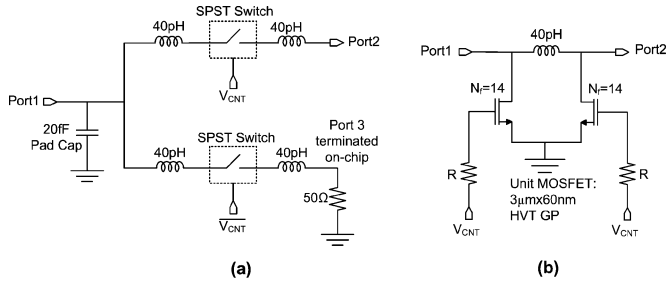

Fig. 38. Schematic of 140-GHz SPDT CMOS switch. (a) SPDT switch. (b) Unit SPST switch.

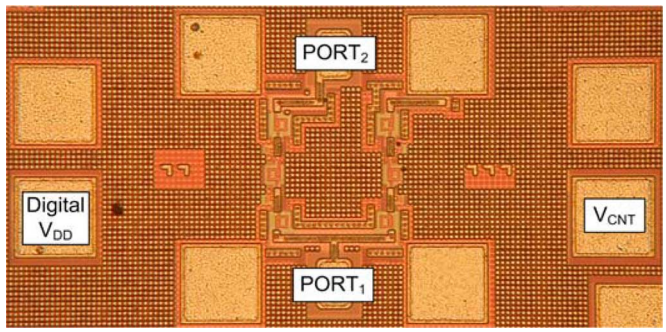

Fig. 39. Die microphotograph of the D-band CMOS switch.

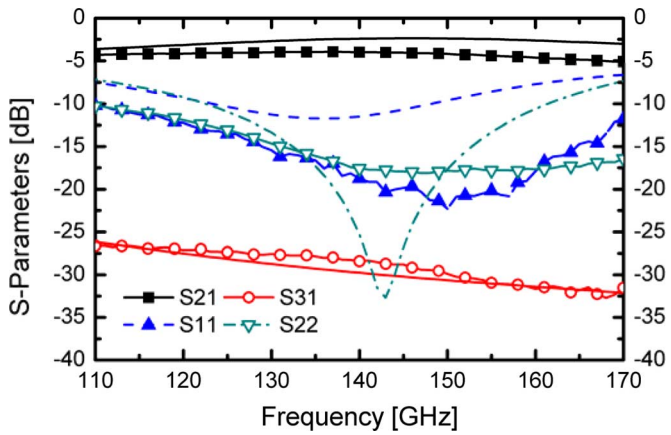

Fig. 40. Measured (solid lines and symbols) versus simulated (dashed lines) switch insertion loss and isolation.

The switch, shown in Fig. 39, occupies 570×280 μm^2 (0.16 mm^2) including all pads, with a core switch area of only 180×130 μm^2 (0.02 mm^2). As illustrated in Fig. 40, the measured insertion loss (S_{21}) in the D-band is better than -5 dB across the band and less than -4 dB at 140 GHz. The isolation (S_{31}) is higher than 25 dB and the return loss is better than 10 dB throughout the 110–170-GHz range. The excellent agreement between simulation and measurements confirms that the proposed modeling and design approach is adequate for predicting the small-signal operation of simple circuits up to 170 GHz.

VI. Conclusion

Potential applications of highly integrated CMOS transceivers in the 90–170-GHz range were discussed along with architectures required for their implementation. The highest frequency transceivers and receivers fabricated in CMOS to date were described in detail. For the first time, the Doppler effect was demonstrated at 94 GHz in silicon, showing excellent cancelation of phase noise without employing a PLL. Although the feasibility of a 140-GHz amplifier, downconverter, and antenna switch was demonstrated in a GPLP 65-nm CMOS process with a conventional digital back end, an RF 32-nm CMOS technology is required to develop products with adequate performance margin at this frequency.

Acknowledgment

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References

[1] K. Kuhn, "IEEE IEDM short course," presented at the IEEE IEDM, Dec. 2008.

[2] S. P. Voinigescu, M. Khanpour, S. T. Nicolson, A. Tomkins, E. Laskin, A. Cathelin, and D. Belot, "CMOS receivers in the 100–140 GHz range," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 193–196.

[3] L. Changzhi, J. Cummings, J. Lam, E. Graves, and W. Wu, "Radar remote monitoring of vital signs," *IEEE Microw. Mag.*, vol. 10, no. 1, pp. 47–56, Feb. 2009.

[4] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A 94 GHz SPST switch in 65 nm bulk CMOS," in *Proc. IEEE Compound Semicond. Integr. Circuits Symp. Dig.*, Oct. 2008, pp. 139–142.

[5] J. Gilb, "Workshop: Millimeter-wave CMOS radio design for gigabit wireless applications," presented at the IEEE MTT-S Int. Microw. Symp., Jun. 2008.

[6] M. C. Budge, Jr. and M. P. Burt, "Range correlation effects in radars," in *Proc. Rec. 1993 IEEE Nat. Radar Conf.*, 1993, pp. 212–216.

[7] L. Yujiri, M. Shoucri, and P. Moffa, "Passive millileter-wave imaging," *IEEE Microw. Mag.*, pp. 39–50, Sep. 2003.

[8] M. E. Tiuri, "Radio astronomy receivers," *IEEE Trans. Antennas Propag.*, vol. 12, no. 7, pp. 930–938, Dec. 1964.

[9] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imager in 65 nm bulk CMOS," in *Proc. IEEE CSICS*, Greensboro, NC, 2009, pp. 91–94.

[10] E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "165-GHz transceiver in SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1087–1100, May 2008.

[11] R. A. Aroca, A. Tomkins, Y. Doi, T. Yamamoto, and S. P. Voinigescu, "Circuit performance characterization of 45-nm digital technology for applications around 110 GHz," in *Proc. IEEE VLSI Symp. Dig.*, Jun. 2008, pp. 162–163.

[12] S. T. Nicolson, A. Tomkins, K. W. Tang, A. Cathelin, D. Belot, and S. P. Voinigescu, "A 1.2 V 140 GHz receiver with on-die antenna in 65 nm CMOS," in *Proc. IEEE Radio-Freq. Integr. Circuits Symp.*, Jun. 2008, pp. 229–232.

[13] A. Tomkins, R. A. Aroca, T. Yamamoto, S. T. Nicolson, Y. Doi, and S. P. Voinigescu, "A zero-IF 60 GHz transceiver in 65 nm CMOS with $>$3.5 Gb/s links," in *Proc. IEEE Custom Integr. Circuits Conf. Dig.*, Sep. 2008, pp. 471–474.

[14] T. O. Dickson, K. H. K. Yau, T. Chalvatzis, A. Mangan, R. Beerkens, P. Westergaard, M. Tazlauanu, M. T. Yang, and S. P. Voinigescu, "The invariance of the characteristic current densities in nanoscale MOSFETs and its impact on algorithmic design methodologies and design porting of Si(Ge) (Bi)CMOS high-speed building blocks," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1830–1845, Aug. 2006.

[15] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*. New York: Wiley, 2006, ch. 4.

[16] S. P. Voinigescu, A. Tomkins, M. Wiklund, and W. Walker, "A direct MM-wave M-ary QAM modulator operating in saturated power mode," U.S. Patent, application.

[17] S. P. Voinigescu, R. Aroca, T. O. Dickson, S. T. Nicolson, T. Chalvatzis, P. Chevalier, P. Garcia, C. Garnier, and B. Sautreuil, "Towards a sub-2.5 V, 100-Gb/s serial transceiver," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, Sep. 2007, pp. 471–478.

[18] M. Khanpour, K. W. Tang, P. Garcia, and S. P. Voinigescu, "A wideband W-band receiver front-end in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1717–1730, Aug. 2008.

[19] E. Laskin, M. Khanpour, R. A. Aroca, K. W. Tang, P. Garcia, and S. P. Voinigescu, "95 GHz receiver with fundamental frequency VCO and static frequency divider in 65 nm digital CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2008, pp. 180–181.

[20] S. Kim and C. Nguyen, "On the development of a multifunction millimeter-wave sensor for displacement sensing and low-velocity measurement," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 11, pp. 2503–2512, Nov. 2004.

[21] S. T. Nicolson, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "Single-chip W-band SiGe HBT transceivers and receivers for Doppler radar and millimeter-wave imaging," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2206–2217, Oct. 2008.

[22] M. Seo, B. Jagannathan, C. Carta, J. Pekarik, L. Chen, C. P. Yue, and M. Rodwell, "A 1.1 V 150 GHz amplifier with 8 dB gain and $+6$ dBm saturated output power in standard digital 65 nm CMOS using dummy pre-filled microstrip lines," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2009, pp. 484–485.

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