122 GHz Low-Noise-Amplifier in SiGe Technology

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***Abstract* — The paper presents two types of 122 GHz low-noise-amplifiers (LNA) fabricated in SiGe BiCMOS technology. The amplifier design takes advantage of a novel transmission line structure with thick metal ground-shield on top of the MMIC. The circuit is a two-stage cascode topology utilizing transmission lines for input, output and inter-stage matching. The amplifiers are designed for high gain, minimum noise figure and low power consumption. Measurements show a gain of 13.5 dB and a noise figure of 9.6 dB at 122 GHz. The power consumption is 52mW from a 3.5 Volt supply. The other version of the LNA with transformer coupling to the output instead of capacitive coupling has slightly lower gain. The amplifier is intended for the use in ISM-band radar and communication systems, wide-band communication systems and in radar imaging systems.**

I. INTRODUCTION

The 122GHz ISM-band with frequency from 122-123 GHz provides new opportunities for a broad range of new products and services, including high data-rate communication, low-cost radar-systems for consumer applications and imaging radar for security applications. Besides of this, there is a proposal to utilize the frequency band around 120 GHz for data transmission with very high data rate to transmit 6 channels of uncompressed HD-SDI signals [4] (HD-SDI: high definition serial-digital interface). In this case, a larger bandwidth, exceeding the ISM-band is required.

Some of these applications include potentially high-volume products calling for cost-effective components fabricated in mainstream silicon-based technologies. Recently, several integrated circuits for these bands were presented based on CMOS and SiGe bipolar or BiCMOS technologies [1], [2], [3].

This paper presents two types of 122 GHz low noise amplifiers fabricated in 130 nm SiGe BiCMOS technology of IHP [5].

II. CIRCUIT DESIGN

The design of integrated amplifiers at millimeter-wave frequencies faces the difficulty of inevitable parasitics at the interface to the PCB. Also internal parasitics in the wiring of internal ground node are difficult to handle in a standard CMOS or BiCMOS technology. In contrast, technologies with compound semiconductors often provide through-holes in the substrate providing nerly ideal ground at every position of the chip surface.

To overcome these problems, many of the designs of MMICs in silicon-based technologies are differential designs [6]. These differential topologies are less susceptible to parasitic feedback loops that can cause stability problems or degeneration of the circuit performance. But, single-ended amplifiers have the advantage of better noise performance and lower power consumption. That's why the single-ended circuit topology was chosen for the design of these novel 122 GHz amplifiers. To overcome the quality-problems with internal ground, an innovative transmission-line structure was used providing high-quality grounding at every place of the chip. The description of the structure follows in section III.

Figure 1 shows the schematic of the two versions of the LNA. The circuit a) is the version with capacitive coupling to the output pad (LNA1). The circuit b) is the version with transformer coupling to the output. It is intended for the use in a 122 GHz frontend using subharmonic mixer with differential RF-input. The differential signal is generated in this output transformer. In both cases, the LNA is a two stage cascode design with matching networks for input and output matching to 50 Ohm. For simplicity, the circuitry for generation of reference voltages V_{B1} and V_{B2} is not included in the schematic. The cascode configuration was chosen for the higher gain per stage in comparison to the common-emitter configuration due to reduction of the Miller effect in the CE-part of the cascode. In addition, the cascade configuration with its stacked transistors is well suited for the intended use of the LNA in RF frontends with 3.0 – 3.5 V supply voltage. Each stage provides around 7 dB of gain with

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a biasing of 4.9 mA and 5.4 mA for the first and second stage respectively at a supply voltage of 3.5 V.

The biasing of the CE transistors T1 and T3 is performed by current mirrors utilizing the transistors T5 and T6 and the transmission lines TL1 and TL3 respectively. These transmission lines are ac-shorted at the one side and connected to the base of transistors T1 and T3 respectively on the other side thereby transforming the ac-short to an open (or at least high-ohmic state) at the bases. The overall input matching network consists of the parasitic pad capacitance, the transmission line for the connection from pad to the first amplifier stage (not shown in the figure), TL2 (ESD protection of the input), C1 (MIM capacitor for dc-decoupling of the input) and TL1. To obtain a high Q of the input pad capacitor C22, the pad is shielded from the Silicon substrate by a grounded plate in metal1. The capacitors C4 and C5 for grounding of the bases of T2 and T4 are MIM capacitors placed nearby to the transistors to obtain low series inductance. The series transmission lines TL4 and TL5 slightly increase the gain of the cascode stages by improved matching between T1 and T2 and between T3 and T4 respectively. Transmission lines TL6 and TL7 are load-elements for the gain stages. Together with the capacitors C2, C3 and the output pad capacitance, they perform the inter-stage matching and the output matching respectively.

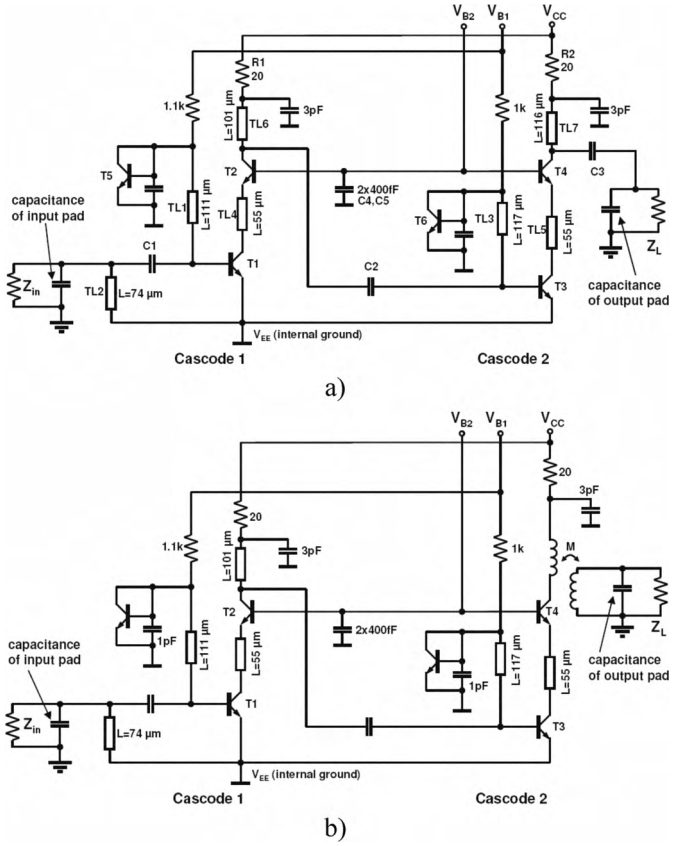


Figure 1: Circuit schematic of LNA; Circuitry for generation of reference voltages V_{B1} and V_{B2} is not included; a) LNA1 with capacitive output coupling, b) LNA2 with transformer coupling

The resistors R1 and R2 are inserted for decoupling of the two stages and for preventing oscillations. The reference voltages V_{B1} and V_{B2} are generated in a separate network consisting of diodes and resistors.

The design was accomplished with the transistor models of IHP for its 130 nm SiGe:C BiCMOS technology with 5 metal layers [5]. The technology provides two types of bipolar transistors, three types of polysilicon resistors, a high-quality MIM capacitor and five aluminium metal layers including two top-metal layers with 2 µm and 3 µm thickness respectively. The latter are especially important for low-loss transmission lines. The separation of top-metal 1 and top-metal 2 to the substrate is 6.4 µm and 11.4 µm respectively. The separation between the top-metal layers is 3 µm. High-ohmic silicon substrate with 50 Ωcm is used. P-well implants are blocked at critical parts of the layout. Table 1 shows some parameters of the bipolar transistors used in the design [5].

TABLE I
Transistor parameters

Parameter	npn1
Emitter area	0.17 x 0.53 µm^2
Peak f_{max}	255 GHz
Peak f_T	315 GHz
BV_{CEO}	1.8 V
BV_{CBO}	5.6 V
β	600

All the transmission lines were simulated with a 3D planar EM-simulator (Momentum). The results were included in the optimization of the circuit by means of transmission line models within ADS of Agilent. The simulation results are presented in Figure 5 and Figure 6. The calculated gain is 16.1 dB at 122 GHz and the reverse gain is -51 dB. The matching was performed in such a way that a good match to 50 Ohm at the output and minimum noise figure at the input were obtained. There is a good coincidence of the noise figure of the amplifier to the minimum noise figure (only a few percent differences as shown in Figure 5 b). The simulated noise figure amounts to 8.3 dB. The optimization of input and output matching was performed for 122 GHz including parasitic elements from the final layout geometry.

III. Layout Design

The layout of the amplifier chip was governed by the use of the new transmission line structure discussed in section II. It provides an excellent ground plane on top of the whole chip. The structure of the transmission line is illustrated in the chip photo in Figure 2 and Figure 3 and in the cross section in Figure 4. The chip size of LNA1 is 0.45 x 0.65 mm^2 including pads. Figure 2 and Figure 3 show the chips with the 100 µm GSG input and output configuration for on-wafer measurement. The pads on the right hand and on the left hand side are dc-pads for ground and supply voltage V_{CC}. Only one supply pad (V_{CC}) is used for on-wafer measurement. The other pads are redundent and can be used for parallel bonding

in board assemblies. The ground-plate fills the area between the pads and covers all the structures below the top metal 2 layer. The holes in the TM2-plate are inevitable for the fabrication of the chip because of mechanical strain in the layers (slit rules). The open areas in the middle of the chip are intended for capacitance reduction at sensitive nodes in the circuit.

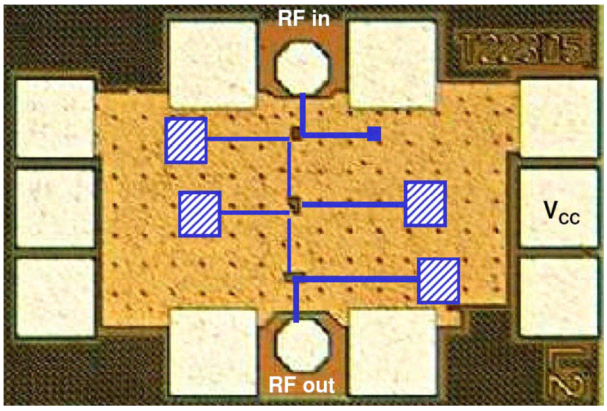


Figure 2: Chip photo of LNA1 with overlay of the transmission line structures (lines) and blocking capacitors (striped areas)

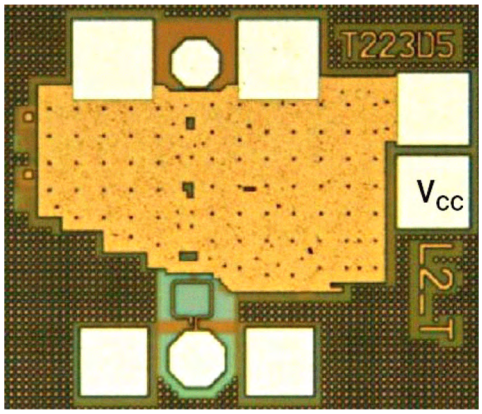


Figure 3: Chip photo of LNA2 with transformer coupling at output

Figure 4 shows the construction of the "inverted" transmission line structure. The large aluminium ground-plate is on top of the structure. It is separated from the semiconductor substrate by silicon dioxide with a thickness of 11.4 µm. The signal line has a thickness of 2 µm and is separated from the ground plate by SiO_2 with a thickness of 3 µm. The properties of these transmission lines are mainly determined by the gap between signal line and ground plate. Because of the larger distance (6.4 µm) to the lossy silicon substrate, the effect of the substrate is low. Additionally, the channel stop implant was removed at critical places resulting in a high-ohmic region that further reduces the losses.

IV. Simulation and Measurement Results

The amplifier circuits were simulated and optimized using ADS. Figure 5 presents simulated gain, noise figure and minimum noise figure. Figure 6 presents the simulated input and output matching.

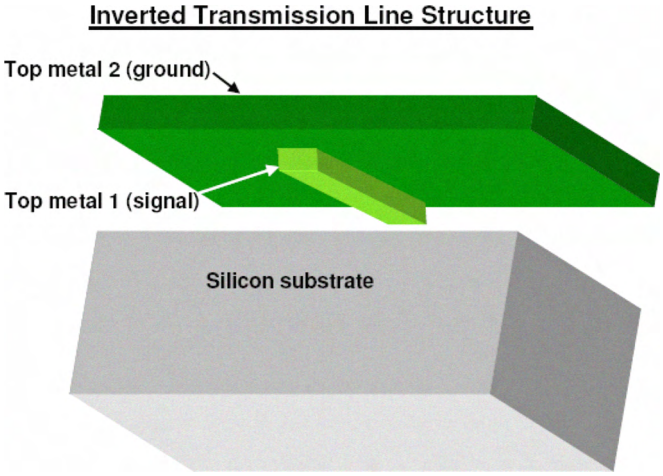
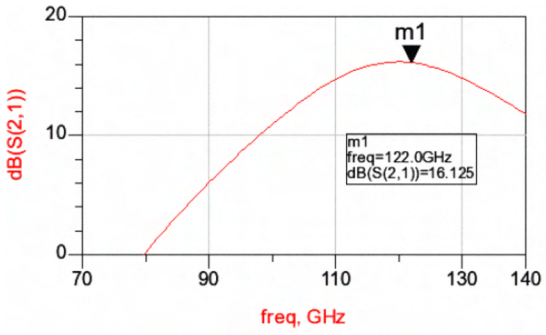


Figure 4: Cross section of transmission lines

TABLE II
Summary of LNA1-Performance in Simulation and Measurement

Parameter	Measurement	Simulation
V_{CC}	3.5 V	3.5 V
I_{CC}	14.2 mA	15 mA
gain @ 122 GHz	13.5 dB	16 dB
NF @ 122 GHz	9.6 dB	8.3 dB



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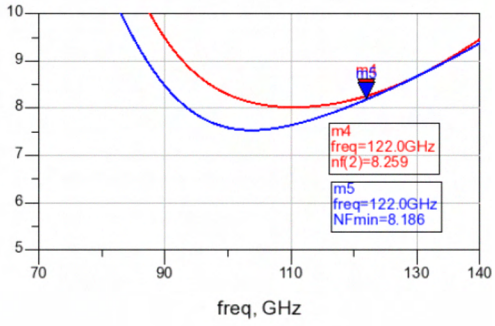


b)

Figure 5: Simulated gain, noise figure and minimum noise figure of LNA1

The s-parameters were measured using an Agilent vector network analyser VNA 8510XF. Figure 7 presents the

measurement results of LNA1. The measured gain is 13.5 dB at 122 GHz. This agrees satisfactorily with the simulated value of 16.1 dB keeping in mind that the transistor models at this high frequency are not yet absolutely precise. This quite good correlation between measurement and simulation shows another advantage of the concept of "inverted" transmission line. Because of the very reliable ground nodes, the modelling and simulation will also be quite trustworthy.

The measured noise figure is 9.6 dB, i.e. 1.3 dB higher than in simulation.

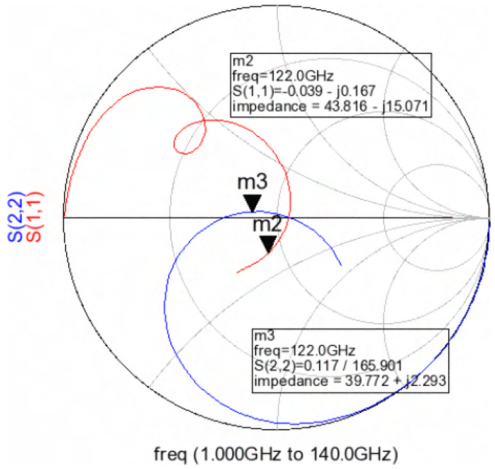
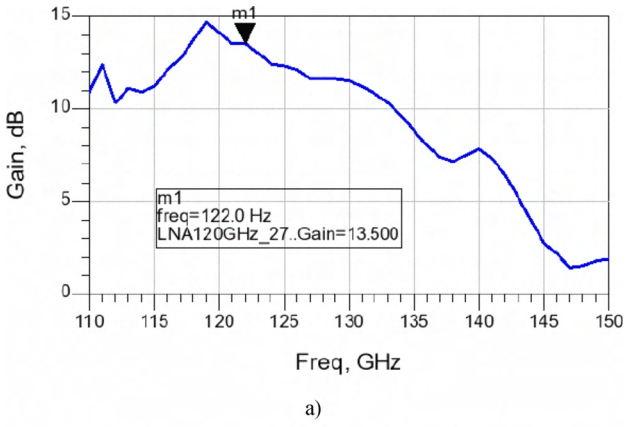
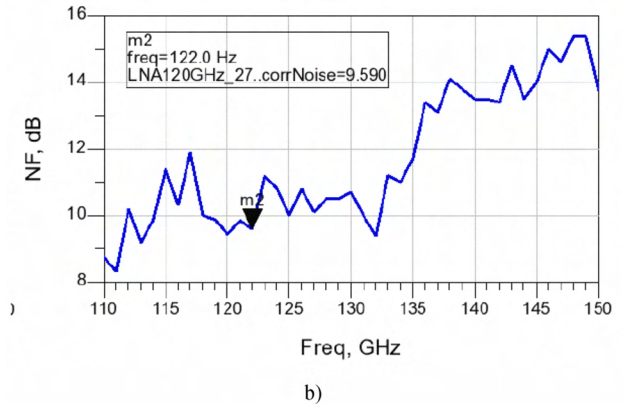


Figure 6: Simulated input and output matching of LNA1 with markers for 122 GHz



a)



b)

Figure 7: Measured gain (a) and noise figure (b) of LNA1

V. Conclusions

A 122 GHz amplifier using a novel transmission line structure compatible to main-stream CMOS was presented. Utilizing the design-style with top-plate ground, very high frequencies can be reached with silicon-based technologies. The demonstrated amplifier has a gain of 13.5 dB and a noise figure of 9.6 dB at 122 GHz. Considerable agreement between simulation results and measurements have verified the concept. The amplifiers are ESD-protected at the input (LNA1) and at input and output (LNA2).

The design-style with top-plate ground used in these LNA-designs is a good candidate for silicon-based integrated circuits at frequencies as high as 100 GHz or even higher.

Acknowledgment

The authors are thankful for the IHP pilot line staff for excellent fabrication of the chip. The authors thank Mr. Hermann Massler from Fraunhofer IAF for gain and noise measurement.

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