A Fundamental Frequency 120-GHz SiGe BiCMOS Distance Sensor With Integrated Antenna

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***Abstract*—This paper describes the first fundamental frequency single-chip transceiver operating at D-band. The low-IF monostatic transceiver integrates on a single chip two 120-GHz voltage-controlled oscillators (VCOs), a 120-GHz divide-by-64 chain, two in-phase/quadrature (IQ) receivers with phase-calibration circuitry, a variable gain transmit amplifier, an antenna directional coupler, a patch antenna, bias circuitry, a transmit power detector, and a temperature sensor. A quartz antenna resonator with 6-dBi gain and simulated 50% efficiency is placed directly above the on-chip patch to transmit and receive the 120-GHz signals. The circuit with the above-integrated-circuit antenna occupies an area of 2.2 mm $\times$ 2.6 mm, consumes 900 mW from 1.2- and 1.8-V supplies, and was wire-bonded in an open-lid 7 mm $\times$ 7 mm quad-flat no-leads package. Some transceiver performance parameters were characterized on the packaged chip, mounted on an evaluation board, while others, such as receiver noise figure and VCO phase noise at the 120-GHz output were measured on circuit breakouts. The AMOS-varactor VCOs have a typical phase noise of -100 dBc/Hz at 1-MHz offset and a tuning range of 115.2–123.9 GHz. The receiver gain and the transmitter output power are each adjustable over a range of 15 dB with a maximum transmitter output power of 3.6 dBm. The receiver IQ phase difference, measured at the IF outputs of the packaged transceiver, is adjustable from 70° to 110°, while the amplitude imbalance remains less than 1 dB. The receiver breakout gain and double-sideband noise figure are 10.5–13 and 10.5–11.5 dB, respectively, with an input compression point of -20.5 dBm. Several experiments were conducted through the air over distances of up to 2.1 m with a focusing lens placed above the packaged chip.**

***Index Terms*—D-band, distance sensor, Doppler radar, integrated antenna, in-phase/quadrature (IQ) receiver, 120-GHz transceiver, phase calibration circuit, radar sensor, SiGe BiCMOS.**

I. Introduction

RECENT advancements in SiGe BiCMOS technology [1]–[3] have paved the way for the development of integrated transmitters, receivers, and transceivers operating well into the D-band (110–170 GHz) frequency range [4]–[10]. This frequency range offers opportunities for new applications of silicon technology, such as passive remote sensing [11], short range radar, nondestructive testing with active imaging [12], and high data-rate point-to-point links [13]–[16].

Most importantly, due to the small operating wavelengths involved, different types of integrated antennas can be implemented [17]–[19], avoiding the use of lossy cumbersome off-chip transitions, and thus greatly simplifying the packaging process and enabling very low-cost solutions.

The 122.5-GHz industrial–scientific–medical (ISM) band with 1-GHz bandwidth is ideal for narrowband short-range radar sensors for velocity and distance detection of a single reflecting target since no target separation that requires larger bandwidths would be needed. For distances of up to approximately 2 m, a relatively low transmitter power of 0 dBm results in signal-to-noise ratios (SNRs) that are adequate for accurate detection, and simultaneously satisfy the maximum allowed effective isotropic radiated power (EIRP) of 20 dBm, thus paving the way for simple silicon realizations, as will be discussed in this paper.

This paper is organized as follows. The system architecture, specification, and analysis are covered in Section II. A detailed description of the transistor-level design considerations and the simulated performance of each block are provided in Section III. Section IV summarizes the antenna design, its simulated performance, and provides a brief overview of the fabrication process and packaging. The experimental verification of the circuit breakouts and of the packaged chip, including radar experiments over a distance of up to 2.1 m, are described in Section V. The main conclusions and comparison with other work are summarized in Section VI.

II. System Architecture

A. General Considerations

The block diagram of the proposed monostatic 120-GHz transceiver, fabricated in a production 130-nm SiGe BiCMOS process with dedicated millimeter-wave back-end-of-line (BEOL) [2], is illustrated in Fig. 1. Two fundamental frequency voltage-controlled oscillators (VCOs), operating at a frequency difference of 1.5–3 GHz, are employed to generate the transmit and receive local oscillator (LO) signals, allowing for an adjustable receiver output frequency. After passing through an amplifier with variable output power, the transmit VCO signal is coupled to the antenna through a 6-dB directional coupler that isolates the transmitted signal and the received signal reflected by the target. The latter is routed to the receiver through the coupler and undergoes downconversion to an IF by a quadrature receiver. The signal from the receive VCO is distributed to the two in-phase/quadrature (IQ) mixers and to a

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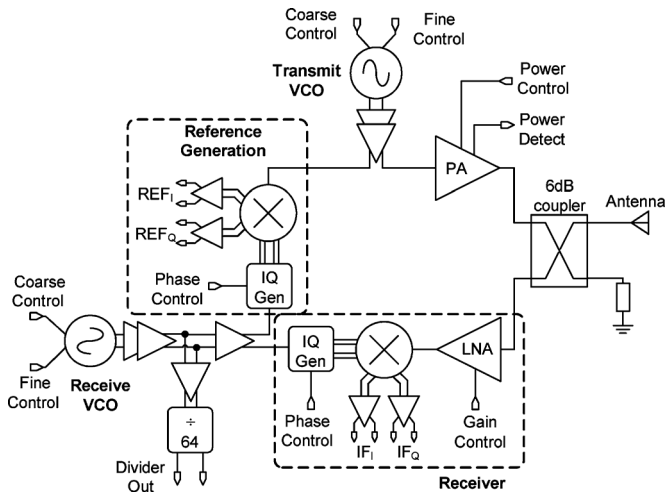


Fig. 1. Block diagram of the transceiver.

divide-by-64 chain whose output, at approximately 1.9 GHz, is provided to an off-chip phase-locked loop (PLL), which locks the VCO to a stable frequency reference.

The local transmit and receive VCO outputs are also downconverted by a second quadrature receiver, which provides a reference IF frequency signal. The reference path IQ downconverter is identical to the main receiver, apart from the low-noise amplifier (LNA), which has been omitted since the amplitudes of the two multiplied signals are large enough for the mixer noise to be irrelevant. The reference receiver serves a dual purpose. First, it can be used to lock the transmit VCO in an external PLL. Second, it provides a phase reference for the main receiver allowing for phase and frequency variations of the signal reflected by the target to be accurately measured.

The monostatic radar architecture was preferred over the bistatic one because of its potential for a simpler lower cost solution. Since the antenna feed and ground plane are formed on the silicon die, it is crucial to reduce the number of antennas in order to minimize the use of silicon area, and thus, reduce system cost.

Due to imperfect antenna, LNA input, and transmit amplifier output matching, as well as because of imperfections in the antenna directional coupler, a portion of the transmitted signal will leak into the receiver, potentially desensitizing it. After conducting an analysis of different microstrip structures for the directional coupler, in which realistic values were assumed for the reflection coefficients of the circuit blocks connected to the coupler, and the process variation of the termination resistor was accounted for, it was concluded that the isolation between the output of the transmit amplifier and the input of the receiver will not be greater than 20–25 dB. As a result, it was decided to limit the transmitter output power to 0 dBm. Therefore, to ensure that the receiver performance is not impaired by the leakage of the transmitter, the receiver input compression point has to be better than -20 dBm. Both the transmitter output power and the receiver input compression point are relatively easy to satisfy using silicon technology at 122 GHz. To provide an adequate margin in case of even poorer isolation, output power control in the transmit amplifier and gain control in the receiver LNA were introduced.

TABLE I
SYSTEM PARAMETERS

Symbol	Description	Value
d	Target distance	$2\,\mathrm{m}$
σ	Radar cross-section	$0.01\,\mathrm{m}^2$
f_0	Center frequency	$122\,\mathrm{GHz}$
T	System temperature	$300\,\mathrm{K}$
G_{ant}	Antenna gain	$20\,\mathrm{dBi}$
P_{TX}	Transmit power	$0\,\mathrm{dBm}$
a_{coupler}	Coupler coupling ratio	$6\,\mathrm{dB}$
F	Receiver noise figure	$15\,\mathrm{dB}$
f_c	Receiver flicker noise corner	$10\,\mathrm{kHz}$
$B = 1/\tau$	Bandwidth/integration time	variable

Another problem associated with the system architecture of Fig. 1 is the crosstalk between the two VCOs, which affects the minimum IF frequency that can be realized in practice. Due to inevitable coupling through the silicon substrate and through the supply distribution planes, the isolation between the two VCOs is finite and they will eventually injection-lock each other if their frequency difference is sufficiently small. When that happens, the IF frequency becomes zero. Unfortunately it is very difficult to analyze and accurately capture all of the coupling mechanisms between the two VCOs in simulation. Therefore, the minimum realizable IF frequency will have to be determined experimentally.

B. SNR Analysis

To estimate the SNR of the radar transceiver for operation over 2 m, the parameters of Table I have been assumed. The receiver noise figure has been set to 15 dB, higher than that of state-of-art D-band SiGe HBT transceivers (e.g., [5], [6], [8], and [9]) in order to account for the degradation due to the antenna coupler. The flicker noise corner for the receiver was set to 10 kHz. The corner frequency is based on simulations of the present receiver and corresponds to the $1/f$ corner of the SiGe HBT at large base and collector currents [2].

Accounting for flicker noise, the receiver output noise floor can be expressed as

$$N_{\mathrm{RX}} = k_B T B \left(1 + \frac{f_c}{f}\right) F G_{\mathrm{RX}} \tag{1}$$

where G_{RX} is the receiver gain, f is the IF frequency, k_B is the Boltzmann's constant, and F is the receiver noise factor. The received signal power at the receiver output is given by

$$P_{\mathrm{RX}} = G_{\mathrm{RX}} P_{\mathrm{TX}} a_{\mathrm{coupler}} a_{\mathrm{radar}} \tag{2}$$

where a_{radar} is the attenuation (free-space loss) predicted by the radar equation

$$a_{\mathrm{radar}} = \frac{G_{\mathrm{ant}}^2 c^2 \sigma}{(4\pi)^3 f_0^2 d^4} \tag{3}$$

and c is the speed of light.

Fig. 2 illustrates the simulated $\mathrm{SNR} = P_{\mathrm{RX}}/N_{\mathrm{RX}}$ at the receiver output versus frequency for three different integration times. The SNR improves by approximately 30 dB when the IF frequency increases from 10 Hz to 1 MHz. The large SNR gain motivates the use of the proposed transceiver architecture with two VCOs, allowing for finite IF, in contrast to zero-IF

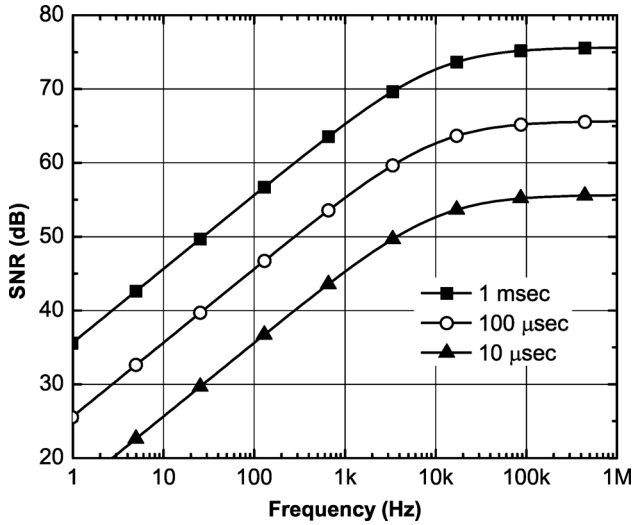


Fig. 2. SNR versus IF frequency for the parameters listed in Table I and variable integration time.

radar transceivers, commonly employed in the W-band (e.g., [20], [21]) that use a single VCO. The penalty is higher system complexity and higher power consumption.

C. Phase-Noise Analysis

The receiver noise floor will typically degrade further due to phase noise. Assuming that the receiver IF and reference outputs of Fig. 1 are multiplied, yielding a final zero-IF output, and accounting for range correlation [22], [23], the phase-noise contribution to the receiver noise floor can be estimated as

$$N_{RX,\mathrm{PN}} = (2P_{\mathrm{RX}}S_\phi B)\cdot\left[4\sin^2\left(2\pi\frac{d\cdot f}{c}\right)\right] \simeq 2P_{\mathrm{RX}}S_\phi B\frac{16\pi^2 d^2 f^2}{c^2} \quad (4)$$

where $10\log S_\phi$ is the single-sideband (SSB) phase noise of the VCO (in dBc/Hz), f is the IF frequency, and B is the IF bandwidth, which is identical to that of (1). Assuming that the VCO phase noise is -100 dBc/Hz at 1-MHz offset from the carrier and that it exhibits a slope of 20 dB/decade between 10 kHz–1 MHz (i.e., $S_\phi = 100/f^2$), the noise-floor contribution becomes

$$N_{\mathrm{RX,PN}} = 2P_{\mathrm{RX}}B\frac{100}{f^2}16\pi^2\frac{d^2f^2}{c^2} = P_{\mathrm{RX}}B\frac{3200\pi^2d^2}{c^2}. \quad (5)$$

At IF frequencies higher than 1 MHz, where the $1/f$ noise contribution can be ignored and N_{RX} is minimized, the ratio $N_{\mathrm{RX}}/N_{\mathrm{RX,PN}}$, calculated from (5), is still larger than 13 dB. This indicates that for a distance of 2 m, the system performance remains largely unaffected by the phase noise of the VCOs, and that it will be limited primarily by the receiver noise figure. It should be noted that there will be an additional phase-noise contribution term due to transmitter leakage. However, because of the even smaller delay, range correlation will be stronger and will also cancel the contribution of this term.

III. Circuit Design

Unlike all other D-band SiGe HBT receivers, transmitters, and transceivers reported to date, which operate from 3.3 V or higher supplies and consume 1.5 W or more, one of the most important goals of this design was to reduce power consumption below 1 W, as needed for a portable system. As a result, a decision was made from the outset to use only circuit topologies that operate from 1.2- or 1.8-V supplies. Telescopic cascodes, which provide large gain at D-band [4] were intentionally avoided and replaced with capacitively or transformer-coupled cascodes or common-emitter topologies.

A. IQ Receiver

The schematic of the IQ receiver is illustrated in Fig. 3. The input signal is first amplified by a three-stage LNA followed by common-emitter transistors Q_5 and Q_6 that double up as transconductors for the I and Q mixers and as an active power splitter. Transformer coupling is employed in the Gilbert-cell mixers that downconvert the 120-GHz RF signal to a low IF frequency. Highly linear unity-gain 50-Ω IF buffers (not shown in the figure) are used as an interface to the external 50-Ω environment.

Due to the small power gain of the transistor at 120 GHz, the LNA design is based on optimizing the noise measure of the transistor, rather than the noise figure [24]–[27]. Following [24], [28], and [29], the noise factor (F) and associated gain (G_A) of the transistor can be expressed as

$$F = F_{\mathrm{MIN}} + \frac{R_{ef}}{G_s}\left[(G_s-G_{of})^2+(B_s-B_{of})^2\right] \quad (6)$$

$$\frac{1}{G_A} = \frac{1}{G_{ma}} + \frac{R_{eg}}{G_s}\left[(G_s-G_{og})^2+(B_s-B_{og})^2\right] \quad (7)$$

where F_{MIN} is the minimum noise factor, G_{ma} is the maximum available gain, G_s+jB_s, $G_{of}+jB_{of}$, and $G_{og}+jB_{og}$ are the admittance of the input source, and the optimum source admittances for F_{MIN} and G_A, respectively.

The expression of the noise measure, M, of an infinite chain of cascaded identical stages becomes

$$M = \frac{F-1}{1-\frac{1}{G_A}} = \frac{F_{\mathrm{MIN}}-1+\frac{R_{ef}}{G_s}\left[(G_s-G_{of})^2+(B_s-B_{of})^2\right]}{1-\frac{1}{G_{ma}}-\frac{R_{eg}}{G_s}\left[(G_s-G_{og})^2+(B_s-B_{og})^2\right]} \quad (8)$$

while the overall noise factor $F_t = 1+M$.

Equation (8) has a global minimum value M_{MIN} at the optimum source admittance $G_{om}+jB_{om}$ [28]. Fig. 4 illustrates the simulated and measured F_{MIN} and G_{ma} at 120 GHz versus current density for a 0.13 μm$\times$ 4.5 μm SiGe HBT in the utilized SiGe BiCMOS technology [2]. Also shown are the minimum noise factor $1+M_{\mathrm{MIN}}$ and the noise factor $1+M_{G_{ma}}$ corresponding to $G_s+jB_s = G_{og}+jB_{og}$ (i.e., source admittance corresponding to the maximum gain) versus current density. The noise factors $1+M_{\mathrm{MIN}}$ and $1+M_{G_{ma}}$ of the infinite chain of cascaded identical stages are based on the measured data, obtained using the methodology described in [30]. Due to the small power gain of the device, less than 5 dB, the minimum noise factor, $1+M_{\mathrm{MIN}}$, attained at a current density of 5–8

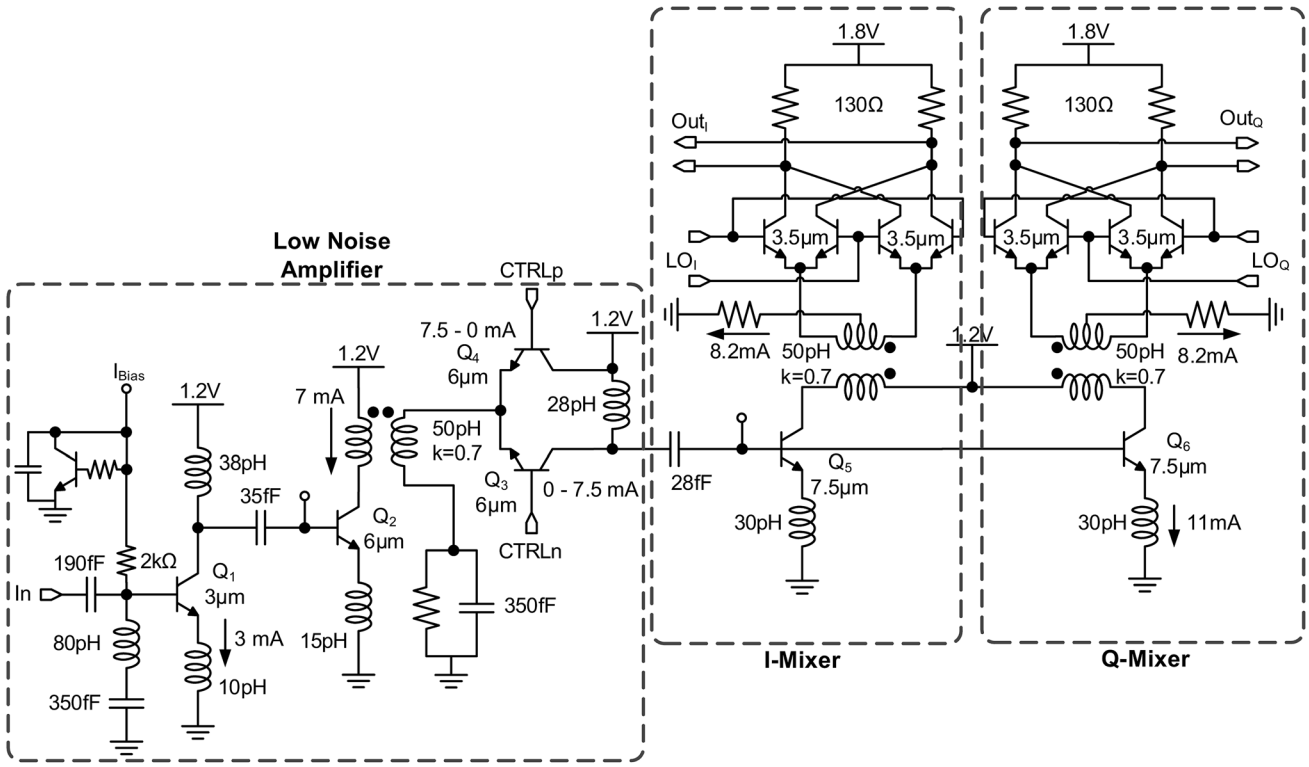


Fig. 3. Schematic of the quadrature receiver.

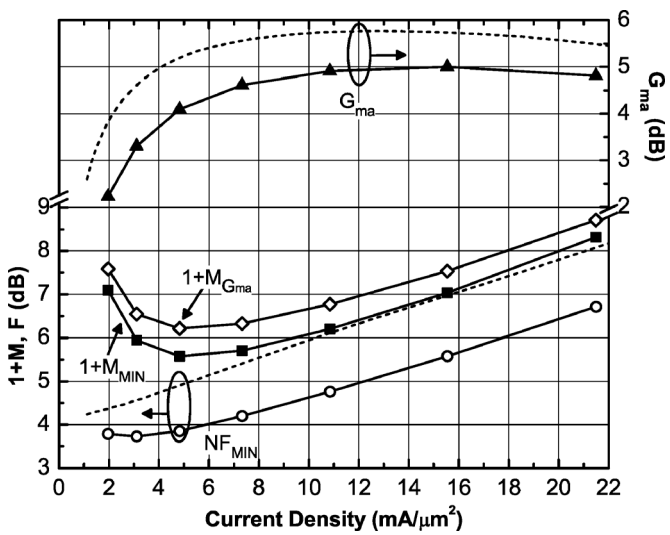


Fig. 4. Measured (lines and symbols) and simulated (dashed lines) maximum available gain (G_{ma}) and minimum noise figure ($F_{\rm MIN}$) for a 4.5-μm device at 120 GHz. The minimum noise measure ($M_{\rm MIN}$) and noise measure $M_{G_{ma}}$, also shown, are extracted from the measured data.

mA/μm^2, is 2 dB higher than the minimum noise factor $F_{\rm MIN}$. Furthermore, if the transistors in the amplifier were matched for maximum gain, the resulting overall noise factor $1 + M_{G_{ma}}$ would be only 0.7 dB higher than $1 + M_{\rm MIN}$.

In the system architecture under consideration, the receiver input needs to be well matched to 50 Ω in order for the 6-dB coupler to be terminated symmetrically. Since the noise factor penalty when matching for G_{ma} is low, directly matching for power ($G_s + jB_s = G_{og} + jB_{og}$) was preferred to using inductive feedback to achieve simultaneous matching for noise and power [31]. Nevertheless, to avoid excessive noise-figure degradation, the first stage of the LNA is biased for low noise, while the second and third stages are biased progressively at slightly higher current densities in order to increase the amplifier gain with negligible impact on the noise figure.

Gain control is implemented in the third common-base stage of the LNA by steering the bias current between transistor Q_3, whose output drives the tuned L–C load, and Q_4, whose collector is connected directly to the power supply. The input impedance of Q_3 in parallel with Q_4 remains constant as the current is steered, ensuring that S_{11} of the LNA does not vary significantly with gain control.

Transistors Q_5 and Q_6, forming the power splitter, are of identical size and loading, guaranteeing that the signal applied at their bases is split equally and in-phase among the I and Q mixers and avoiding unwanted I-Q imbalance [32]. Both the LNA and the transconductor cells operate with a 1.2-V supply.

Since the linearity of the receiver is limited by the mixer, special attention was paid to maximizing its input compression point. To achieve this, Q_5 and Q_6 are biased at the peak f_T current density of 12 mA/μm^2 and their emitter length is set to 7.5 μm, more than two times larger than the size of Q_3. Similarly, the mixing quad transistors have an emitter length of 3.5 μm, forming a one-to-one cascode with Q_5 and Q_6, respectively. The input compression point of the mixer is further improved by inserting 30-pH degeneration inductors at the emitters of Q_5 and Q_6 and by employing a 1.8-V supply for

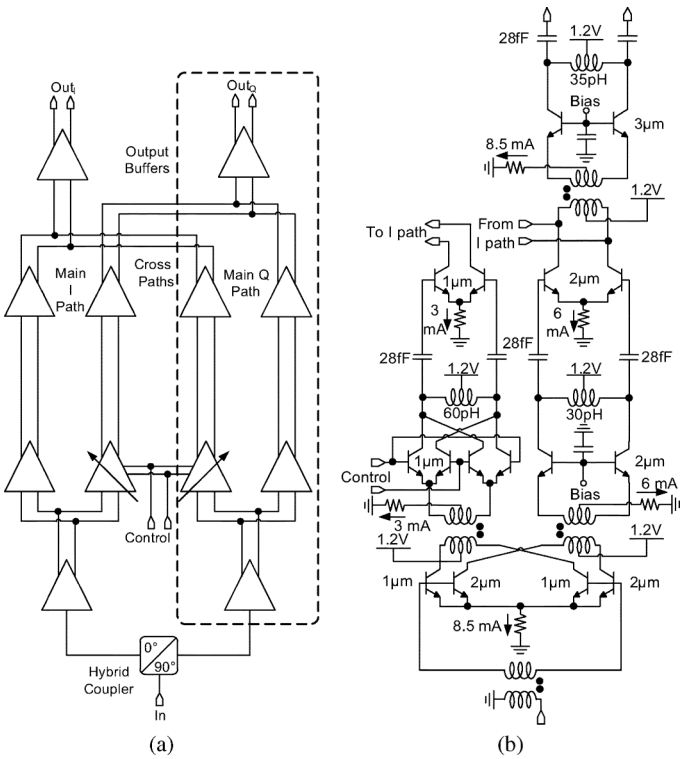


Fig. 5. IQ generation and calibration circuits. (a) Block diagram. (b) Schematic of one of the two parallel paths highlighted in the block diagram.

the mixing quad and IF buffers to maximize the linear output voltage swing.

The simulated conversion gain, input 1-dB compression point, and double-sideband noise figure of each of the I and Q mixers (including signal splitting at Q_5 and Q_6) are 5 dB, -10 dBm, and 18.5 dB, respectively, including the unity gain 50-Ω IF buffers.

Although the linearity of the mixer could, in theory, be improved by further increasing the size of Q_5 and Q_6, the required power consumption of the mixer becomes prohibitively high. As a result, the number of stages in the LNA were limited to three so that the receiver achieves the goal of the -20-dBm input 1-dB compression point at maximum gain. Nevertheless, limiting the number of LNA stages does degrade the overall noise figure of the receiver, resulting in a power-noise-linearity tradeoff where noise is traded for linearity.

The total power consumption of the receiver is 130 mW, including the 50-Ω IF buffers. The simulated receiver downconversion gain, double-sideband (DSB) noise figure, and input compression point from the LNA input to either the I or the Q IF outputs are 13.5 dB, 12.5 dB, and -20.5 dBm, respectively.

B. I-Q Generation and Calibration

Due to possible modeling inaccuracies and layout asymmetries in the I-Q LO distribution circuits, phase calibration is necessary in order to guarantee that the receiver IF outputs are in quadrature.

Fig. 5(a) illustrates the block diagram of the IQ phase correction circuit that splits the LO signal into quadrature outputs and allows for their phases to be calibrated. Calibration is performed by adding weighted I and Q cross paths to the main LO distribution path of opposite phase, i.e., the I cross path is added to the Q main path and vice versa. The operation of the phase correction circuits can be described in the phasor domain as

$$V_{\text{out},I} = Z_L(I_I + kI_Q) = A + kAe^{-j\pi/2} = A - jkA \quad (9)$$

$$V_{\text{out},Q} = Z_L(I_Q + kI_I) = Ae^{-j\pi/2} + kA = kA - jA \quad (10)$$

where I_I and I_Q are the tail currents of the I and Q differential pairs added on the load impedance Z_L, A is the amplitude of the I and Q outputs before calibration (assumed equal), and k is the variable gain of the cross path. The amplitude imbalance and phase difference of the I and Q outputs are given by

$$\left|\frac{V_{\text{out},I}}{V_{\text{out},Q}}\right| = \frac{\sqrt{A^2 + k^2A^2}}{\sqrt{k^2A^2 + A^2}} = 1 \quad (11)$$

$$\angle V_{\text{out},I} - \angle V_{\text{out},Q} = \tan^{-1}\frac{1}{k} - \tan^{-1} k. \quad (12)$$

As a result, under ideal conditions, the amplitude ratio of the I and Q outputs remains constant and the phase difference between $V_{\text{out},I}$ and $V_{\text{out},Q}$ can be varied around 90°, according to the sign of k.

Fig. 5(b) reproduces the transistor-level schematic of the Q path, highlighted in the block diagram of Fig. 5(a). The input signal is first converted from single-ended to differential mode and is split into the main and cross paths using two parallel differential common-emitter amplifiers in a 2:1 size ratio. The output signal from each differential amplifier is coupled via 1:1 symmetrical baluns to a buffer amplifier on the main path, and to a Gilbert-cell variable gain amplifier (VGA) on the cross path. The advantage of using a Gilbert-cell-based VGA is that both variable gain and sign selection are possible. The output of the VGA is then buffered by a differential common-emitter stage before being added to the main I path. This buffering stage is absolutely necessary because the output impedance of the VGA varies with the gain-control setting and would otherwise lead to uncontrolled loading of the main I path, and ultimately to parasitic amplitude modulation. After adding the currents of the main and cross paths at the primary of yet another balun, the resulting output signal is buffered by a 3-μm differential common-base stage to ensure that the output power is sufficiently large to fully switch the HBTs in the mixing quads.

As shown in Fig. 5(a), the input signal to the phase correction circuit is first split into in-phase and quadrature paths by a lumped 90° hybrid, illustrated in Fig. 6(a), which is designed according to the methodology presented in [33]. Fig. 6(b) reproduces the measured and simulated amplitude imbalance and phase difference between the I and Q outputs of the hybrid. To perform the S-parameters measurement, two separate test structures with on-chip 50-Ω terminations were utilized [32], as well as a two-tier de-embedding procedure described in [34]. The 6° disagreement between measurement and simulation of the phase difference is attributed to limitations in modeling the lumped components, as well as to possible deviation of the on-chip terminations from their ideal 50-Ω value, indicating the necessity of calibration.

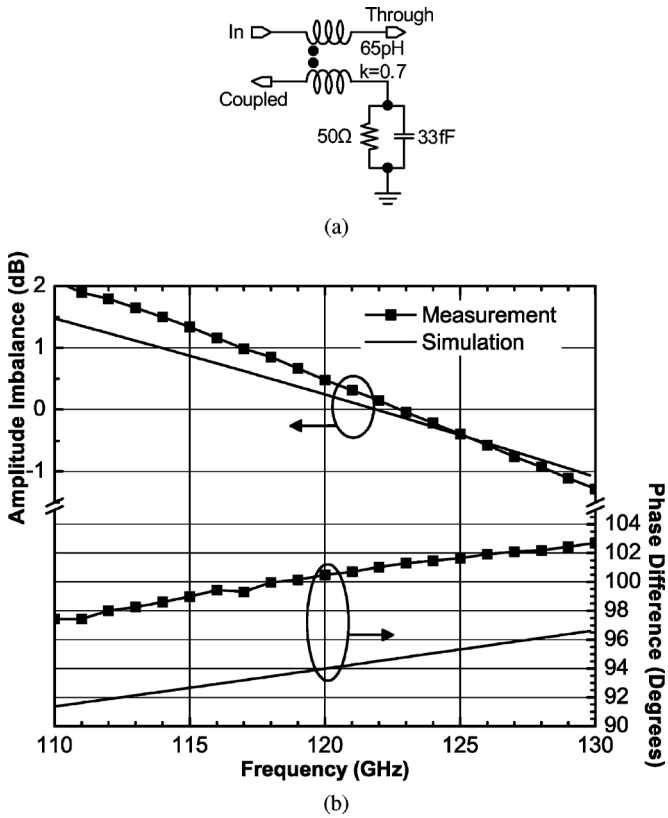


Fig. 6. Quadrature hybrid. (a) Schematic. (b) Measured and simulated results.

The simulated small-signal power gain and phase difference at 122 GHz from the input to the I and Q outputs is illustrated in Fig. 7. A phase adjustment range of 60° to 110° is predicted. The absolute amplitude imbalance between the I and Q outputs is less than 1.8 dB for the entire phase adjustment range. This amplitude imbalance is not predicted by (11) and is due to non-idealities such as unequal delays between the main and cross paths, as well as due to variation of the VGA transmission phase as a function of its gain setting. The power consumption of the I-Q generation and calibration circuit is 92 mW from a single 1.2-V power supply.

C. VCO

The schematic of the 120-GHz fundamental frequency VCO is shown in Fig. 8(a) and follows a differential Colpitts topology [35], a common choice for low phase-noise millimeter-wave VCOs [36]–[38]. In order to achieve low phase noise, a single transistor topology is employed. It has the added benefit of operation from a low-voltage supply, avoiding the use of a stacked common-base buffer [37], [39].

In order to maximize the quality factor of the tank, multifinger double-side contacted 130-nm accumulation-mode MOS varactors with 1-μm-wide gate fingers were employed. The measured quality factor of these varactors is 4–16 in the D-band [30], and is typically higher than that of pn-junction varactors [30], [38], while their measured $C_{\max}/C_{\min}$ ratio is 2:1 [30] with a voltage tuning range that is CMOS compatible (0–1.2 V). Moreover, in order to maximize the voltage swing on the oscillator tank and thus minimize phase noise, the HBT emitter length is set to the largest possible value that still permits a reasonable tank inductance value, 7.5 pH in this case. The HBTs are biased at their peak-f_T current density, guarantying the oscillation condition [38] and large output power.

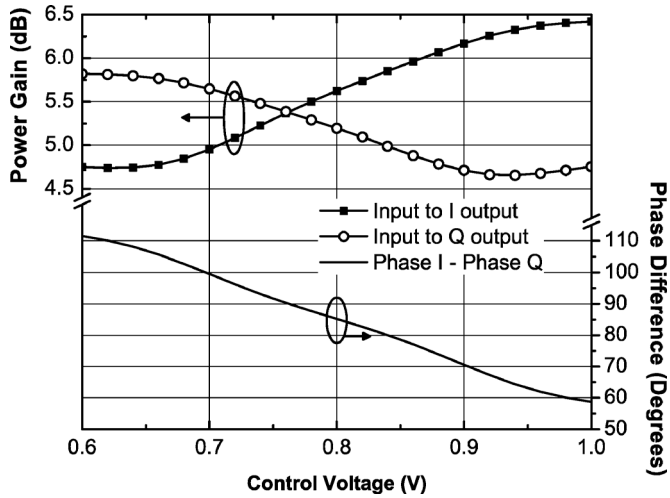


Fig. 7. Simulated performance of the I-Q generation and calibration circuit at 122 GHz.

To simplify the design of the external PLL and to minimize the PLL noise contribution and spurs, coarse and fine control of the VCO frequency is provided by two groups of varactors. The grouping for coarse control has a total varactor size of $13 \times 1\ \mu\text{m} \times 0.13\ \mu\text{m}$ and can be adjusted once, at power up, to bring the VCO frequency close to the intended value. A $3 \times 1\ \mu\text{m} \times 0.13\ \mu\text{m}$ varactor is used for fine tuning as part of the PLL. This arrangement minimizes the VCO gain in the PLL. Single-ended controls were preferred in order to simplify the chip interface with the external loop filter.

A previous version of this VCO [8], [10] featured a single differential control voltage, as shown in Fig. 8(b). Half of the varactors have the gates connected to the tank, while the other half have their n-wells tied to the tank. Although this arrangement reduces the common-mode noise and yields better phase noise, the varactors with the n-well connected to the tank introduce additional parasitic capacitance and reduce the overall VCO tuning range. The VCO with single-ended controls is expected to have wider tuning range and slightly higher phase noise than that in [8] and [10].

Optimization of the symmetrical VCO layout is crucial to achieve the intended oscillation frequency and tuning range at D-band. The 7.5-pH tank inductors were formed as a single 5-μm-wide inductive line with the top two copper layers shunted together for a total thickness of 6 μm in order to be able to precisely control the inductance. Fig. 8(c) reproduces the die microphotograph of a VCO breakout.

The total power consumption of each VCO is 76 mW from a 1.8-V power supply.

D. LO Distribution

Distributing the 120-GHz LO signal to a relatively large number of circuits without degrading its amplitude is a challenging task. Passive power splitting has been employed at lower frequencies (e.g., [40]–[43]). However, such an approach

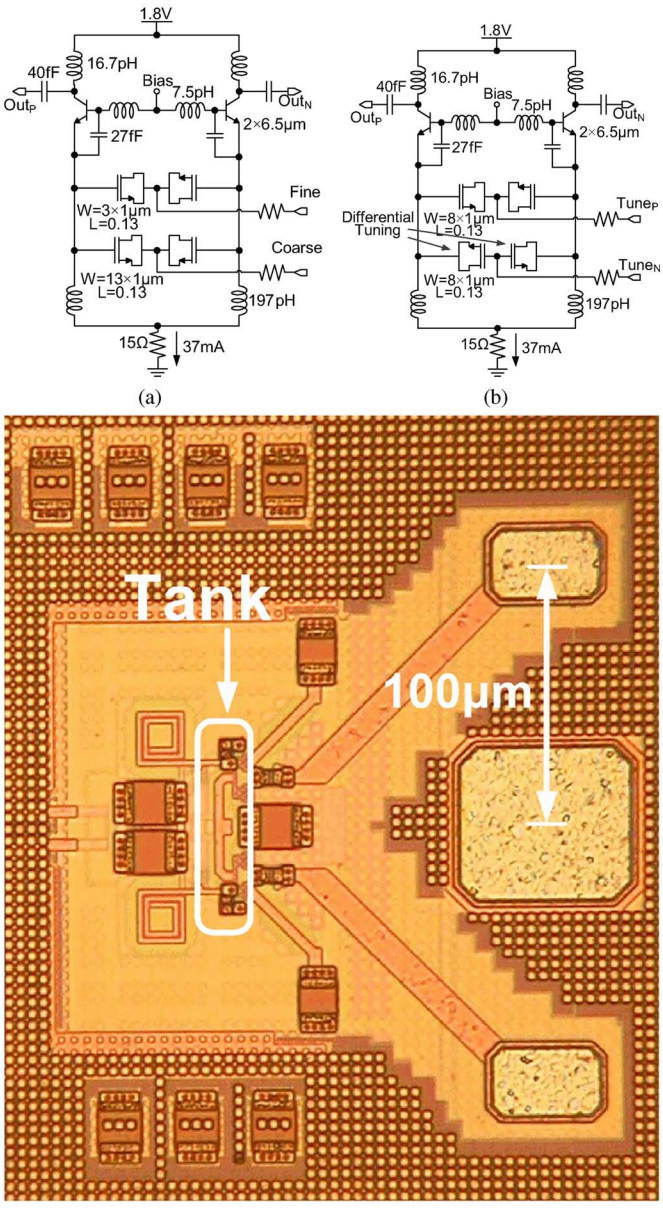


Fig. 8. 120-GHz Colpitts VCOs. (a) VCO with single-ended control. (b) VCO with differential control. (c) Die microphotograph.

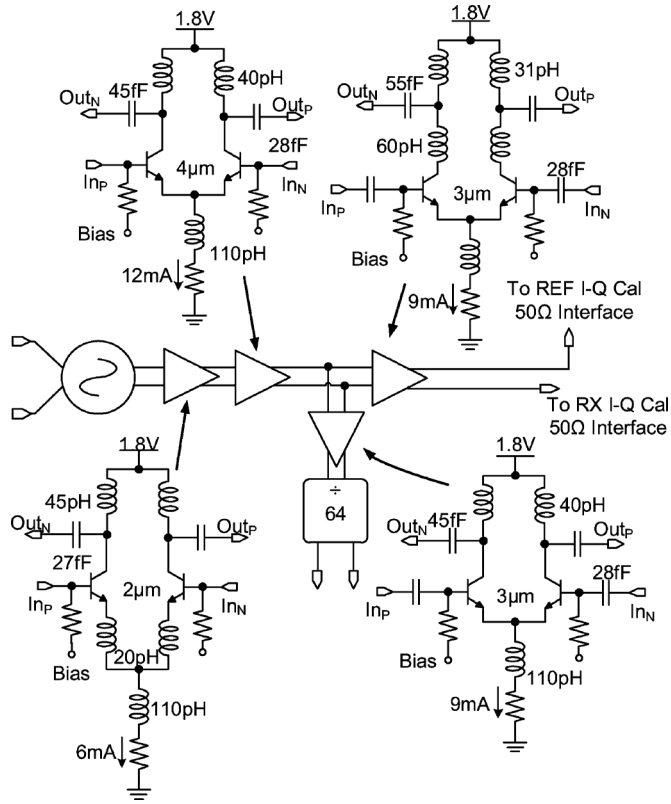


Fig. 9. Receive VCO signal distribution.

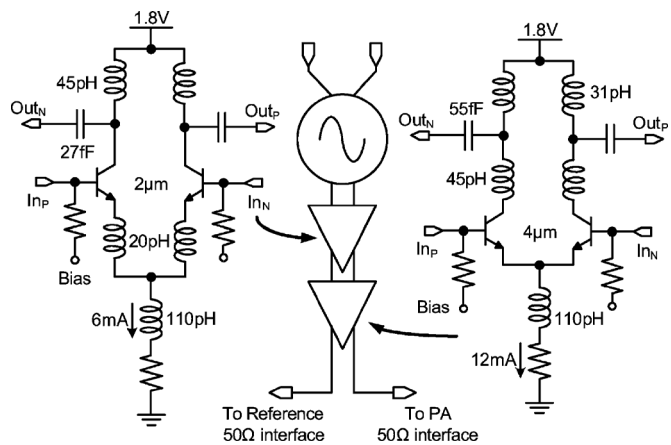


Fig. 10. Transmit VCO signal distribution.

would suffer from very high insertion loss, which, ultimately, requires very powerful buffers to be placed at the output of the VCO. In order to avoid designing such buffers, an active power distribution solution was preferred, as illustrated in Figs. 9 and 10 for the cases of the receive VCO and the transmit VCO, respectively.

The first set of buffers, placed immediately after the VCOs, employ the smallest transistor size in order to avoid overloading the VCO, which would endanger the oscillation condition. Furthermore, in order for the two VCOs to be loaded similarly and to oscillate in the same frequency range, these buffers are identical for both the TX and RX LO trees. The second-level buffers are scaled by a factor of two (4 μm) and operate close to their 1-dB output compression point, ensuring that their output power is sufficiently large to drive the subsequent stages in compression. The third set of buffers in the receiver LO tree have their inputs connected in parallel and the transistor size is selected such that the divider receives adequate input power to guarantee proper frequency division.

Conjugate power matching with L-sections was employed between buffer stages, whereas Π-matching networks were used at the 50-Ω interfaces (Figs. 9 and 10) since the corresponding L-sections would require very small capacitors and would result in very narrow bandwidth. Common-mode inductors and resistors are introduced to increase the common-mode rejection ratio and improve the bias stability. All transistors in all buffers are biased at the peak-f_T current density.

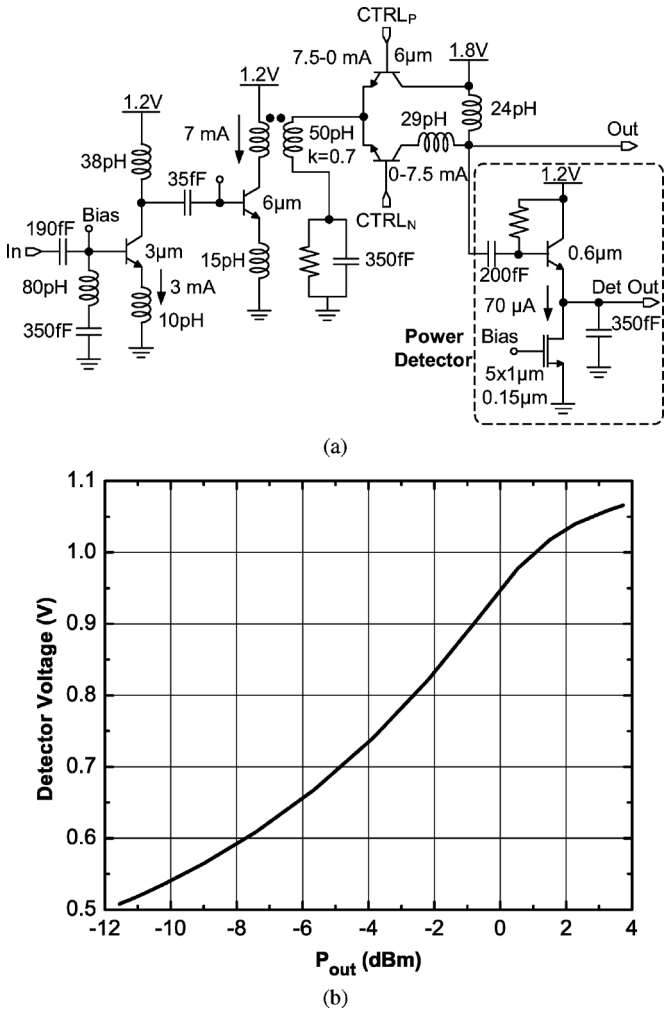


Fig. 11. Transmit amplifier schematic and simulation results. (a) Schematic of the variable gain transmit amplifier. (b) Simulated power detector output voltage versus amplifier output power at 122 GHz. The output power is varied through the gain control function.

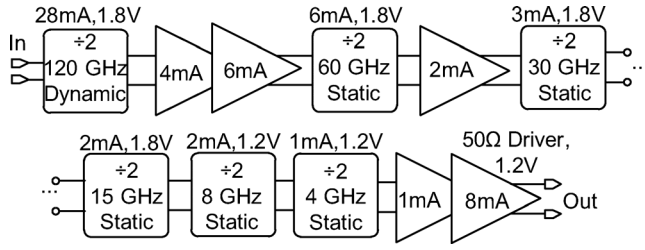


Fig. 12. Block diagram of the divider chain.

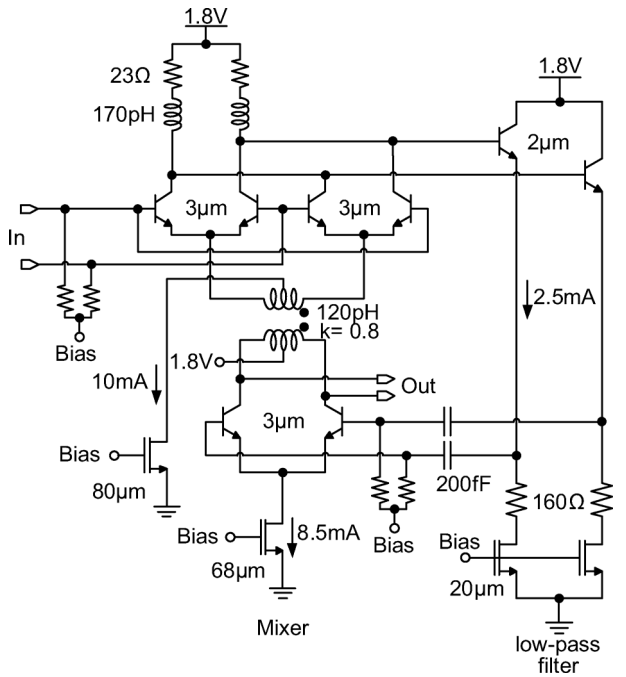


Fig. 13. Schematic of the 120-GHz dynamic divider.

The LO distribution network in the receiver delivers +4 dBm to the divider and +1 dBm to each of the I-Q generation and calibration circuits at 120 GHz, while consuming 90 mW from a single 1.8-V power supply. The transmitter LO distribution tree delivers +1 dBm to the transmit amplifier and to the reference downconverter while consuming 40 mW from 1.8-V power supply.

E. Transmit Amplifier

The schematic of the transmit amplifier is illustrated in Fig. 11(a) and is identical to that of the LNA, except for the power supply voltage of the last stage, which was increased to 1.8 V in order to ensure that the output power is at least 0 dBm. The output network was modified to facilitate 50-Ω matching.

The power detector function is realized with a common-collector HBT biased at a low current density using a MOS current source [44]. The detector is ac-coupled through a 200-fF capacitor to the output of the amplifier. The smallest HBT size was selected in order to minimize the loading of the amplifier. The simulated power detector output voltage versus the output power of the transmit amplifier is reproduced in Fig. 11(b).

F. Divider Chain

The block diagram of the divider chain is reproduced in Fig. 12 and consists of a 120-GHz dynamic divider stage, chosen for its high operation frequency[45], [46], followed by 1.8- and 1.2-V static current-mode logic (CML) dividers. Two cascaded CML-buffers were inserted between the 120- and 60-GHz divider stages to boost the signal level over all process, supply, and temperature corners. A single CML buffer was placed between the 60- and 30-GHz divider stages for the same purpose.

The schematic of the 120-GHz dynamic divider is shown in Fig. 13. It features a low-voltage Gilbert-cell mixer and a low-pass filter formed by a pair of ac-coupled emitter followers, the 200-fF series capacitors and the input resistance of the differential transconductor pair. The LO signal is applied directly to the mixing quad. In order to facilitate operation from a 1.8-V supply, transformer and capacitive coupling is employed in the feedback path between the transconductor pair and the mixing quad, and between the emitter followers and the transconductor pair, respectively.

An earlier version of the dynamic divider [8], [10] used transformer coupling also between the emitter followers and the transconductor pair. Simulation predicts that replacing

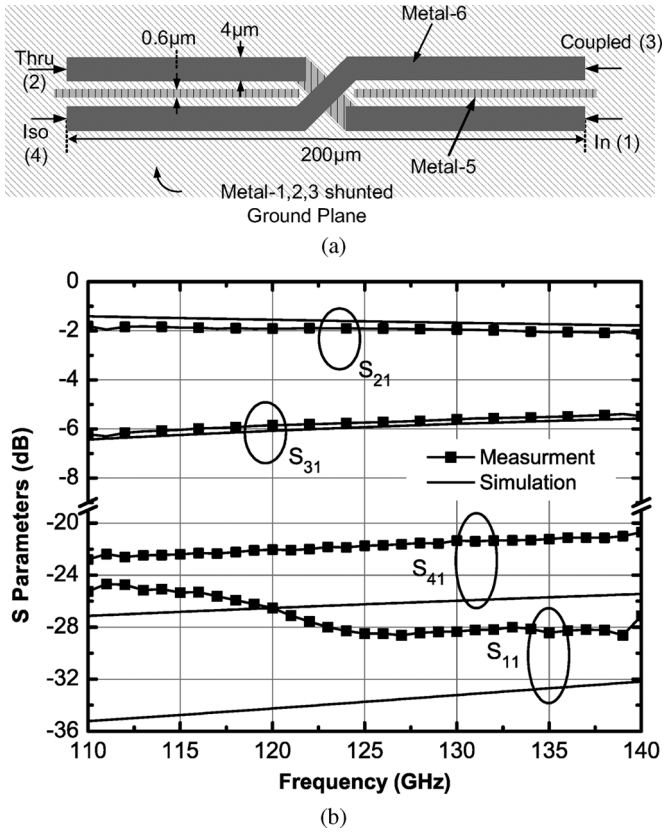


Fig. 14. 6-dB coupler. (a) Sketch. (b) Measured and simulated S-parameters.

the transformer with a pair of metal–insulator–metal (MiM) capacitors increases the maximum division frequency by approximately 5 GHz. However, replacing the second transformer between the transconductor and the mixing quad is more difficult since four inductors and two capacitors would be needed to provide loads to the transconductors, the ac coupling, and the supply current, resulting in unacceptably narrowband operation and larger area.

The penalty for ac coupling the feedback path in dynamic dividers is an increase in the lowest division frequency [47]. However, this is partially circumvented by the higher transistor gain at lower frequencies. The simulated division range of the dynamic divider extends from 130 GHz down to 80 GHz.

The simulated power consumption of the entire divider chain is 115 mW from 1.2- and 1.8-V power supplies.

G. 6-dB Coupler

The sketch of the coupled-line, 6-dB antenna coupler is illustrated in Fig. 14(a) [8]. The two coupled lines are realized in the top 3-μm-thick metal layer (M6), while the ground plane is realized with the bottom three metal layers shunted together. In order to meet the required metal density rules, a floating bar in metal 5, located 1.5 μm below the top metal layer, is inserted between the two arms of the coupler. The width of the floating bar is chosen to improve the overall isolation of the coupler by optimizing the matching between the even- and odd-mode velocities [48], [49].

A comparison between the measured and simulated S-parameters of the 6-dB coupler is reproduced in Fig. 14(b). The 6-dB

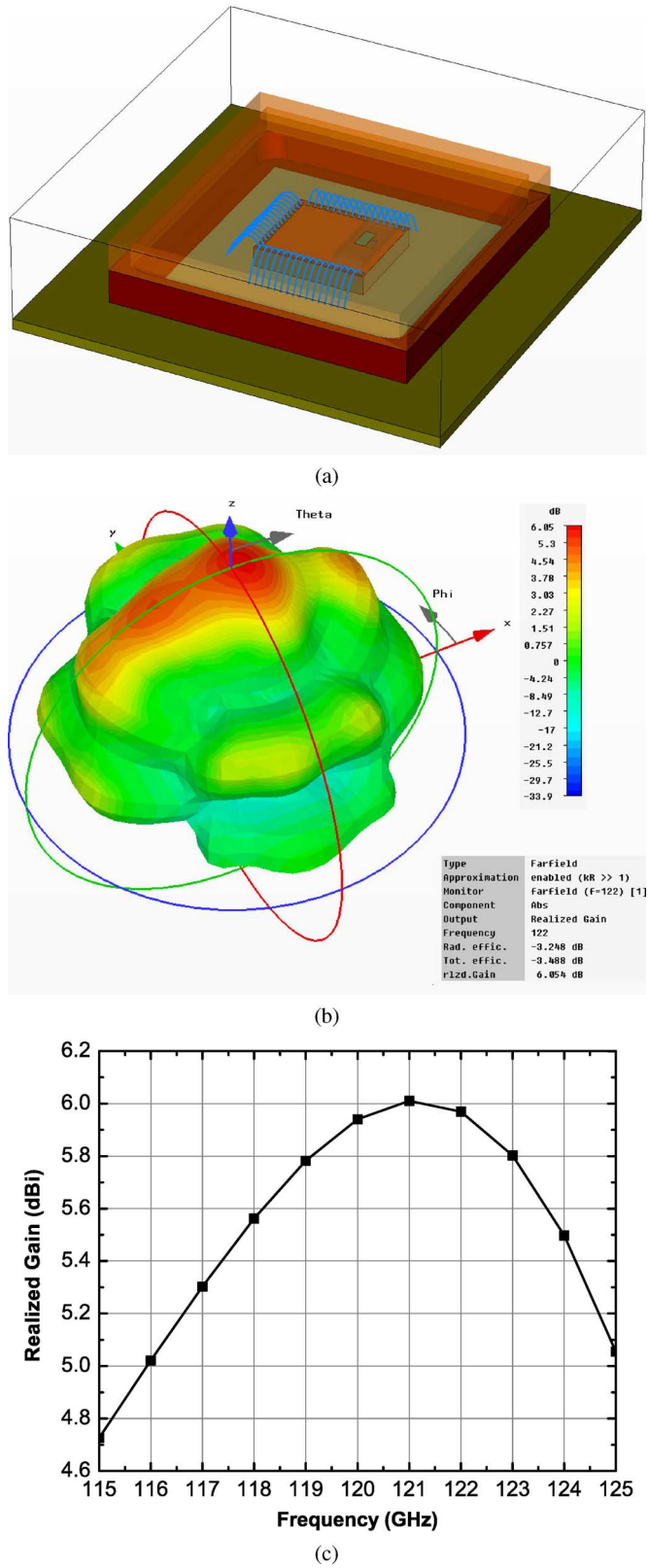


Fig. 15. Simulated performance of the antenna. (a) Antenna simulation CAD model. (b) 3-D radiation pattern. (c) Simulated gain versus frequency, including mismatch losses.

coupler was also characterized using two separate test structures with on-chip terminations. The loss of the "thru" arm remains below 2 dB at 120 GHz, while the isolation and input reflection

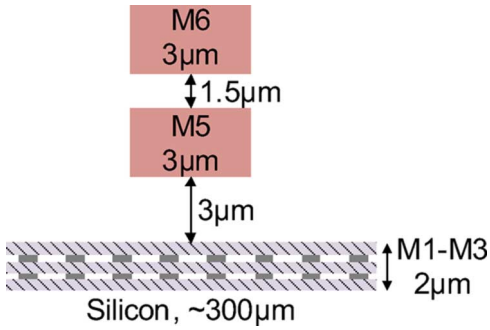


Fig. 16. Cross section of the BEOL.

TABLE II
QUALITY FACTORS OF PASSIVE COMPONENTS

Component	Q factor/loss @ 120 GHz
30 pH inductor	18
28 fF capacitor	22
50 pH 1:1 transformer	13*
50 Ω microstrip transmission line (12 μm wide M6)	0.8 dB/mm

* $Q_{11} = \frac{Im(Z_{11})}{Re(Z_{11})}$

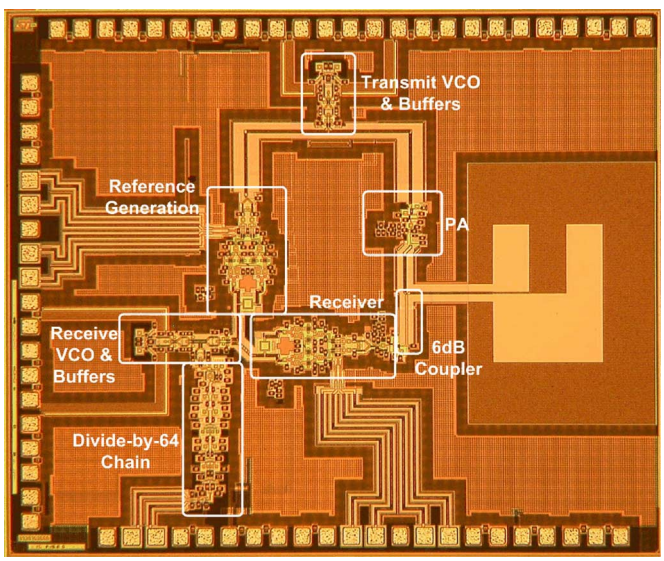


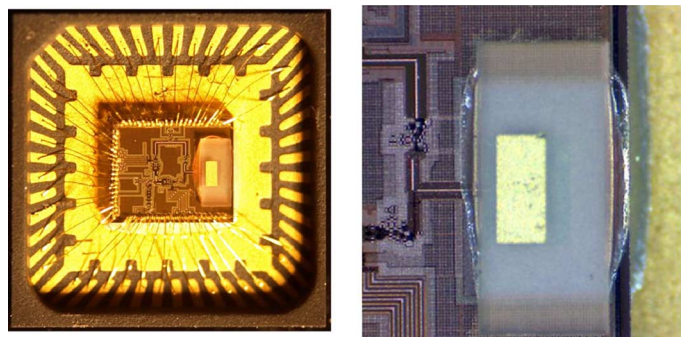
Fig. 17. Die microphotograph. The dimensions are 2.2 mm × 2.6 mm.

are better than 20 dB. Very good matching between the simulated and measured "thru" and "coupled" transmission coefficients is achieved. The measured reflection coefficient and isolation slightly deviate from their simulated values. However, it is difficult to know if this is due to a design inaccuracy or because of deviations and mismatches of the on-chip terminations.

IV. ANTENNA DESIGN, FABRICATION, AND PACKAGING

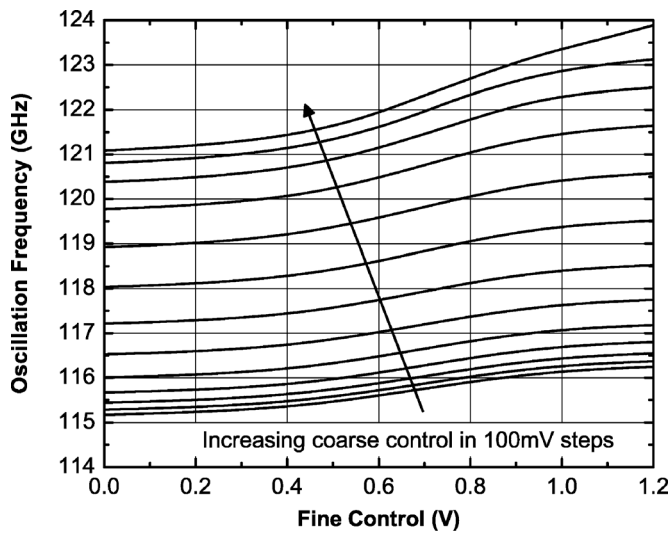
A. Antenna Design

The antenna is a frequency-scaled version of the antenna presented in [17] and consists of a shorted patch on-die feed radiating from one side, electromagnetically coupled to an external

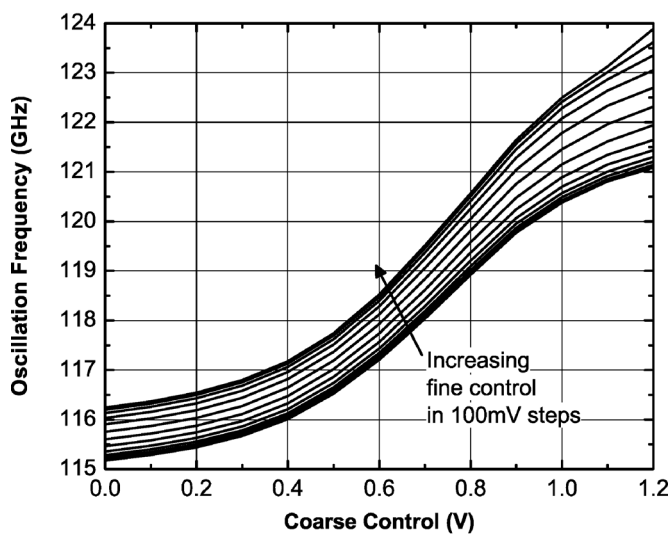


(a) (b)

Fig. 18. Packaged transceiver. (a) Transceiver mounted in a QFN package. (b) Close-up view of the quartz resonator.



(a)



(b)

Fig. 19. Measured VCO tuning range. (a) Tuning range versus fine control. (b) Tuning range versus coarse control.

$\lambda/2$ patch resonator. The latter is manufactured on a low-loss quartz substrate.

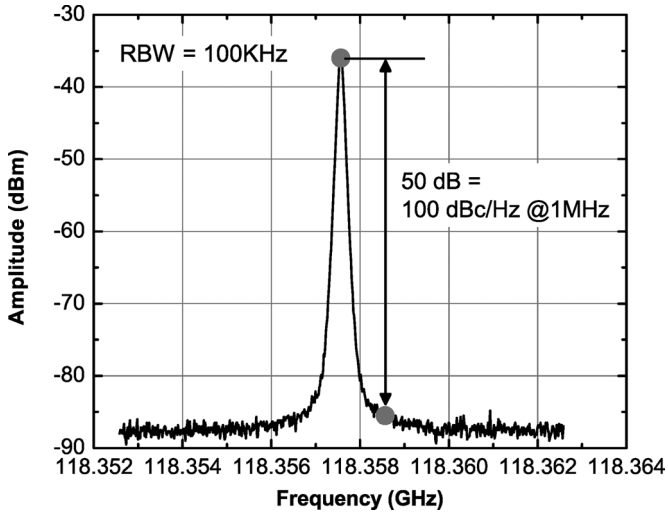


Fig. 20. Measured phase noise of the VCO at 118 GHz.

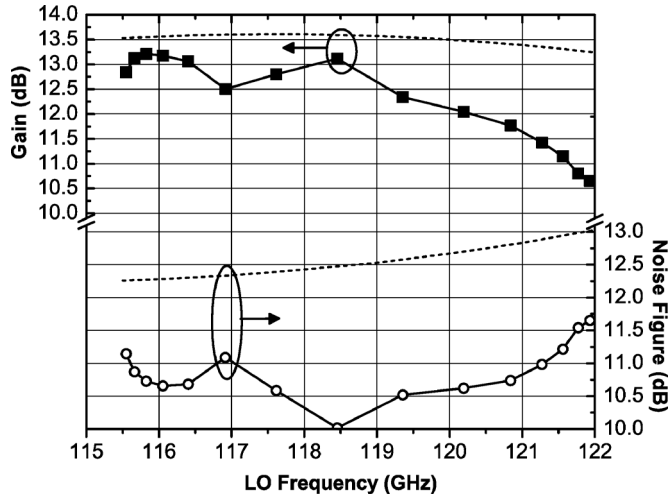


Fig. 22. Measured (lines and symbols) and simulated (dashed lines) DSB noise figure and downconversion gain of the receiver breakout.

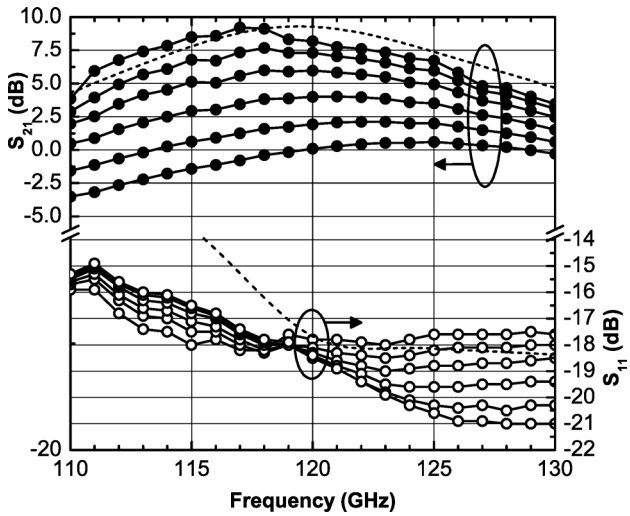


Fig. 21. Measured (lines and symbols) S-parameters of the LNA breakout for six gain settings. The dashed lines correspond to simulations at maximum gain.

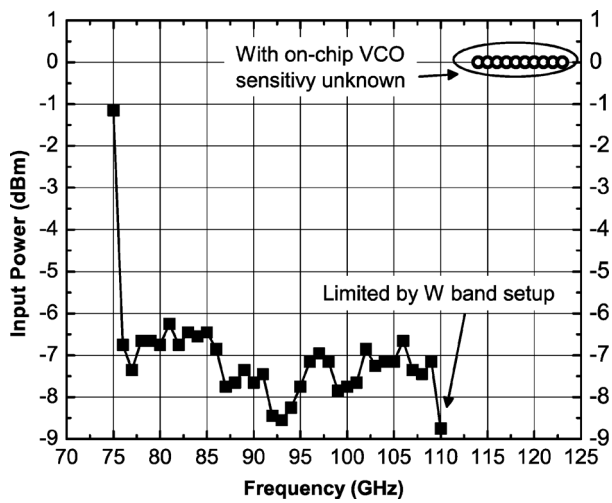


Fig. 23. Measured sensitivity of the divider chain.

The antenna was simulated along with the package and the bondwires in a 3-D electromagnetic (EM) simulator, as illustrated in Fig. 15(a). The gain and radiation pattern are reproduced in Fig. 15(b). The simulated antenna gain and efficiency are 6 dBi and 50%, respectively, including the mismatch loss. The simulated antenna 1-dB bandwidth of 9 GHz is shown in Fig. 15(c).

Similar antenna solutions with comparable performance have also been reported at 94 GHz in [18] and [19].

B. Fabrication and Packaging

The transceiver was fabricated in STMicroelectronic's BC9MW 130-nm SiGe BiCMOS process [2], which features heterojunction bipolar transistors (HBTs) with f_T/f_{MAX} of 230/280 GHz, 130 nm MOSFETs, and six copper layers, the top two being 3-μm thick, as illustrated in the cross section of Fig. 16. These top two metal layers (M5–M6) and the 2-fF/μm^2 MiM capacitors were employed to realize all of the high-frequency passive components, while the bottom three (M1–M3) were utilized for the ground plane.

The passive components (inductors, transformers, couplers, and transmission lines) were designed using two commercial planar EM simulators (Agilent Momentum and Sonnet). Furthermore, the design methodology and the simulation accuracy of the passive components have been verified in many cases using D-band S-parameter measurements [34]. Table II summarizes the quality factors of some characteristic frequently used passive components.

Fig. 17 shows a die microphotograph of the transceiver, which occupies 2.2 mm $\times$ 2.6 mm. Several 0.3-pF capacitors have been employed for bias decoupling in all circuit blocks in order to ensure circuit stability and proper power supply noise filtering. In addition to surrounding the receiver, VCOs, and divider with ground shields to avoid noise coupling, their power supplies are provided from separate pads and employ isolated supply planes [50].

The physical distance from the transmit VCO and amplifier to the rest of the circuits has been maximized in an effort to

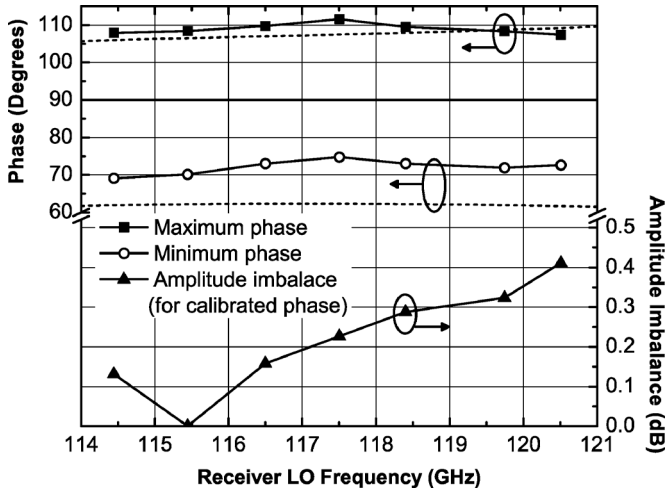


Fig. 24. Measured (lines and symbols) and simulated (dashed lines) phase adjustment range of the I-Q receiver and amplitude imbalance when the phase is calibrated.

minimize the leakage from the transmitter to the receiver and to reduce the frequency range over which the TX and RX VCOs are injection locking.

The chip is mounted in an open-lid quad-flat no-leads (QFN) package with the external quartz antenna glued on top of the chip, as illustrated in Fig. 18(a). Fig. 18(b) shows a close-up view of the resonator glued on the chip.

V. Measurement Results

The antenna coupler, the on-chip power detector, and the phase generation and calibration circuits allow for the verification of the functionality and for some of the quantitative performance parameters of the packaged transceiver to be evaluated without millimeter-wave equipment and measurements. At the same time, due to the difficulty of accurately quantifying all performance parameters of the integrated transceiver with antenna through free-space measurements, and in order to evaluate the performance of the individual blocks, several breakouts of the transceiver circuits were fabricated and characterized separately on wafer.

A. Breakouts

1) VCO: The VCO was characterized: 1) as a standalone breakout; 2) in a breakout that includes the VCO and the divider chain; 3) in the receiver breakout; and 4) in the packaged transceiver at the divider output. Fig. 19 reproduces the measured tuning range of the VCO at the IF output of the receiver, when the fine tuning control is swept from 0 to 1.2 V for different values of the coarse tuning control [see Fig. 19(a)] and [see Fig. 19(b)] when only the fine control is swept. The tuning range spans 8.7 GHz from 115.2 to 123.9 GHz.

Fig. 20 illustrates the measured -100 dBc/Hz at 1-MHz phase noise of the VCO at 118 GHz. This is on par or better than that of other state-of-the-art SiGe HBT VCOs in this frequency range [5], [51] and approximately 3–5 dB worse than the VCO version with differential control in [8].

2) LNA: The S-parameters of the LNA were measured in a separate breakout using a D-band VNA. The S_{21} and S_{11} for

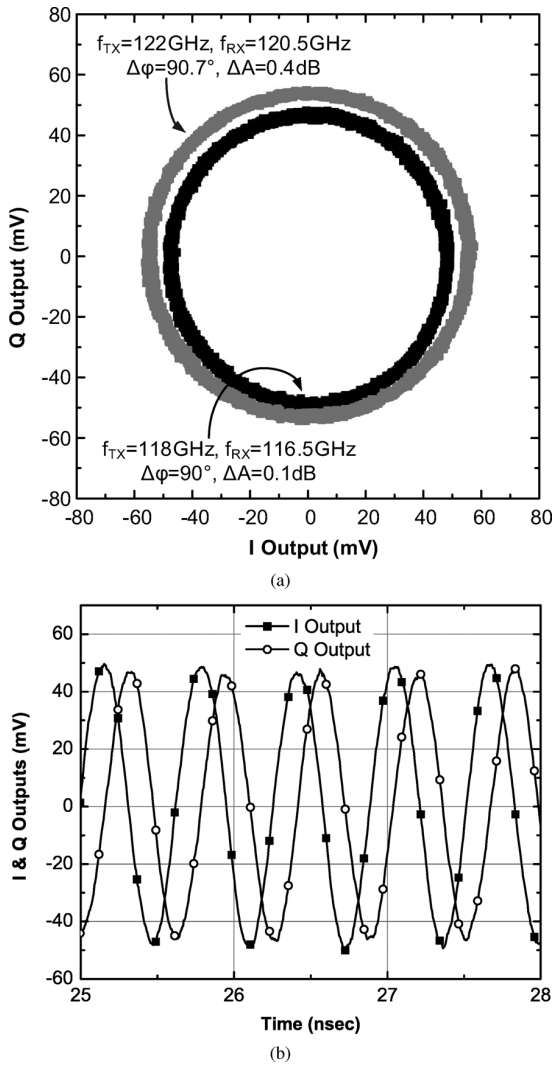


Fig. 25. Quadrature receiver outputs. (a) XY plot of the receiver IQ outputs at two frequencies. (b) Time-domain signals when $f_{\rm TX} = 122$ GHz.

the first few gain settings are depicted in Fig. 21. The dashed lines correspond to simulations in the highest gain state. The S_{11} variation with gain has been minimized by using the gain control technique described in Section III-A. Good agreement between simulation and measurements has been achieved due to careful modeling of all interconnects and passive components. Similar results, but with slightly higher S_{21}, were obtained for the transmit amplifier.

3) Receiver: A separate receiver breakout was characterized with an ELVA-1 D-band noise source. The measured single-ended conversion gain and DSB noise figure (from the RF input to the I IF output), at a 500-MHz IF frequency, are shown in Fig. 22. Since the 50-Ω IF buffers have no gain, the entire downconversion gain is achieved by the RF front-end alone. Although in this application the gain of the LNA had to be limited in order to preserve the overall linearity of the receiver, the 10–11.5-dB receiver noise figure is comparable to those of other D-band transceivers fabricated in technologies with similar performance [5], [6], [9]. The measured noise figure is 2 dB better than simulation, consistent with many other results obtained with this design kit [30], [52] and is attributed to the inadequate capturing of the correlation between

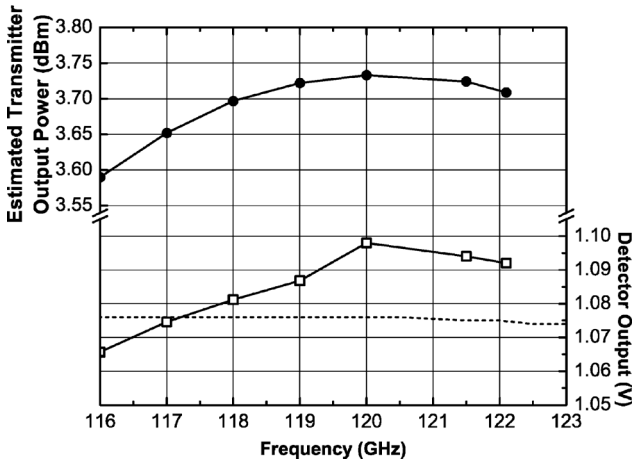


Fig. 26. Measured (lines and symbols) and simulated (dashed line) on-chip power detector output voltage versus frequency and transmitter output power based on the simulated performance of the detector.

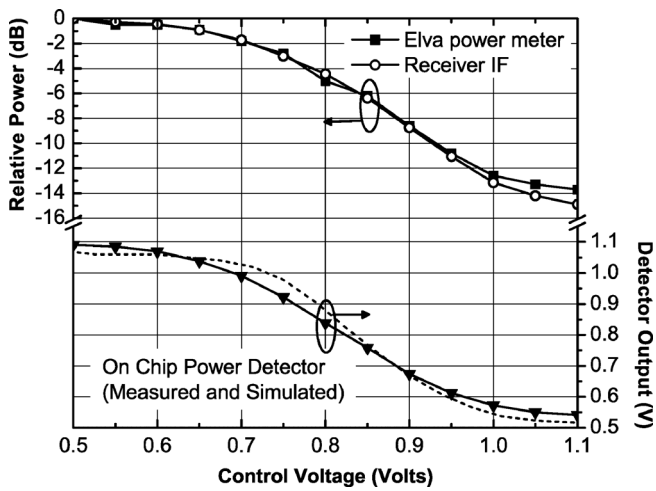


Fig. 27. Transmitter output power versus control voltage measured with a power meter, at the IF receiver outputs, and at output of the on-chip power detector at 122 GHz.

the collector and base noise currents and to an overestimation of the noise resistance [30], [53].

4) Divider Chain: The divider chain was characterized as part of the transceiver and as a standalone divider-chain breakout. The measured sensitivity is reproduced in Fig. 23 and hovers at -7 to -8 dBm for input signals in the 76–110-GHz range. *D*-band operation was also verified between 115–123 GHz, when the divider chain is driven by the VCO. However, the absolute value of the sensitivity in this frequency range is unknown since there are no means to control and measure the power at the input of the divider.[1]

B. Transceiver

1) Receiver: Although the transceiver with the on-die antenna feed could not be wafer-probed, certain measurements could be carried out on the packaged chip, mounted on the printed circuit board (PCB), by taking advantage of the leakage

[1]The available source does not provide sufficient power to measure the sensitivity of the standalone divider chain.

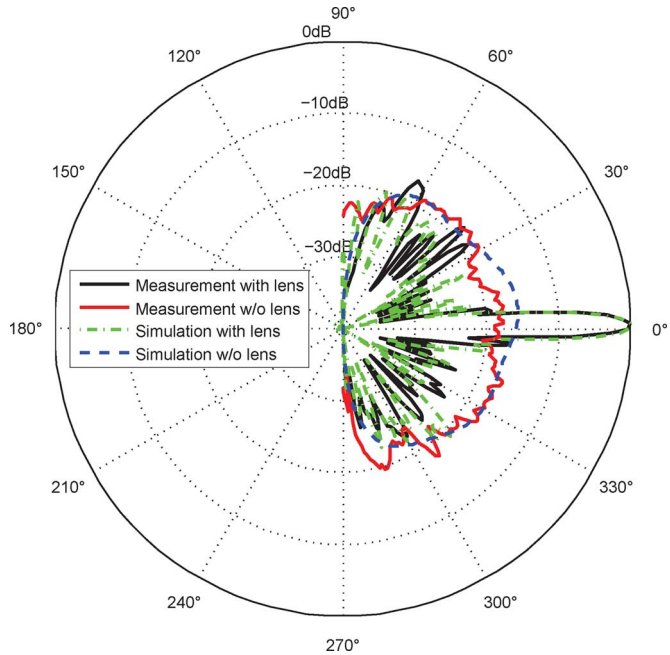


Fig. 28. Measured and simulated *H*-plane normalized antenna radiation patterns with and without the focusing lens.

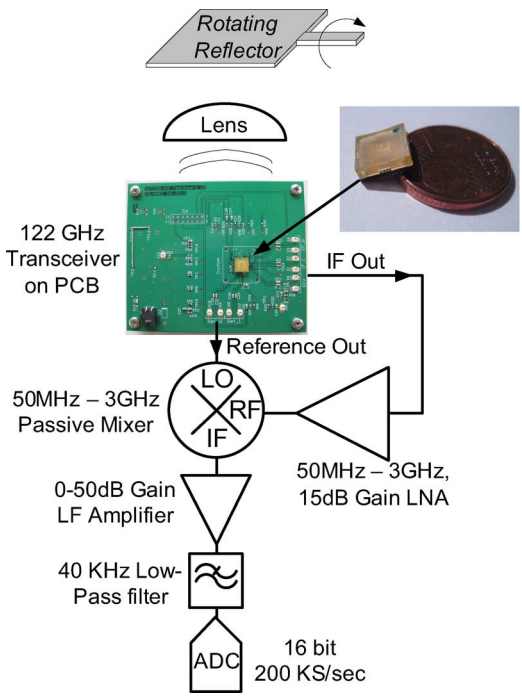


Fig. 29. Rotation speed test setup.

from the transmitter to the receiver and of the detector placed at the output of the transmitter.

The IF outputs of the receiver and divider chain were monitored with a spectrum analyzer and an oscilloscope, and the injection-locking properties of the two VCOs were analyzed. As the frequency difference between the transmit and receive VCOs, and thus the IF frequency, was decreased to less than 1 GHz, the harmonics of the IF signal started to emerge and modulating tones appeared in the divided-down receive VCO

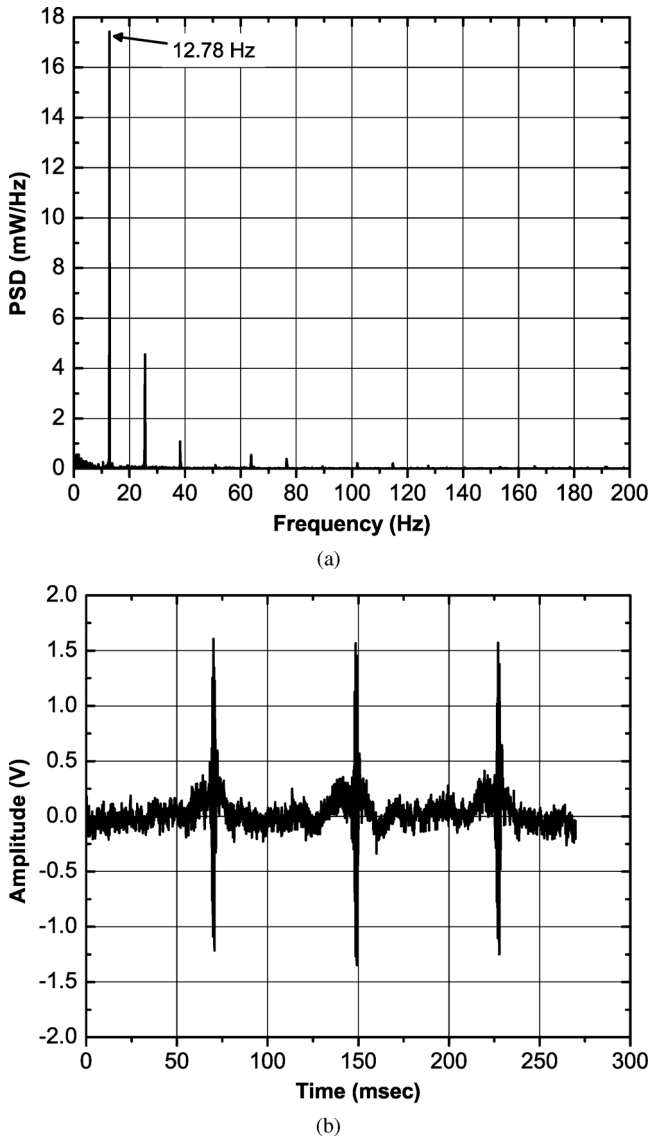


Fig. 30. Measured speed of a rotating reflector placed at 30 cm above the board. (a) Spectrum. (b) Time-domain signal.

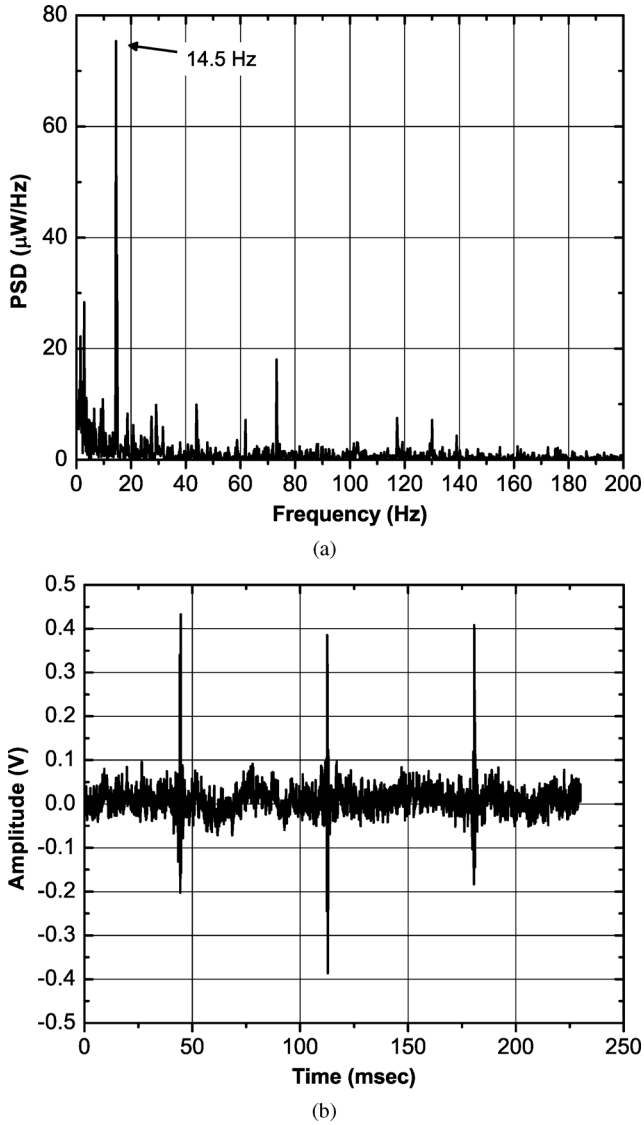


Fig. 31. Measured speed of a rotating reflector placed at 2.1 m above the board. (a) Spectrum. (b) Time-domain signal.

spectrum. In order to avoid this injection-locked mode of operation, the rest of the transceiver measurements were performed with 1.5-GHz frequency offset between the transmitter and receiver VCOs. The upper limit of the IF frequency is 5 GHz due to receiver bandwidth and package limitations.

The phase difference and phase adjustment range of the I and Q IF outputs were measured by taking advantage of the leakage from the transmitter to the receiver. Fig. 24 reproduces the measured phase adjustment range of the I and Q outputs of the receiver as a function of the LO frequency. The phase difference can be adjusted from 70° to 110°, which agrees reasonably well with the simulated values. The discrepancy between measurements and simulations in the lower range is attributed to the mismatch between the measured and simulated performance of the quadrature hybrid, as well as to other layout imbalances in the mixer that were intended to be calibrated with this circuit.

Also shown in Fig. 24 is the measured amplitude imbalance between of the I and Q receiver outputs when the phase is calibrated to be exactly 90° for each receiver LO frequency. The amplitude imbalance remains less than 0.4 dB (better than simulation due to the saturated operation of the mixer in the LO port) for the entire range, and could be easily compensated by including variable gain in the baseband amplifiers.

Fig. 25(a) reproduces an X–Y plot of the calibrated I and Q receiver outputs for two LO frequencies while the corresponding time domain signals are shown in Fig. 25(b).

TABLE III
POWER CONSUMPTION

Block	Count	Power per instance (mW)
VCO	2	2×76
Divider chain	1	115
I-Q generation and calibration	2	2×92
Receiver	1	130
LO distribution	2	90 (RX), 40 (TX)
Reference generation	1	100
Transmit amplifier	1	35
Total (including bias)		**900**

TABLE IV
PERFORMANCE COMPARISON

	f_0 (GHz)	G_{RX} (dB)	NF (dB)	P1dB (dBm)	P_{out} (dBm)	PN (1MHz) (dBc/Hz)	P_{DC} (W)	f_T/f_{MAX} (GHz)	Notes
[5]	122	21	11	-44	-	-94	0.37	245/350 SiGe	Receiver 2×60 GHz
[6]	140	30	12	-	-8	-80	1.5	230/280 SiGe	Transceiver 2×70 GHz
[9]	160	-	-	-	1	-89	1.7	260/380 SiGe	Transmitter 9×17.7 GHz
[9]	160	25	14	-	-	-89	1.5	260/380 SiGe	Receiver 9×17.7 GHz
[51]	122	-	-	-	2	-95	0.35	210/240 SiGe	Transmitter 1×122 GHz
[16]	118	-	-	-	-8	-	0.2	65nm CMOS	Transmitter ext. LO
[54]	220	3.5	7.4	-	-	-	0.11	200/300 GaAs	Receiver 4×55 GHz
[55]	123	3	5	-	-	-	0.12	200/300 GaAs	Receiver 4×30 GHz
This Work	122	13	11.5	-20	3.6*	-100	0.9	230/280 SiGe	Transceiver 1×122 GHz

* At transmitter output, not including the antenna coupler and antenna

2) Transmitter: In order to characterize the output power of the transmitter, the dc voltage of the on-chip power detector was measured over frequency, as illustrated in Fig. 26. Based on the simulated performance of that detector [see Fig. 11(b)], the signal power at the transmit amplifier output was estimated to be approximately 3.6–3.7 dBm across the entire TX VCO frequency range. Furthermore, the less than 20-mV mismatch between the measured and simulated detector output voltages indicate that the error in the estimated output power is expected to be less than 1 dB.

The output power control function was verified, as illustrated in Fig. 27, by varying the transmit amplifier output power control and monitoring the power of the receiver IF output and the dc output voltage of the on-chip power detector. Furthermore, an ELVA-1 D-band power sensor with a horn antenna was brought close to the chip and its power reading was monitored.[2] As seen in Fig. 27, the three power measurements track each other, indicating that the output power can be controlled over a range of at least 15 dB. Furthermore, this experiment also validates the linear operation of the receiver since the amplitude of the IF output signal due to transmitter leakage responds linearly to changes in the transmitter output power.

3) Antenna: The relative radiation pattern of the antenna was measured at the output of the receiver by placing the PCB with the packaged chip on a rotating table and illuminating it using a 122-GHz signal source. As illustrated in Fig. 28, two cases were compared, which were: 1) the board with the EM-coupled antenna alone and 2) the board with an EM-coupled antenna and a dielectric meniscus lens with $D = 35$ mm diameter and 20-mm focal length, which yields a maximum theoretical gain of

$$G = \frac{\pi D}{\lambda^2} = 33 \text{ dBi}. \tag{13}$$

[2]This measurement was performed in the near field as the power sensor does not have enough sensitivity to measure the power in the far field. Therefore, deembeding the free-space loss was not attempted.

Based on the measured patterns of Fig. 28, the antenna gain is improved by 20 dB by the lens. As a result, the estimated total antenna gain is 26 dBi.

4) Measurement of Rotation Speed: To verify the intended operation of the transceiver through the air, the speed of a rotating reflector placed at various distances was measured using the evaluation board with the packaged chip and the dielectric lens.

In this simple test case, a portion of the transmitted signal at frequency $f_{\rm TX}$ leaks into the receiver input and another portion is transmitted and reflected back by the reflector. The signal at the I IF output of the receiver can be expressed as

$$\begin{aligned}\text{IF}(t) = {} & A_{\rm leak} \cos\left(2\pi f_{\rm IF} t + \phi_{\rm leak}\right) \\ & + a_R(t) A_{\rm refl} \cos\left(2\pi f_{\rm IF} t + \phi_{\rm refl}\right)\end{aligned} \tag{14}$$

where $A_{\rm leak}$ and $A_{\rm refl}$ are the amplitudes of the signal leaking from the transmitter to the receiver and the reflected signals, respectively, $\phi_{\rm leak}$ and $\phi_{\rm refl}$ are the corresponding phases, while $f_{\rm IF} = f_{\rm TX} - f_{\rm RX}$ is the IF frequency. $a_R(t)$ is a function that depends on the reflector type, the antenna radiation pattern, and the rotation speed. In its simplest form, $a_R(t)$ is unity when the reflector is in parallel with the evaluation board and zero elsewhere. The amplitude of the reflected signal can be calculated by using (2) as

$$A_{\rm refl} = \sqrt{2 Z_0 P_{\rm RX}} = \frac{(2 Z_0 G_{\rm RX} P_{\rm TX} a_{\rm coupler} \sigma)^{1/2} G_{\rm ant} c}{(4\pi)^{3/2} f_0 d^2} \tag{15}$$

where $Z_0 = 50\ \Omega$ is the termination impedance at the IF output.

Similarly, the I reference output is

$$\text{REF}(t) = A_{\rm ref} \cos\left(2\pi f_{\rm IF} t + \phi_{\rm ref}\right). \tag{16}$$

By multiplying the reference and IF output signals and low-pass filtering, the baseband signal becomes

$$\begin{aligned}BB(t) = {} & A_{\rm leak} A_{\rm ref} \cos\left(\phi_{\rm ref} - \phi_{\rm leak}\right) \\ & + a_R(t) A_{\rm refl} A_{\rm ref} \cos\left(\phi_{\rm ref} - \phi_{\rm refl}\right).\end{aligned} \tag{17}$$

Equation (17) indicates that the baseband signal includes a dc component that depends on the leakage and a time-varying part that depends on the rotation speed of the reflector. Based on the simple model for $a_R(t)$, the strongest harmonic in the spectrum of the baseband signal $BB(t)$ will correspond to the rotation speed.

In practice, all four outputs of the chip could be further downconverted to a lower IF frequency of a few megahertz, digitized and processed by a digital signal processor. However, for a simple demonstration, the in-phase receiver IF output is amplified and multiplied with the in-phase reference output using an external passive mixer, as illustrated in Fig. 29. Fig. 30 reproduces the $BB(t)$ output in time and frequency domains for a 13×13 cm reflector, located 30 cm away from the PCB (including the dielectric lens). Fig. 31 shows $BB(t)$ when the reflector is positioned 2.1 m away from the PCB. The lower frequency tones in Fig. 31(a) correspond to movement spurs caused by the person who held the rotor in place. The difference in rotation speed between the two positions is also caused by this person's movement. In both experiments, the transmitter frequency was 122 GHz, while the receiver frequency was 120 GHz.

VI. Conclusion

A single-chip low-power low-voltage SiGe BiCMOS transceiver operating at 120 GHz has been presented. By careful selection of circuit topologies and by exploiting ac coupling techniques, the power supply voltage was kept below 1.8 V and the power consumption was reduced to 900 mW. By employing an on-chip antenna feed along with an external patch resonator, no off-chip transitions were necessary at 120 GHz. As a result, the chip was wirebonded in a low-cost open-lid QFN package, demonstrating the feasibility of future low-cost highly integrated D-band systems.

A breakdown of the 900-mW power consumption of the transceiver chip is presented in Table III. Most of the power was consumed for generating, distributing, and calibrating the LO signals, which was necessary in order to ensure proper operation of the transceiver. Table IV compares the performance of this transceiver with recently reported transmitters, receivers, and transceivers operating at D-band.

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