Second Generation Transceivers for D-Band Radar and Data Communication Applications

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***Abstract*— A single chip, dual-functionality radio and FMCW radar transceiver, operating at 140 GHz is described. Doppler, loop-back, and 4Gb/s NLOS radio link demos, over the air and at distances exceeding one meter, are demonstrated. The second part of the paper presents novel, sub-1.8 V circuit topologies intended for a low power, high resolution 120 GHz radar transceiver with self-calibration capabilities. The measured receiver noise figure, gain, and phase noise are 7.5 dB, 20 dB, and -100 dBc/Hz@1MHz offset, respectively.**

I. Introduction

Recent advanced SiGe HBT processes with f_{MAX} exceeding 400 GHz [1] provide adequate performance margin for the next generation of mm-wave systems in the $110-170$ GHz range (D-band). During the last two years, several groups have reported basic D-band circuit blocks such as VCOs, detectors [2], and LNAs [3], [4]. The first receivers [3], [5] and transceivers [6] fabricated in silicon, and operating above 100 GHz were also reported.

This paper presents a second generation of D-band transceivers which take advantage of the recent developments in process technologies, measurement and modeling techniques, to achieve enhanced functionality, such as gain and phase control, direct frequency and amplitude modulation, and at-speed self-test. New system architectures as well as low voltage, low power circuit topologies, enabling low-cost products in the frequency range under consideration, are presented.

II. 140 GHz Transceiver

The block diagram of the 140 GHz radio and radar transceiver [7], fabricated in a SiGe BiCMOS process with f_T/f_{MAX} of 230/280 GHz [8] is illustrated in Fig. 1. The most challenging function at this frequency is the LO signal generation and distribution. This block must lend itself to easy integration in a low noise PLL, operate with low power consumption, and minimize the number of harmonics and sub-harmonics produced on-chip. In lower frequency commercial transceivers, these goals are usually accomplished with a fundamental frequency VCO and a static divider chain. Since the latter cannot be reliably implemented at 140 GHz in current silicon technologies, the solution adopted here relies on a push-push VCO which simultaneously generates differential signals at $135.9-141.2$ GHz and quadrature signals at $68-70.6$ GHz, a pair of which drive the static divider

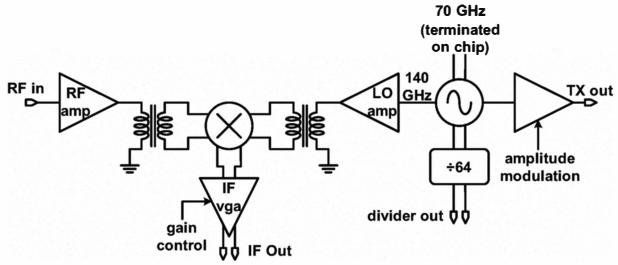

Fig. 1: 140 GHz transceiver architecture.

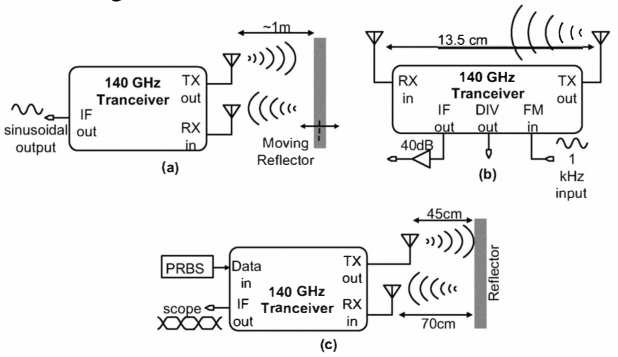

Fig. 2: Three different experiments conducted using the 140 GHz transceiver.

chain. The power dissipation is minimized by taking advantage of the differential LO outputs and by judiciously employing single-ended amplifiers and transformer-based single-ended to differential conversion to distribute the 140 GHz LO and RF signals to the double balanced Gilbert cell mixer.

Three different experiments [7], illustrated in Fig. 2, were conducted by connecting two horn antennas, with 24 dB gain each, at the transmitter output and receiver input, respectively. First, the Doppler effect was demonstrated (Fig. 2(a)) by slowly waving a reflector placed at a distance of approximately one meter from the TX and RX antennas, and recording the low frequency output of the receiver.

In a second experiment, direct frequency modulation, phase noise cancelation due to range correlation, and loop-back for at-speed self-test, without external mm-wave signals or equipment, were performed as shown in Fig. 2(b). These experiments were conducted by pointing the two antennas directly at each other, over a distance of 13.5 cm, and applying a 1 kHz sinusoidal signal at the control pads of the VCO. An amplified 8Vp-p 1 kHz signal was recovered at the IF output

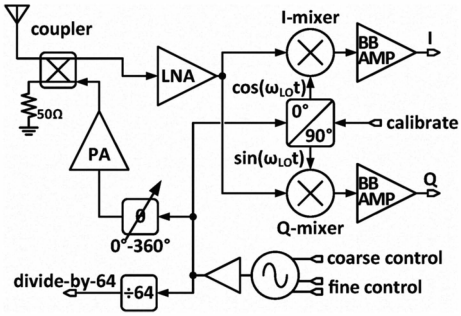

Fig. 3: Intended system architecture for the 122 GHz transceiver.

of the receiver whose phase noise was recorded at different offset frequencies, as low as 1 Hz.

Finally, as illustrated in Fig. 2(c), a non Line of Sight (NLOS) wireless data link experiment was set-up by pointing the input and output antennas at a fixed reflector. PRBS data sequences, provided by an external PRBS source, directly modulate the 140 GHz transmitter signal in amplitude, while the differential IF output of the receiver is monitored with an oscilloscope and a spectrum analyzer. In this manner, correct ASK operation at data rates up to 4Gb/s was verified over a distance of 1.1m.

III. $100 - 122$ GHz Transceiver Building Blocks

Fig. 3 represents a monostatic radar sensor for precision position and velocity detection at a range of a few meters, and which operates in the $122 - 123$ GHz band. A transmit power of less than 0 dBm is sufficient for this application. The main advantage of the monostatic architecture is that only one antenna is used for simultaneous transmission and reception. Furthermore, if a thick, mm-wave metal back-end is available, as in this SiGe BiCMOS technology [8], the 122 GHz antenna can be efficiently realized on-die, because of its small size and low back-end loss.

Compared to the transceiver architecture in Fig. 1, this system has increased functionality that allows on-chip loop-back, phase and amplitude correction, gain control, and IQ down-conversion.

The 6 dB coupler facilitates the single antenna operation and provides a loop-back path between the transmitter and the receiver which is required for on-die, at-speed, self-test. However, during normal operation, the finite isolation of the coupler (typically less than 20 dB) results in a portion of the transmitted signal leaking into the receiver, degrading its noise figure and setting stringent linearity requirements. The sketch of the 6 dB coupler is illustrated in Fig. 4 and comprises two side coupled transmission lines. A floating metal bar was introduced between the two lines in order to equalize the even and odd mode velocities and boost the coupler isolation, which is simulated to be better than 25 dB at 122 GHz.

Due to the low output power requirements of the transmitter, the same Variable Gain Amplifier, shown in Fig. 5, can be used as a low noise amplifier in the receiver and as a variable output power amplifier in the transmitter. The VGA features two common-emitter stages with inductive degeneration and a transformer-coupled, common-base output stage with gain control. The circuit consumes 21 mW from 1.2 V and 26.5 mW when the supply of the last stage is increased to 1.8 V, as needed when operated as a PA.

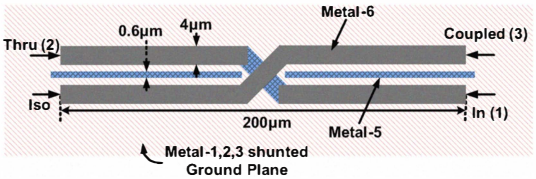

Fig. 4: Sketch of the 6 dB Coupler.

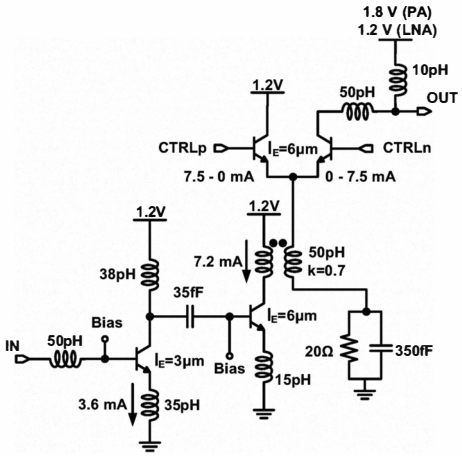

Fig. 5: Schematic of the 122 GHz VGA.

A transmit, 4-quadrant variable phase shifter, illustrated in Fig. 6, is required for at-speed self-test and to suppress the noise figure degradation due to transmitter leakage into the LNA. It consists of a lumped 90° hybrid and two variable gain amplifiers whose differential output currents are summed by transformer T1, which also performs single-ended to differential conversion. The circuit consumes 28 mW from 1.2 V.

The first stage in the divider chain can be realized with the Miller topology illustrated in Fig. 7 and utilizes a transformer to provide feedback from the output of the emitter followers to the input of the transconductors, thus facilitating low voltage

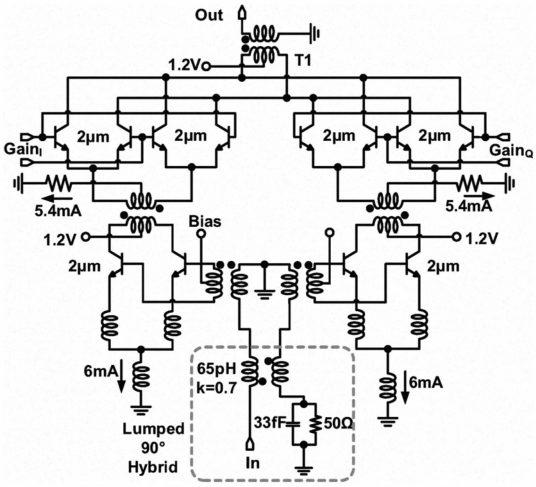

Fig. 6: Schematic of the 122 GHz phase shifter.

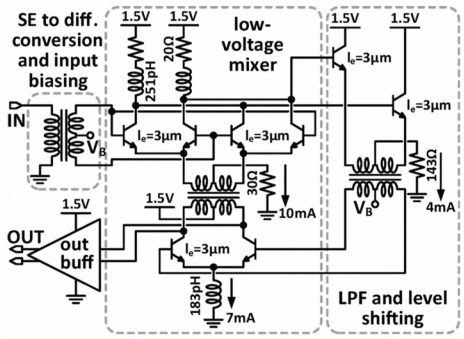

Fig. 7: Schematic of the Miller divider

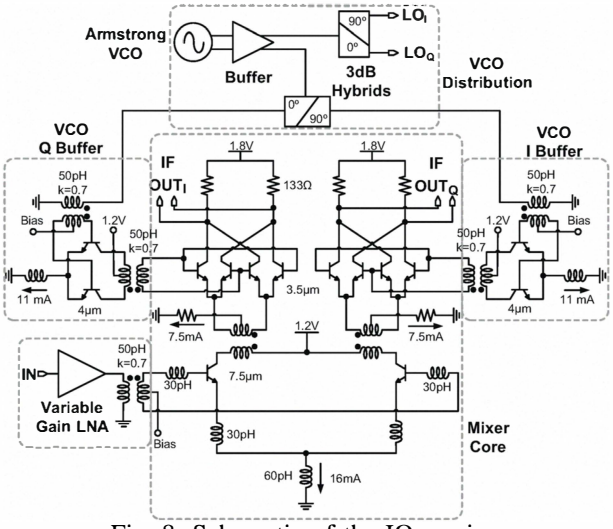

Fig. 8: Schematic of the IQ receiver.

operation from 1.5 V supply. The power consumption of 32 mW is significantly lower than that of previously reported bipolar dividers.

Finally, the schematic of the implemented receiver is shown in Fig. 8. Colpitts and Armstrong 1.8 V VCO topologies were designed and evaluated for 122 GHz operation. The Armstrong VCO, illustrated in Fig. 9, employs positive transformer feedback between the base and emitter of the HBTs and consumes 36 mW, compared to the 72 mW of the Colpitts VCO.

The receiver integrates the Armstrong VCO, a 7 mW and two 11 mW differential VCO buffers, two lumped 90° hybrids, the variable gain LNA, and a 45 mW double balanced IQ mixer whose schematic is shown in Fig. 8. The receiver occupies $1 \times 1.275\,\mathrm{mm}^2$ and consumes 220 mW, 58 mW of which are in the 50 Ω baseband buffers.

IV. Simulation and Experimental Validation

Accurate modeling of passive components is essential during the design of mm-wave circuits above 100 GHz, where any modeling inaccuracy can result in a shift of the operating frequency and reduction of the gain. To alleviate this problem, 2.5D electromagnetic simulations were employed to model all passive components.

Fig. 10 compares the measured and simulated S-parameters of the 6 dB coupler, showing good agreement up to 170 GHz with only 0.5 dB discrepancy in S_{21}. Similarly, Fig. 11 shows

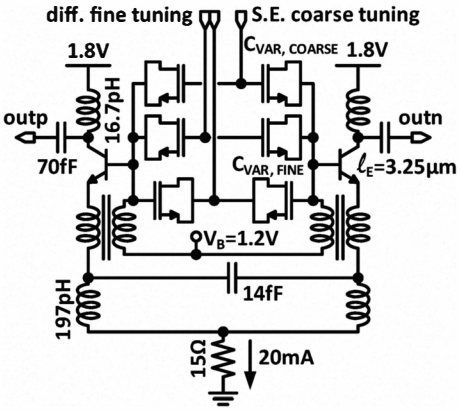

Fig. 9: Schematic of the Armstrong VCO.

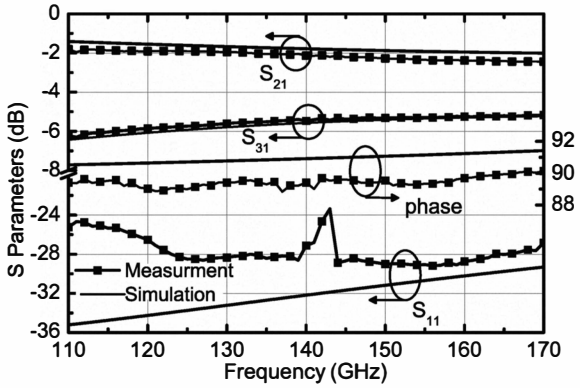

Fig. 10: Simulated versus measured S-parameters of the 6 dB coupler.

the measured and simulated S-parameters of the 90° hybrid used in the phase shifter and IQ receiver. The measured amplitude imbalance at 122 GHz is 0.15 dB while the phase error is 11°, a 7° difference from simulation.

The measured performance of the VGA is compared in Fig. 12 with simulations. The good agreement proves that both the transistors and the passive components are well modeled above 100 GHz.

Fig. 13 shows the measured tuning range, phase noise, and output power of the Colpitts VCO. It provides +5 to +6 dBm of output power over its entire 119.4−122.4 GHz tuning range, while the phase noise remains below -100dBc/Hz at 1MHz offset. Similarly, the Armstrong VCO has a tuning range of 107 − 111 GHz, 1 dBm output power, and phase noise better than and -95dBc/Hz measured at 1MHz offset. It continues to

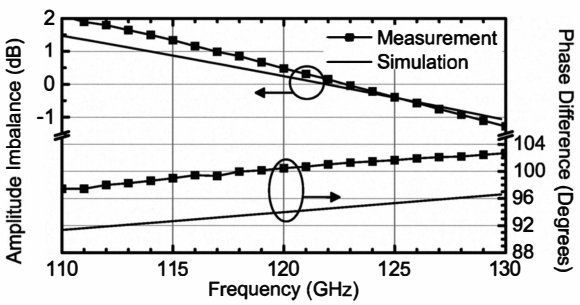

Fig. 11: Measured and simulated amplitude and phase imbalance of the 90° hybrid.

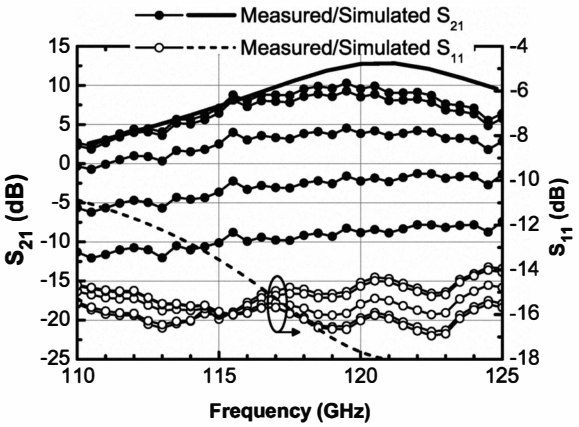

Fig. 12: S-parameter results for the 122 GHz VGA.

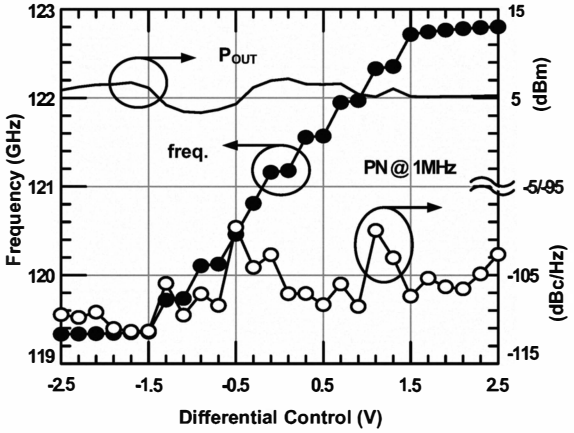

Fig. 13: Measured tuning curve, output power and phase noise of the Colpitts VCO.

oscillate even when the supply is reduced to 1 V.

The Miller divider operates from 112 GHz to 122 GHz with the upper frequency range being limited by the lack of a signal source with more than -15 dBm output power above 122 GHz. The measured phase response of the phase shifter is summarized in Fig. 14 for the different phase control settings, with a maximum phase error of 5° and amplitude of -14 ± 2 dB from 117 GHz to 122.5 GHz.

The IQ receiver shown in Fig. 8 was also characterized as a separate breakout. The measured receiver down-conversion gain (from the RF input to the I baseband output) has a peak value of 20 dB at 110 GHz, and a minimum DSB NF of 7.5 dB, as illustrated in Fig. 15. The receiver power

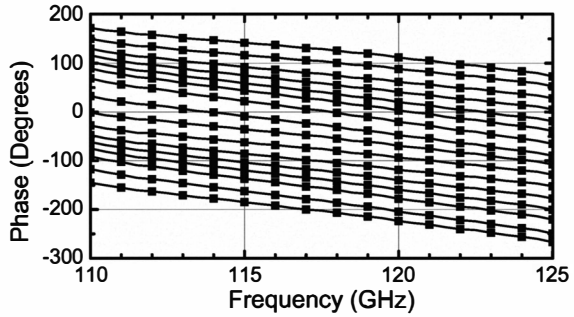

Fig. 14: Phase shifter response versus frequency.

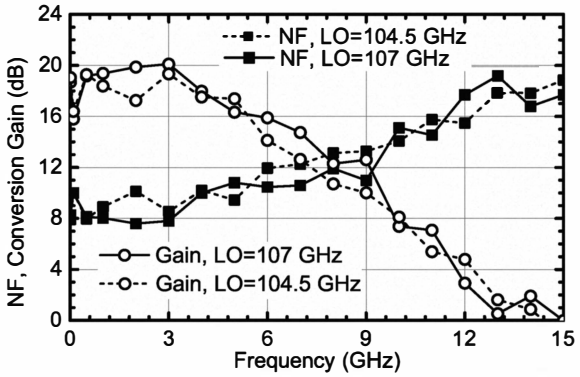

Fig. 15: Measured receiver down-conversion gain and DSB NF vs. IF frequency at $f_{LO} = 104.5$ GHz and 107 GHz.

TABLE I: Performance Summary

VCO frequency	135.9 – 142.2 GHz	107 – 111 GHz
VCO Phase Noise@ 1 MHz	-80 dBc/Hz	-95 dBc/Hz
RX Gain	32 dB	20 dB
RX Noise Figure	12.3 dB	7.5 dB
TX Output Power	-8 dBm	-
Data Rate	4 Gb/sec	-
DC Power	1.5 W	220 mW (RX)

consumption, noise figure, and VCO phase noise represent records for circuits operating above 100 GHz.

V. Conclusions

A 140 GHz transceiver capable of both ASK and FM modulation was presented, along with through-the-air data transmission, loop-back, and Doppler experiments. In an effort to decrease power consumption and increase functionality, a transceiver chip-set operating at 122 GHz based on novel, low-voltage topologies was developed and achieved record phase noise and NF while consuming only 220 mW. The performance of the two chips is summarized in Table I.

Acknowledgments

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References

[1] P. Chevalier *et al.*, "A conventional double-polysilicon FSA-SEG Si/SiGe:C HBT reaching 400 GHz $f_{\max}$," in *IEEE BCTM 2009.*, Oct. 2009, pp. 1–4.

[2] S. Sankaran *et al.*, "Towards terahertz operation of CMOS," in *IEEE ISSCC 2009*, Feb. 2009, pp. 202–203.

[3] S. T. Nicolson *et al.*, "A 1.2V, 140GHz receiver with on-die antenna in 65nm CMOS," in *IEEE RFIC 2008.*, Jun. 2008, pp. 229–232.

[4] M. Seo *et al.*, "A 1.1V 150GHz amplifier with 8dB gain and +6dBm saturated output power in standard digital 65nm CMOS using dummy-prefilled microstrip lines," in *IEEE ISSCC 2009.*, Feb. 2009, pp. 484–485.

[5] K. Schmalz *et al.*, "A 122 GHz receiver in SiGe technology," in *IEEE BCTM 2009.*, Oct. 2009, pp. 182–185.

[6] E. Laskin *et al.*, "165-GHz Transceiver in SiGe Technology," *IEEE JSSC*, vol. 43, no. 5, pp. 1087–1100, May 2008.

[7] ——, "A 140-GHz double-sideband transceiver with amplitude and frequency modulation operating over a few meters," in *IEEE BCTM 2009.*, Oct. 2009, pp. 178–181.

[8] G. Avenier *et al.*, "0.13 μm SiGe BiCMOS Technology Fully Dedicated to mm-wave Applications," *IEEE JSSC*, vol. 44, no. 9, pp. 2312–2321, Sep. 2009.