A 20 dBm Q-Band SiGe Class-E Power Amplifier With 31% Peak PAE

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***Abstract*—A Q-band two-stage Class-E power amplifier is designed and fabricated in a 0.13 μm SiGe HBT BiCMOS process. A mm-wave Class-E architecture considering the effect of various interconnect parasitics is adopted to achieve high power efficiency. Proper input and output networks have been designed to enable efficient switching of the HBT at large voltage swings without causing unwanted impact ionization-induced negative base current and instability. The measured performance of the fabricated chip show 20.2 dBm maximum output power, 31.5% peak power added efficiency, and 10.5 dB power gain across 4 GHz centered around 45 GHz for a supply voltage of 2.5 V. The total chip area including the pads is 0.74 mm $\times$ 1.7 mm.**

***Index Terms*—Power Amplifier (PA) , silicon germanium (SiGe) HBT, millimeter-wave, Q-band, Class-E .**

I. Introduction

In recent years, there has been a push towards implementation of mm-wave transceivers in silicon processes for a myriad of applications including high data rate wireless communications, radars, and imaging. Complex mm-wave silicon transceivers, including phased arrays, have been commercialized and are under consideration for high-performance defense applications where historically compound semiconductors have been used. Despite these advancements, efficient (PAE $>$ 20%) mm-wave Power Amplifiers (PA) with medium-to-higher output power level ($>$ 20 dBm) have not been demonstrated on silicon.

There is a fundamental trade-off between the breakdown voltage and the maximum frequency of operation of semiconductor devices [1]. For instance, the breakdown voltage of modern SiGe HBTs with f_{max} and f_T of above 200 GHz is limited to a few Volts, limiting the maximum output power that can be generated from a single device. Most published mm-wave silicon PAs operate in linear classes (A,B,AB) with a theoretical peak collector/drain efficiency of less than 100%. Moreover, the Power Added Efficiency (PAE) of amplifiers is degraded by their limited power gain at mm-waves.

Switching class amplifiers with a maximum theoretical efficiency of 100%, like Class-E, enable efficient power amplifiers. The major challenge in realization of switching power amplifiers at mm-waves is preserving the harmonic-rich non-overlapping voltage and current waveforms for efficient switching mode operation, as the higher harmonic frequencies get closer to the f_{max} and f_T of the device. In this paper, a systematic approach into designing switching amplifiers at mm-waves, incorporating the layout parasitics in the design cycle, is presented. Specifically, a two-stage Q-band power amplifier, is designed and implemented based on a mm-wave Class-E approach using SiGe HBTs. This power amplifier can serve as the core of a Digital Polar Transmitter (DPT) [2] to support complex modulations with high efficiency, linearity, and output power. The design methodology and implementation details are covered in Section II. The measurement results of the power amplifier are presented in Section III. Section IV concludes the paper.

II. Design and Implementation

In comparison with CMOS FET, SiGe HBTs generally offer a larger breakdown voltage for the same f_{max} and f_T. IBM8HP 0.13μm BiCMOS process with f_T = 200 GHz and f_{max} = 280 GHz [3] is used as the technology of choice for the reported power amplifier. The breakdown voltages for the high-f_T NPN SiGe HBTs are BVCEO = 1.7 V and BVCBO = 5.9 V. The BVCBO is the absolute voltage limit by which a device can be stressed before it suffers catastrophic breakdown. The collector breakdown voltage of HBT is a function of base impedance and collector current [5]. In a properly designed switching amplifier design, collector voltage and current waveforms do not overlap; therefore, with a proper base impedance, the collector voltage swing can be as much as 5.9 V, much higher than the nominal open base breakdown voltage of 1.7 V. In order to ensure reliable continuous operation, the maximum collector voltage is confined to less than 5.5 V in this design.

In this work, Class-E switching amplifier was adopted for a target output power of 20 dBm at 45 GHz. The conceptual block diagram of the mm-wave Class-E power amplifier is shown in Fig. 1. Design guidelines for Class-E operation with an ideal choke at the collector or a finite inductance L_1 have been reported [4].

Class-E operation at mm-waves imposes new challenges and design constraints. First, the combination of

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the input time constant due to finite base charge time of the HBT and the base-collector capacitance increases the rise and fall times of the collector voltage. As such, the collector voltage cannot reach its maximum theoretical value as predicted by ideal Class-E design equations. The second issue is that the capacitance budget for C_1, that ensures non-overlapping collector current and voltage Class-E waveforms, is almost entirely dictated by the transistor parasitics. The value of transistor parasitics vary widely with voltage swing and the device operation region. This is more pronounced in an HBT design (compared with FET) and makes the Class-E analysis and design more challenging. The third challenge, also unique to the bipolar transistor designs, stems from impact ionization and base current reversal under large collector voltage swings [5]. In the absence of closed-form analytical expressions capturing all the aforementioned complex dynamics, mm-wave design approach should rely on systematic simulations.

The performance of single-stage Class-E at 45 GHz is a function of device size, load value, and output power. Assuming a fixed supply voltage and lossless input and output passive networks, the output power and PAE of a Class-E design can be determined by a two-dimensional sweep of the device size and the load value. Fig. 2 shows a simulated plot of the maximum achievable PAE in a single-stage Class-E SiGe amplifier at 45 GHz and the corresponding device size versus the load value. At small load impedances, the ON resistance of the HBT degrades the collector efficiency more significantly. The ON resistance can be reduced by using large devices at the expense of increasing the collector capacitance. But, at 45 GHz, a larger collector capacitance exceeds the maximum allowable capacitance budget for proper Class-E operation (*i.e.*, non-overlapping collector current and voltage waveforms), and degrades the collector efficiency. At large load impedances, the collector efficiency can still improve by increasing the device size. But, the input power required to drive the larger transistor has to increase; hence, the PAE drops. On the other hand, device size cannot be too small; or, it will not handle the necessary collector current for the desired output power. From simulations, for output power above 20 dBm, a load impedance in the range of 20 Ω to 40 Ω gives the highest PAE. It should be noted that in an actual design, the layout parasitics influence the optimum points considerably. After conducing a systematic iterative process, a parallel combination of 4 HBTs, each with a 16μm emitter length, is chosen for the PA design. A Class-E driver stage is also designed using the same aforementioned procedure.

Stability analysis of power amplifiers forms a very important part of the design process. Large device sizes, common in power amplifiers, translate to larger

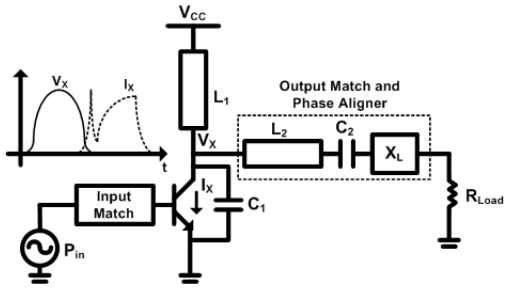

Fig. 1. Simplified schematic of a mm-wave Class-E power amplifier.

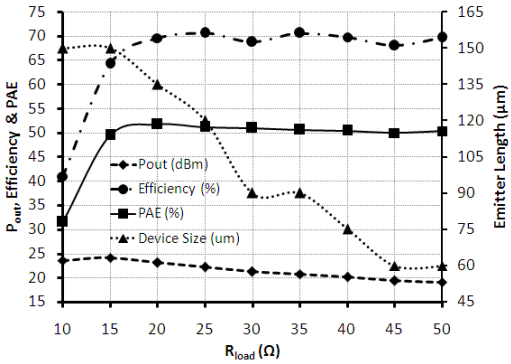

Fig. 2. Maximum achievable PAE in a single-stage Class-E at 45 GHz from simulation with lossless passives versus the load (and the corresponding device size).

collector-base capacitance and reduced reverse isolation, which oftentimes causes instability. Unlike small-signal systems, various forms of bifurcations and instability can occur in large-signal power amplifiers including sub-harmonic generation, spurious oscillations, etc. [6] This is especially true in HBT designs at mm-waves where a significant portion of the capacitances are device's voltage-dependent parasitics values. In our design, first, a small signal stability analysis is carried out using two-port S-parameter and Rollett's stability factor (K). Then, a large signal nonlinear stability analysis is conducted using periodic steady state simulations followed by large signal S-parameter of the two-port network. Through these simulations, sub-harmonic tones were detected in the designed circuit, most likely caused parametrically due to the device's large nonlinear capacitance. A half-harmonic trap is added to the base of each stage to prevent sub-harmonic generation. A parallel base resistance is used to mitigate the effect of base current reversal at large collector voltage swings. The complete schematic of the designed circuit is shown in Fig. 3.

The chip is fabricated in a technology with 7 metal layers (Fig. 4). The HBTs are laid out in a CBEBC (collector-base-emitter-base-collector) configuration for additional collector current handling reliability at the cost of increased device parasitics. Agilent ADS Momentum

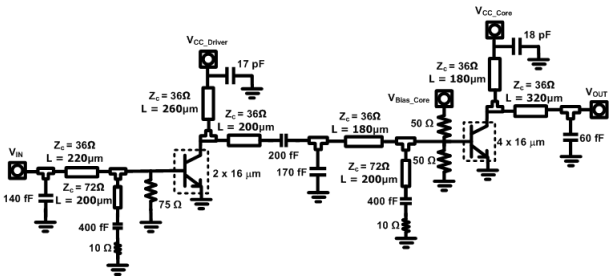

Fig. 3. Two-stage Q-band SiGe Class-E power amplifier schematic.

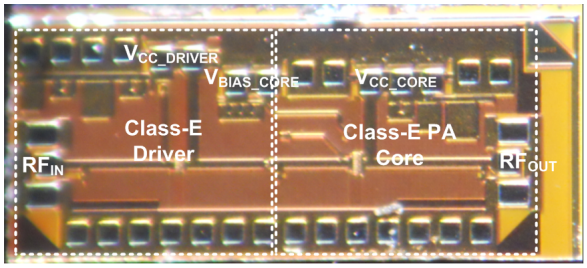

Fig. 4. The chip microphotograph.

is used to model the interconnects between the parallel HBTs into a multi-port lumped network. All passives are simulated in the IE3D electromagnetic simulator. The simulated and measured performance of a typical micro-strip, and an MIM capacitor are shown in Fig. 5 and Fig. 6, respectively. Multiple design iterations including the effect of layout parasitics are performed to ensure the desired performance.

III. Measurement Results

The fabricated chip is mounted on an FR4 PCB using a conductive epoxy. All DC connections are through wire-bonds. Input and output are probed using Cascade GSG probes. A directional coupler at the input of the amplifier is used to calculate the power supplied to

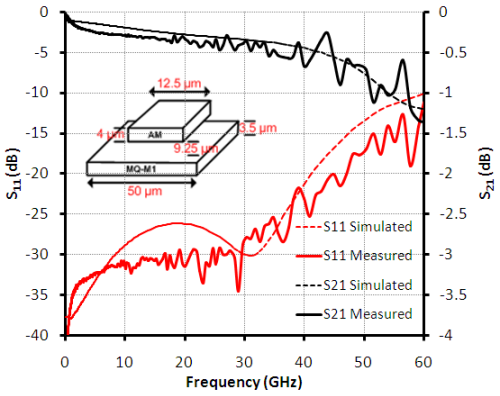

Fig. 5. S-parameters of a 50Ω 800μm long micro-strip line.

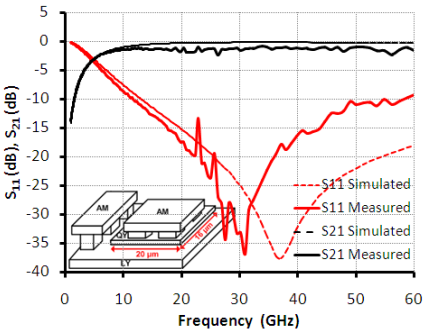

Fig. 6. S-parameters of a 325 fF (20μm $\times$ 16μm) MIM capacitor.

the amplifier. The output is connected to a spectrum analyzer to measure the generated output power, and also to ensure the absence of spurious/low frequency oscillations under large signal operation.

The chip is measured at two different supply voltages of V_{cc} = 1.8 V and 2.5 V, respectively. For V_{cc} = 1.8 V , the chip generates a maximum output power of 17.5 dBm with a peak PAE of 27.3% and 7.8 dB power gain at 45 GHz. The P_{-1dB} bandwidth is measured to be larger than 4 GHz spanning from 42 GHz to 46 GHz limited by the measurement setup at the higher end. To obtain higher output power and larger power gain, a supply voltage of V_{cc} = 2.5 V is used for the driver stage and V_{cc} = 2.5 V is used for the power amplifier core. Fig. 7 shows the measured output power and power gain versus the input power. The corresponding drain efficiency and PAE versus the output power are plotted in Fig. 8. A maximum output power of 20.2 dBm is generated at 45 GHz with 31.5% peak PAE and 10.5 dB power gain. The measured peak output power and PAE are slightly higher compared with simulations; this is likely due to conservative modeling of the interconnect parasitics and losses. The good match between the simulations and measurements validate the proper mm-wave based design approach. The power amplifier performance across 42 GHz to 46 GHz band is shown in Fig. 9 indicating a P_{-1dB} bandwidth of more than 4 GHz.Measurements done across 3 chips show consistent performance.

The measured chip does not show any spurious oscillations for the nominal DC bias points under condition of zero input power. However, for very low input power ranges of -10 dBm to -1 dBm, oscillatory behavior at 840 MHz due to the high Q bondwires was initially observed in the spectrum. This low frequency oscillation was completely removed on adding loss to the external bypass caps without affecting high frequency performance. For the measured results reported in this paper the chip is unconditionally stable and shows a clean spectrum. This bifurcation type oscillatory behavior with variation of input power is a known problem in power amplifiers

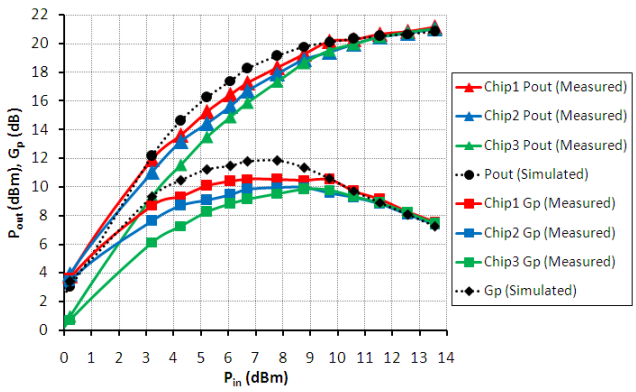

Fig. 7. Output power and power gain versus input power.

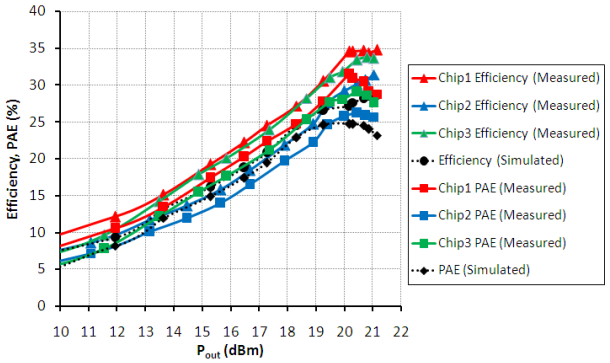

Fig. 8. Efficiency and PAE versus output power.

[6]. Analysis and design of power amplifier including this effect are parts of our ongoing and future work. The performance summary of the designed chip is shown in Table 1.

IV. Conclusion

A Q-band SiGe two-stage Class-E power amplifier with 20.2 dBm peak output power and 31.5% peak PAE is reported. The chip has been designed based on a systematic mm-wave based design approach to generate high power with high efficiency at mm-waves. A comparison with previously reported work (Fig. 10) shows that a 31.5% peak PAE is the highest recorded efficiency number for 20 dBm output power at mm-waves. Highly efficient switching power amplifier modules, like the current design, can be used in mm-wave digital polar transmitters for efficient generation of complex waveforms at watt-levels.

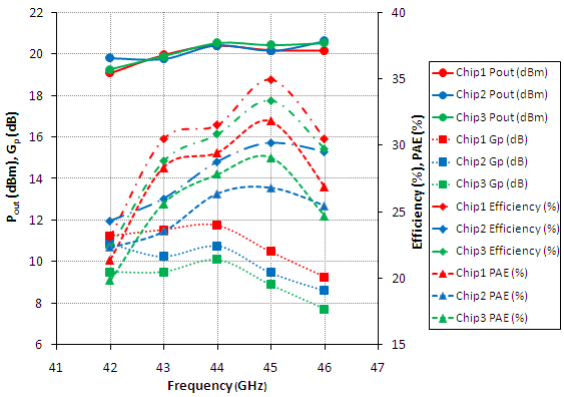

Fig. 9. Measured performance versus frequency.

TABLE I
Performance Summary of Q-band Class-E PA

Performance Metric	Chip 1	Chip 2	Chip 3
Frequency	45 GHz	45 GHz	45 GHz
$P_{out\_Peak\ PAE}$	20.2 dBm (104 mW)	20.5 dBm (110 mW)	20.5 dBm (110 mW)
G_p at $P_{out\_Peak\ PAE}$	10.5 dB	8.8 dB	8.9 dB
Drain Efficiency $_{Maximum}$	34.5%	30%	33%
PAE $_{Maximum}$	31.5%	26.2%	29%
$P_{-1\ dB\ Bandwidth}$	> 4 GHz	> 4 GHz	> 4 GHz
Chip Area	1.3 mm^2	1.3 mm^2	1.3 mm^2
Technology	130 nm BiCMOS	130 nm BiCMOS	130 nm BiCMOS

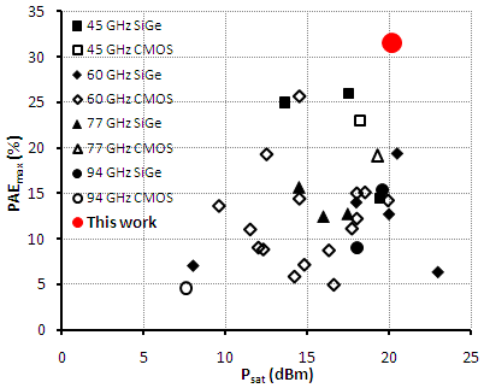

Fig. 10. PAE versus maximum output power of published mm-wave silicon power amplifiers.

Acknowledgment

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