

Release Notes

June 2009

GaN FET show different characteristics depending on the channel thickness, Al content in the channel, field plates, gate structure, passivation etc. This results in variety of IV and Gm shapes, pinch off voltages, SS and large signal characteristics. When technology is not settled, it is probably more efficient and faster to work with Table Based (typ. 1000 measurement points) or Empirical Table Based models (typ. 100 measurement points). When technology is settled, empirical models (typ. 100 measurement points) can be very useful, as they allow easy implementation of process variations, thermal conditions and to extend the model far beyond the measurement range in voltages and frequency. The ETB model can be used in the transactional period or in the case when very complicated characteristics should be modeled accurately, keeping the model structure simple and using table for the complicated characteristics.

Generally for GaN FET the transconductance per/mm is lower, Channel current is higher and ratio Gm/Ip_{pk} is lower in comparison with ordinary GaAs and InP HEMT.

When GaN technology is comparable mature & device reliable, the CW and pulsed characteristics are very similar, i.e. dispersive effects are rather small. Comparison with ordinary FET show that as characteristics are similar, the basic GaN FET model is similar to the available FET model and respective Verilog implementation. For some GaN FET with small dispersion & small difference between pulsed and CW characteristics, high P1 = (Gm/Ip_{pk}) > 0.5 ratio, the default model can be applied with a good accuracy. But as the GaN devices from different manufacturing processes differ and there are some specific issues for the GaN FET (device is pushed to the current & breakdown limits). Some of these issues are addressed in the GaN FET model design kit.

The main new different things in the GaN FET model in comparison with the default model in this Verilog implementation are:

1. Modified psi function(tanh(sinh(psi)) Ids model 3 .

This will produce shape closer to rectangular using one term of the power series P1. Very small addition of the P3-rd term can produce even sharper pinch-off and rectangular shape. In addition, by using double hyperbolic function the fit for the harmonics is better when ratio P1 = Gm/Ip_{pk} is low < 0.4, which is often the case for GaN FET, SiC FET and some other FET.

2. Capacitance model which can provide peaking of Cgs if device show this effect, Cap model 3, 4.

The capacitances are implemented as charge-Capmodel4 (to provide charge conservation) and as capacitance capacitance Cap model3 to keep the model compatible with simulators with capacitive.

In this implementation is considered that some of GaN devices show peak of Cgs at about -2 to 1 V. This is arranged with the peaking parameter part of P222, Cgs, **MJC** is the standard depletion coefficient, **m** will define how large can be the peak capacitance. The default P222=0 will switch-off the peaking part transferring to the standard capacitance model s 1,2 respectively.

$$y = (((V_{gsc} + 2.0)/P10) - 1.0); \text{ MJC} = 0.5;$$

$$C_{gsdepl} = \text{pow}((m + (y * y)), (-1 - \text{MJC})) * (m + (1 - 2 * \text{MJC}) * (y * y));$$

The shape of the caps& position of the peak can be changed if required. If device is very different, for example the peak of the cap is at -10v, this can be arranged modifying part $((V_{gsc}+2.0)/P10)$ to $((V_{gsc}+10.0)/P10)$.

3. Temperature and bias dependent R_d , R_s . – this is very important when the device is pushed hard.

Typical $T_{crs}=0.003$ which is used for both R_s and R_d . This will effect also the knee walkout and change the junction temperature in time.

Bias dependence of R_d is assumed similar to the current dependence.

$$R_{d1} = R_d + R_{d2} * (\tanh_psi);$$

R_d is the bias independent R_d and R_{d2} is the user defined value, default 0.

4. Enhanced dispersion modeling, back gate approach V_{bg} , delay circuit to model the knee walkout.

$$V_{pkm} = V_{pks} - D_{vpks} + D_{vpks} * \tanh(\text{Alphas} * V_{ds}) - V_{bg} - V_{sb2} * (V_{dg} - V_{tr}) * (V_{dg} - V_{tr});$$

Delay circuit represent s the slowed down reaction of I_{ds} on the gate control voltage at RF. It is arranged as $R_{del} * C_{del}$. Typical values are $C_{del}=1-2$ fF (the gate footprint of the gate capacitance) and $R_{del}=1-5$ kohm- the channel charging resistance. At high frequency C_{del} shunts directly the control V_{gs} input.

5. The channel breakdown was implemented in the default model with parameters - $L_{sb0_T} * \text{limexp}(V_{dg} - V_{tr})$. New is the exponents parameter can be adjusted with parameter E_{bd} .

$$L_{sb0_T} * \text{limexp}(E_{bd} * (V_{dg} - V_{tr}))$$

6. In the GaN model, as devices are pushed to the limits, the GS and GD junction breakdown is also included.

This is arranged with breakdown voltages for the respective junctions V_{bdgs} (typ. 10), V_{bdgd} (typ. 100), the exponent slope P_{bdg} (typ 0.5), and breakdown coefficient K_{bdgate} . Setting $K_{bdgate}=0$ will switch-off the junction breakdown (default=0)

$$I_{gs1} = \exp(P_g * \tanh((_v3 - V_{jg}))) - \exp(-P_g * \tanh(V_{jg}))$$

$$I_{gs} = I_j * (I_{gs1} - K_{bdgate} * 0.001 * I_{gs2}) + 0.000000000000001$$

$$I_{gd1} = (\exp((P_g) * \tanh((_v2 - V_{jg}))) - \exp(-P_g * \tanh(V_{jg})))$$

$$I_{gd} = I_j * (I_{gd1} - K_{bdgate} * 0.001 * I_{gd2}) + 0.000000000000001$$

7. Many functional changes made by Tiburon to improve the stability.

The important feature of Verilog A implementation is that parameters equations which are of user's interest can be arranged to be see what the CASD tool is calculating. This is arranged using the command Desc in some lines. (* desc="Cgssim" *) for example. What is calculated can be viewed selecting "Detailed" in the simulation box ,keeping in mind that this will slow down the simulations if too many parameters are displayed.

When device has some specifics features the model equations can be changed using the Verilog model as mainframe . For example, highly asymmetrical G_m shape or G_m Asymmetrical with 2 peaks of the transconductance can be easily implemented in Verilog or SDD. But this will require adding 2 more parameters: V_{pks2} of the second peak and the splitting current parameter AA.

$$I_{ds} = I_{pk0T} * (1 + AA * \tanp + (1 - AA) * \tanp11) * \tanh(\text{alphap} * V_{ds}) * (1 + \text{lambdap} * V_{ds} + L_{sb0} * \exp(E_{bd} * (V_{ds} - V_{tr})))$$

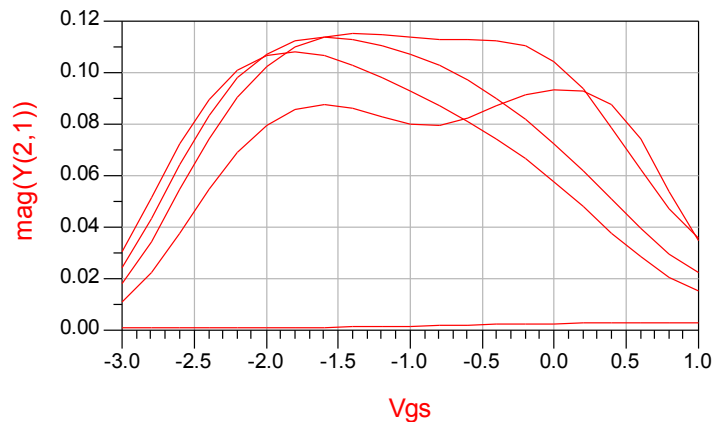
$$V_{pkm} = V_{pks} - DV_{pks} + DV_{pks} \cdot \tanh(\text{Alphas} \cdot V_{ds}) - V_{bg} - V_{sb2} \cdot (V_{dg} - V_{tr})^2$$

$$V_{pkm2} = \text{Vpks2} - DV_{pks} + DV_{pks} \cdot \tanh(\text{Alphas} \cdot V_{ds}) - V_{bg} - V_{sb2} \cdot (V_{dg} - V_{tr})^2$$

$$x_{11} = P1T \cdot ((V_{gs} - V_{pkm2}) + P2 \cdot (V_{gs} - V_{pkm2})^2 + P3 \cdot (V_{gs} - V_{pkm2})^3)$$

$$\tanh_{11} = \tanh(x_{11})$$

In a similar way other changes can be arranged, but it should be considered what is more efficient to do: table based model or to increase complexity of the empirical model.



$$V_{pks} = -0.3\text{V}; V_{pks2} = -2\text{V}, AA = 0.1;$$