MOS Capacitors

ECE 2204
Some Classes of Field Effect Transistors

- **Metal-Oxide-Semiconductor Field Effect Transistor**
  - MOSFET, which will be the type that we will study in this course.
- **Metal-Semiconductor Field Effect Transistor**
  - MESFET, typically fabricated with III-V semiconductors
- **Junction Field Effect Transistor**
  - JFET, resilient to electrostatic discharge (ESD)
- **High Electron Mobility Transistor or Modulation Doped Field Effect Transistor**
  - HEMT or MODFET, typically fabricated with III-V semiconductors
- **Fast Reverse/Fast Recovery Epitaxial Diode**
  - FREDFET
- **DNA Field Effect Transistor**
  - The conduction path is through a strand of DNA
Field Effect Transistors

- A voltage is applied to the gate of the transistor, which produces an electric field within the semiconductor.
  - Typically, the gate current is zero.
- The conductivity (or resistivity) of the path between two contacts, the source and the drain, is altered by the voltage applied to the gate.
  - Device is also known as a voltage controlled resistor.
MOS Capacitor

- The operation of a metal-oxide-semiconductor is used to explain the operation of the MOSFET.
  - In a MOSFET, the channel in the semiconductor, the oxide, and the gate metalisation forms a MOS capacitor.
    - The structure looks like a parallel plate capacitor where one of the plates is the semiconductor and the other is the gate metalisation. The insulator between the parallel plates is the oxide.
MOS Capacitor

\[ C_{OX} = \frac{\varepsilon_{OX} A}{t_{ox}} = \frac{\varepsilon_{ox} \varepsilon_o A}{t_{ox}} \]

\( \varepsilon_{OX} = \varepsilon_{ox} \varepsilon_o \) where \( \varepsilon_{ox} \) is the relative dielectric constant of the oxide and \( \varepsilon_o \) is the vacuum permittivity.
Operation of a MOS Capacitor

• In the following analysis, it is assumed that the channel in the semiconductor is lightly doped with acceptors (i.e., p type).
  ▫ There are three regions of operation
    • Accumulation (in this case, $V_G < 0 \text{ V}$)
    • Depletion (in this case, $0 \text{ V} \leq V_G \leq V_{TN}$)
    • Inversion (in this case, $V_G \geq V_{TN}$)
Accumulation ($V_G < 0$ V)

- An electric field $E$ is induced by the applied voltage $V_G$.
  - More holes are at the oxide-semiconductor interface than expected from the concentration of acceptors.
    - Holes are attracted to interface by the negative gate voltage.
    - Electrons are repelled towards the body contact.

$$E = -\frac{V_G}{t_{ox}}$$
Depletion (0 V < $V_G \leq V_{TN}$)

- The induced electric field $E$ causes the concentration of holes at the oxide-semiconductor interface to be smaller than the acceptor concentration and the electron concentration to be greater than expected.
Depletion Mode Capacitance

- The unscreened acceptors and a higher than expected electron concentration at the oxide semiconductor interface induce an electric field in the semiconductor, producing a depletion region to form.

\[ C_{MOS} = \frac{C_{OX}C_S}{C_{OX} + C_S} \]

\[ C_S = \frac{\varepsilon_S A}{W} \]
Inversion ($V_G \geq V_{TN}$)

- The gate voltage is large enough that the concentration of electrons at the oxide-semiconductor interface is greater than the concentration of holes.
  - The type of the semiconductor has effectively been converted from p-type to n-type. The voltage when $n = p$ at the oxide-semiconductor interface is called the threshold voltage, $V_{TN}$. 
Inversion Mode Capacitance

- A depletion region still exists in the semiconductor, but is now located between the inverted (n-type) region and the remaining p-type semiconductor.
  - The thickness of the depletion region \( W \) is constant, even if \( V_G \) increases so the magnitude of the MOS capacitance is constant.

\[
C_{MOS} = \frac{C_O X C_S}{C_O X + C_S}
\]

\[
C_S = \frac{\varepsilon_S A}{W}
\]
MOS Capacitance

- Is largest in the accumulation mode when $V_G \leq 0$ V
- Is smallest in the inversion mode when $V_G \geq V_{TN}$
- Varies with $V_G$ in the depletion mode