Logic Gate Specifications

Definitions
Currents and Voltages

- **All currents** are defined as positive when they flow into the terminal of a logical gate. This includes the output terminals.
- **All voltages** are measured with respect to ground, unless otherwise specified.
- The **first subscript** on a voltage or current indicates the terminal where the parameter was measured. $I_I$ is the current entering the input terminal. $V_O$ is the voltage at the output terminal.
Output Voltages

• $V_{OH\text{min}}$
  – CMOS: the largest output voltage when the absolute value of the slope of the voltage transfer characteristic is 1
  – TTL: the minimum allowable voltage on the output pin when the value of the logical operation is a “1” and the output stage transistor is still in cut-off.

• $V_{OL\text{max}}$
  – CMOS: the smallest output voltage when the absolute value of the slope of the voltage transfer characteristic is 1
  – TTL: the maximum allowable voltage on the output pin when the value of the logical operation is a “0” and the output stage transistor is still in saturation.
Input Voltages

- $V_{IHmin}$
  - CMOS: the smaller of the two input voltages when the absolute value of the slope of the voltage transfer characteristic is 1
  - TTL: the minimum voltage on the input pin that causes the output transistor to be in the same piecewise model as it is when 5V is applied to the input terminal.

- $V_{ILmax}$
  - CMOS: the larger of the two input voltages found when the absolute value of the slope of the voltage transfer characteristic is 1
  - TTL: the maximum voltage on an input pin that causes the output transistor to be in the same piecewise model as it is when 0V is applied to the input terminal.
Output Currents

- $I_{OH\text{max}}$ – the maximum current that flow into the output terminal when the output of the logical circuit is a “1”.
- $I_{OH\text{min}}$ – the minimum current that flow into the output terminal when the output of the logical circuit is a “1”.
- $I_{OL\text{max}}$ – the maximum current that flow into the output terminal when the output of the logical circuit is a “0”.
- $I_{OL\text{min}}$ – the minimum current that flow into the output terminal when the output of the logical circuit is a “0”.
Input Currents

• $I_{IH_{\text{max}}}$
  – the maximum current that flow into the input terminal when the input of the logical circuit is a “1”.

• $I_{IH_{\text{min}}}$
  – the minimum current that flow into the input terminal when the input of the logical circuit is a “1”.

• $I_{IL_{\text{max}}}$
  – the maximum current that flow into the input terminal when the input of the logical circuit is a “0”.

• $I_{IL_{\text{min}}}$
  – the minimum current that flow into the input terminal when the input of the logical circuit is a “0”.

Max and Min Currents

- If one of the currents at, for example, the output terminal is positive and the other is negative, then the positive current is $I_{O_{\text{max}}}$ and the negative current is $I_{O_{\text{min}}}$.

- However, if one of the currents is 0A and the other is negative, then the negative current is assigned to be $I_{O_{\text{max}}}$ and 0A is assigned to be $I_{O_{\text{min}}}$. 
Power Supplies

- $V_{CC}$
  - Voltage of the positive power supply for the digital electronic circuit/the logic gate, usually used when some of the components in the circuit are bipolar junction transistors (BJTs)

- $V_{DD}$
  - Voltage of the positive power supply for the digital electronic circuit/the logic gate, usually used when some of the components in the circuit are field effect transistors (FETs)

- $-V_{CC}$
  - Voltage of the negative power supply for the digital electronic circuit/the logic gate, used when some of the components are BJTs. This is not commonly noted as the negative power supply voltage is typically ground.

- $-V_{DD}$
  - Voltage of the negative power supply for the digital electronic circuit/the logic gate, used when some of the components are FETs. This is not commonly noted as the negative power supply voltage is typically ground
Undefined

• X – an undefined logic level that is associated with a voltage between $V_{IL\text{max}}$ and $V_{IH\text{min}}$. 
Fanout

- **N – Fanout**
  - Fanout is the maximum number of logic gates (exactly the same at the first one) that can be attached in parallel to the output of the logic gate.

\[
N = \text{Floor} \left( \frac{|I_{OLmin}|}{I_{ILmax}} \right)
\]
Noise Margin

• **DNM**  \( DN_{\text{M}} = V_{\text{OH}_{\text{min}}} - V_{\text{IL}_{\text{max}}} \)
  - Dynamic noise margin. This is the amount of noise at the output terminal of a gate that will cause the signal at the input of a cascaded gate to be recognized as the opposite logic level.

• **NML**  \( N_{\text{M}} = V_{\text{IL}_{\text{max}}} - V_{\text{OH}_{\text{min}}} \)
  - Noise margin low. The maximum amount of noise allowed at the output terminal of a logic gate that, added to \( V_{\text{OL}_{\text{max}}} \), will always be recognized as a low at the input of a cascaded gate.

• **NMH**  \( N_{\text{MH}} = V_{\text{OH}_{\text{min}}} - V_{\text{IH}_{\text{max}}} \)
  - Noise margin high. The maximum amount of noise allowed at the output terminal of a gate that, subtracted from \( V_{\text{OH}_{\text{min}}} \), will always be recognized as a high at the input of a cascaded gate.
Propagation Delay Time

• $t_{pd}$ is the time required for a change of voltage at the input terminals of a logic gate to cause a change in the voltage at the output of the gate.
  – Note that the rise time, $t_r$, and the fall time, $t_f$, do not have to be the same.
  – Also, the propagation delay time may not be the same length of time when the transition is from $0 \rightarrow 1$ as it is from $1 \rightarrow 0$.

• Electrons and holes do not move instantaneously, they have mobility, and there are capacitors and inductors in the circuit that must charge and discharge.