Digital to Analogue Conversion

Chapter 13
Why is conversion needed?

- Most signals in the world are analogue.
- Microprocessors and most computers use digital signals.
  - Analogue to Digital Converters (ADCs) change analogue signals to digital signals that are then used by the microprocessor.
  
  - Digital to Analogue Converters (DACs) may be used to change digital signals to analogue signals that are then used by the peripherals attached to the microprocessor.
ADCs and DACs

• ADCs tend to be more common on a microprocessor.
  ▫ The number of peripherals that have ADCs and DACs integrated inside is increasing so the microprocessor may not need this capability in the future.
  • Why? Because more peripherals are manufactured with integrated ADCs. However, you then need to decide type of format that the digitized data will be transferred to your microprocessor
    • Examples: I²C, CAN, SPI, ethernet, USB
Note: Analogue (UK) and Analog (US) are two different spellings for the same word.
Digital to Analogue Conversion (DAC)

Block Diagram

- D is the digital input.
- Vo is the Analog output.
- \( V_r \) is a precise, stable, known voltage reference.
- There are some control lines that are used to determine how often the DAC should convert the input signal, for example.
A relatively straightforward DAC can be realised using a resistor network, a common type is the **R-2R ladder**

**Good test of your knowledge of Thévenin’s theorem, can you show that:**

\[
V_{out} = \frac{V_r}{2^n} (D_{n-1}2^{n-1} + D_{n-2}2^{n-2} + \ldots + D_02^0)
\]
A simple relationship usually relates the digital input to the analog output, such as

$$V_o = \frac{D}{2^n} V_r$$

- $V_o$ is the analog output voltage
- $D$ is the value of the binary input word
- $n$ is the number of bits in the input word
- $V_r$ is the value of the voltage reference

![Diagram of output voltage (V_o) vs. D (input binary number)]

- $V_r/2^n$
- $(2^n-2)V_r/2^n$
- $(2^n-1)V_r/2^n$
- $2V_r/2^n$
- $V_r/2^n$

D (input binary number): 000, 001, 010, $2^{n-2}$, $2^{n-1}$, $2^n$
Analog Output

- There are a finite set of voltages that are generated by the DAC.
  - For each digital input value, there is a corresponding analogue output voltage.
  - Number of possible output voltages is $2^n$ (number of bits in the word)
- The **range** of the DAC is the difference between the maximum and minimum output values.
- The **resolution** of the DAC is the step size between each analog value.
  \[
  V_r = \frac{V}{2^n}
  \]
- **Conversion speed** is the inverse of the time that it takes the DAC to act on changes to the input.
Maximum possible output value occurs when $D = (2^n-1)$.

The value of $V_r$ as an output is never reached. (Review the R-2R figure to determine why.)

3 bit DAC where $V_r = 3$V

<table>
<thead>
<tr>
<th>D</th>
<th>Vo</th>
<th></th>
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</thead>
<tbody>
<tr>
<td>000</td>
<td>0 V</td>
<td>(0 V)</td>
</tr>
<tr>
<td>001</td>
<td>3/8 V</td>
<td>(0.375 V)</td>
</tr>
<tr>
<td>010</td>
<td>6/8 V</td>
<td>(0.75 V)</td>
</tr>
<tr>
<td>011</td>
<td>9/8 V</td>
<td>(1.125 V)</td>
</tr>
<tr>
<td>100</td>
<td>12/8 V</td>
<td>(1.5 V)</td>
</tr>
<tr>
<td>101</td>
<td>15/8 V</td>
<td>(1.875 V)</td>
</tr>
<tr>
<td>110</td>
<td>18/8 V</td>
<td>(2.25 V)</td>
</tr>
<tr>
<td>111</td>
<td>21/8 V</td>
<td>(2.625 V)</td>
</tr>
</tbody>
</table>
3 bit DAC in previous example

- Maximum number of analog output voltages?
- Range of the DAC?
- Resolution of DAC?
### Key Features of the NXP LPC 1768

<table>
<thead>
<tr>
<th>LPC1768 features</th>
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</thead>
<tbody>
<tr>
<td><strong>ARM Cortex-M3 core</strong></td>
<td>• 100 MHz operation&lt;br&gt;• Nested Vectored Interrupt Controller for fast deterministic interrupts&lt;br&gt;• Wakeup Interrupt Controller allows automatic wake from any priority interrupt&lt;br&gt;• Memory Protection Unit&lt;br&gt;• Four reduced-power modes: sleep, deep sleep, power-down and deep power-down</td>
</tr>
<tr>
<td><strong>Memories</strong></td>
<td>• 512 KB of Flash memory&lt;br&gt;• 64 KB of SRAM</td>
</tr>
<tr>
<td><strong>Serial peripherals</strong></td>
<td>• 10/100 Ethernet MAC&lt;br&gt;• USB 2.0 full-speed device/Host/OTG controller with on-chip PHY&lt;br&gt;• Four UARTs with fractional baud rate generation, RS-48, modem control, and IrDA&lt;br&gt;• Two CAN 2.0B controllers&lt;br&gt;• Three SSP/SPI controllers&lt;br&gt;• Three I²C-bus interfaces with one supporting Fast Mode Plus (1-Mbit/s data rates)&lt;br&gt;• I²S interface for digital audio</td>
</tr>
<tr>
<td><strong>Analog peripherals</strong></td>
<td>• 12-bit ADC with eight channels&lt;br&gt;• 10-bit DAC</td>
</tr>
<tr>
<td><strong>Other peripherals</strong></td>
<td>• Ultra-low-power (&lt; 1 uA) RTC&lt;br&gt;• General-purpose DMA controller with eight channels&lt;br&gt;• Up to 70 GPIO&lt;br&gt;• Motor control PWM and Quadrature Encoder Interface to support three-phase motors&lt;br&gt;• Four 32-bit general-purpose timers/counters</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>• 100-pin LQFP (14 x 14 x 1.4 mm)</td>
</tr>
</tbody>
</table>
The LPC1768 has a 10 bit DAC, and uses its regulated 3.3 V power supply as the voltage reference.

- What are the number of steps, range, the resolution, the range, and the conversion speed of the LPC1768 DAC?
  - It takes 5 μs per conversion.
  - How many clock cycles does this conversion take?
The mbed’s LPC1768 chip has a 10-bit DAC (i.e. \( n=10 \)).

The mbed uses its own 3.3 V power supply as voltage reference.

- There will therefore be \( 2^n \) steps in the mbed DAC output characteristic, i.e. 1024.
- The step size, or resolution, is therefore be \( 3.3/1024 \), i.e. 3.2 mV per bit.
- The conversion speed is 200,000/s. The clock speed is 100 MHz so the conversion time is equivalent to 500 clock cycles.
- There is another specification called the sampling frequency. The maximum sampling frequency provides a limit to the speed at which the digital signal can be sent to the DAC.
It is relatively easily check the resolution of the DAC.

For example, create an extremely slow sawtooth. In this case, it takes 10,000 steps to reach the max value with a 1 second interval between each step. The period of the waveform is about 2 hours 45 minutes, but this is not the point.

```c
/* Program to check DAC resolution of mbed*/
#include "mbed.h"
AnalogOut Aout(p18);
DigitalOut led1(LED1);
float i;
int main(){
    while (1){
        for (i=0;i<1;i=i+0.0001){
            Aout=i;
            wait(1);
            led1=!led1;
        } }
}
```

Note: By the end of this course, you should be able to go through a simple program and describe what each line of code means and what the mbed will do as a result. You should also be able to write a simple program for the mbed.
Measurement

• Connect the AnalogOut pin to a voltmeter or an oscilloscope.
• LED flashes each time that a new analog value is outputted by the DAC.
• However, 10,000 is larger than the maximum number of steps for the mbed DAC.
• So, the DAC output voltage only changes on approximately every 5\textsuperscript{th} step and when it does, the output voltage changes by about 3 mV.
  • The float value is rounded to the nearest digital input to the DAC.
Ideal DAC

From Understanding Data Converters, Texas Instruments Application Note
Offset Error

From Understanding Data Converters, Texas Instruments Application Note
Gain Error

(a) ADC

(b) DAC

Gain Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 111), After Correction of the Offset Error

From Understanding Data Converters, Texas Instruments Application Note
Total Error

- Gain Error
- Offset Error
- Nonlinearity Error

Absolute Accuracy or Total Error of a Linear ADC or DAC

From Understanding Data Converters, Texas Instruments Application Note