Advanced techniques for
Cadence OrCAD PCB Designer
Version 16.2

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This document explains some more advanced techniques for the layout of PCBs that go beyond the basic methods taught in Electronic Design Project 2.

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1 Where to learn more

Extensive documentation is provided with OrCAD, divided into over 100 documents. They are supplied online and as pdf files, which you may find easier to read. Unfortunately their names are cryptic and the interdocument links have been set up in a way that works only on unix. Here is a guide to the most helpful documents with their filenames (all have the extension .pdf, which I have omitted). The documentation is not entirely consistent with OrCAD PCB Editor, nor has it been updated throughout for version 16.2.

• The OrCAD Flow Tutorial (flowtut) takes you through the complete process of capture, simulation and PCB design and covers several techniques that I have not described in these notes.

• OrCAD Capture User’s Guide (cap_ug) has a particularly relevant chapter on Using Capture with PCB Editor, which includes issues such as assigning the No Connect property.
Figure 1. Toolbars in Allegro, taken from the Allegro PCB and Package Physical Layout Command Reference. It has not been updated for version 16.2. Not all of the buttons are available in OrCAD PCB Editor.

- The Allegro PCB Editor User Guide (algromast) is the most helpful set of documents but is so long that it is split into thirteen parts, of which these are most relevant:

  1. Getting Started with Physical Design (algrostart). This is the most useful document for learning how to use Allegro.
  2. Defining and Developing Libraries (algrolibdev). Mostly devices, symbols and padstacks but also technology and parameter files.
  3. Transferring Logic Design Data (algrologic). Despite the name, this means importing from Capture or a similar application and includes analogue components.
  4. Preparing the Layout (algrolay). This includes the cross-section of the board, keepins and keepouts, padstacks and etch shapes – fills or pours.
  6. Placing the Elements (algroplace). Most of this is rather advanced too.
Routing the Design (algroroute). This describes different strategies for routing, both manual and automatic, and covers fanouts, which I have not mentioned.

Completing the Design (algrodescmp). Another one that I have barely opened.

Preparing Manufacturing Data (algroman). Covers the final steps needed to send a board for commercial manufacture – silkscreens, artwork (Gerbers) and drill files.

You might also need the Allegro Constraint Manager User Guide (cmug). The Allegro PCB Editor Tutorial (algrotutorial) concentrates on the user interface.

- Routing from PCB Editor, both manual and automatic, is explained in the Autorouting with Allegro PCB Editor Tutorial (aleg_spec_tut). The Allegro PCB Router Tutorial (sptut) explains routing within SPECCTRA itself, for which the complete reference is Allegro PCB Router User Guide (spug).

- If you know precisely which PCB Editor command is involved, the files A Commands (acoms) to Z Commands (zcoms) contain comprehensive explanations of each command, often with helpful examples. The names of the commands are not always obvious, in which case the Allegro PCB and Package Physical Layout Command Reference (cmdref-mast) is the place to start. The new board wizard is under L (layout wizard), for instance. Figure 1 on the preceding page for the toolbars is taken from this manual. (It does not appear to have been updated for version 16.2.)

- The limits of the demo versions are in OrCAD Demo Products Reference (demoswitch).

Search the Cadence PCB Forum at www.cadence.com/community/forums/27.aspx if these references fail. The experts may have solved your problem already.

### 2 Capture techniques

#### 2.1 Entering repeated data into Properties

Here is a faster way of entering footprints into Capture if you have numerous components with the same footprint.

1. Select all the identical components and open the Properties spreadsheet.
2. Click on the name of the property, PCB Footprint here, to select the whole row or column.
3. Right-click and choose Edit... , which opens a spreadsheet with a single cell.
4. Enter the value into the cell and click OK. This value is copied into all parts.

This sounds fine, but how do you select all the parts with identical footprints? Capture offers several methods for dealing with large designs. Here’s an example.

1. Make the project window active and choose Edit > Find.... Choose Parts and search for R*.
2. This opens the Parts Browser, which shows a list of the parts that match the search criterion. You can also open the browser with Edit > Browse > Parts, in which case it lists all parts.

3. Select the parts whose footprints should be identical and choose Edit > Properties... from the menu. This brings up a different form of properties spreadsheet.

4. Find the PCB Footprint column and enter the desired value into one cell. Copy it with the Copy button. Select the whose column by clicking on its heading and click Paste. The copied value now fills all cells.

2.2 Useful buttons on the toolbar

Figure 2 shows two handy buttons on the toolbar that are often overlooked.

- **Area select** controls the selection of objects by drawing a rectangle: whether they must be fully enclosed or merely intersected. This can also be chosen using Options > Preferences... and the Select tab.

- **Wire drag** controls whether or not objects are reconnected when they are moved around. (I find it hard to distinguish the two settings from the icons on the button.) This is useful if you wish to replace a component – you placed the wrong type of op-amp, for instance – and delete the incorrect object. By default Capture will not let you drop another op-amp into the empty space and connect it to the existing wires but this button permits it. The behaviour can also be set up using the Miscellaneous tab of Preferences.

3 PCB Editor techniques

This is a disorganised collection of techniques that I have found useful but seemed too complicated for the body of this handout (which is already far too long).

3.1 Modes of operation

I didn’t dwell on this because we would all rather try out the software than read a lengthy ‘theory of operation’ but here is a little more. The main point is that the tools in PCB Editor can be used in two different ways (see Getting Started with Physical Design for further details).

- **Menu-driven editing mode** or **verb–noun use model**. In this mode you first choose a command, either from the menu bar or by clicking a button, then the design element on which the tool should operate.
• **Pre-selection mode** or **noun–verb use model**. In this mode you first choose the object followed by the command, which is usually selected from the contextual menu by right-clicking.

Confusion can arise when you switch from one method to the other because the tools do not behave ‘cleanly’ if a command or object is already selected. Disable any active tool (right-click and choose **Done** if it is offered) and clear any selection (left-click outside the board or right-click and choose **Selection Set > Clear All Selections** if things do not appear to be working correctly.

The verb–noun approach is a little more cumbersome but it is much easier to see what is happening, particularly if you keep the control panels open. For example, if you choose Add Connect, the Find panel automatically selects Pins, Vias and so on – the items to which a connection can be added. The Options panel displays the etch layers available and options for the tracks, such as width and angle of bends. If the Move command is selected instead, different options are offered and other classes are activated in Find.

The noun–verb model is often more convenient when you know what you are doing and want to perform a set of operations on the same object. However, there is a huge number of possible operations and they don’t all fit into a contextual menu. PCB Editor therefore has different **Application Modes**, which can be selected from the menu bar with Setup > Application Mode or with a button. These are the two most important modes.

• **General Edit** (GEN) is the most useful mode and is optimized for arranging components and adding connections.

• **Etch Edit** (EE) is for drawing new tracks and editing existing tracks.

Placement Edit (PLC) was added in version 16.2 but is not useful for the simple designs described here, and Flow Planning (IFP) is not available in OrCAD. The current mode is shown near the right-hand end of the status bar below the windows.

The particular set of commands in the contextual menu depends on exactly what is selected. You may therefore need to adjust the Find control panel before you are able to select the desired element – a pin for Add Connect, for instance.

Use Setup > Application Mode > None to exit from the current application mode and return to a menu-driven editing mode (there is no button). No contextual menu is available and the Find control panel is deactivated until a tool or application mode is chosen again. PCB Editor appears ‘dead’ if there is no application mode nor tool selected.

If that isn’t enough, further shortcuts are described in **Getting Started with Physical Design**. The following actions take place by default when you click on an object and drag it, often while holding a modifier key down, and are the quickest ways of performing the most common tasks. In general editing mode:

• dragging a symbol, text or via moves it

• control-dragging a symbol, text or via duplicates it

• shift-dragging a symbol rotates (spins) it

• dragging a cline segment slides it
Similarly, in etch editing mode:

- dragging a cline segment slides it
- double-clicking a pin or via adds a connection (this can be shortened further to a single click with the contextual menu Customize > Enable Single Click Execution)

That should be enough for now!

### 3.2 Alternative design flow

If you don’t like the idea of the new board wizard, you can follow a more conventional flow to start the board. It gives a little more control.

1. Send the netlist from Capture to PCB Editor *without* first setting up a bare board. Leave the Input Board File empty in the Create Netlist dialogue box. PCB Editor opens with your new board.

2. Use **Setup > Outlines > Board Outline** to define the outline of the board and the route and package keepins, which are made identical. The same dialogue box can be used to change these outlines later. You might wish to draw a different route keepin with **Setup > Areas > Route Keepin**.

   I have not tried placing the components first and subsequently drawing the board outline and keepins around them. You would obviously have to ignore DRC errors and could not use Quickplace.

3. Import a technology file with **File > Import > Techfile** if you have one. Otherwise, work through the steps below.

4. Use **Setup > Cross-section** to define the number, names and types of layers. The default is two layers, which is fine.

5. Set up the grids with **Setup > Grids**. I suggest 100 mil for the non-etch layers and 25 mil for the etch.

6. Define the widths of tracks with **Setup > Constraints > Physical** and the separations with **Setup > Constraints > Spacing**. Select the upper All Layers spreadsheet in the tree on the left to bring up a row labelled DEFAULT on the right. Values entered here propagate into all nets, where you can override them for power nets and the like. While you are doing this, edit the vias in the Physical pane.

7. You might wish to tweak some of the parameters in **Setup > Design Parameters > Display**, such as the display of drill holes and the ratsnest. Their visibility is treated differently from other elements of the design. You can also enlarge the DRC markers.
3.3 More approaches for placing components

The simplest approach is to place components on the board roughly in position using the Placement dialogue box, then rearrange and reorient them later. You can also rotate and mirror components using the contextual menu while the Placement dialogue box is open. Curiously the command for rotation becomes Rotate rather than Spin.

OrCAD Capture 16.2 is better integrated with PCB Editor than in previous versions and provides another method to place components. Keep Capture open after you have sent the netlist to PCB Editor. Open the Placement dialogue box in PCB Editor as if you were going to place the components manually. Instead of selecting components from this dialogue box, return to Capture and select a component on your schematic. This component is automatically selected for placement and attached to the cursor in PCB Editor.

Communication between Capture and PCB Editor can also be used to identify components.

- If you select a component in Capture it becomes highlighted in PCB Editor. There is an item PCB Editor Select on the contextual menu in Capture but it appears to be redundant in version 16.2 – the highlighting happens automatically. (The opposite happens if the last command in PCB Editor was Dehighlight.)

- If you highlight a component in PCB Editor it is selected in Capture. Do this by selecting a component and choosing Highlight from the contextual menu (often on the Symbol submenu), or by selecting Display > Highlight from the menu bar and clicking on a component. (There used to be a ‘sun’ button on the toolbar for highlighting but it has vanished in version 16.2. The ‘eclipsed sun’ for dehighlighting is still there, though. Strange.)

These features require Intertool Communication (ITC) to be enabled in Capture. This is the default; check the Miscellaneous tab of the Preferences dialog box if it seems not to be working.

3.4 Design rules

The suggested design rules of 20 mil tracks with 20 mil separation do not permit a track to run between the pads of of an integrated circuit, 0.1” apart. This produces a board that is easy for inexperienced students to solder but makes it more difficult to route. If you wish to allow tracks between the pads, reduce the Minimum Line width to something like 12 or 15 mils in the New board wizard or Constraint Manager (the number depends on the spacing between your pads, of course). Remember to spread the wires after routing the board, which you will need to solder carefully! Mitzner [3] and Jones [3] offer useful advice on design rules and you should of course follow the guidance of your manufacturer.

Use the Constraint Manager to change the tracks and spacing for an existing design. Open Physical constraints, which means the widths of tracks. Select the upper All Layers spreadsheet in the tree on the left to bring up a row labelled DEFAULT on the right. Change the widths, which are copied into all nets. Similarly, choose Spacing and All Layers to adjust the spacings. Several widths can be specified in the Constraint Manager.

- Under Line Width, the Min (minimum) figure is used as the default and is the value specified in the New board wizard.
• I have made the Max (maximum) width double the minimum value. This is useful for parts of tracks that carry a high current.

• Sometimes it is helpful to make a track narrower than its usual minimum width for a short distance, perhaps to pass between pads. This is called a neck, for which you specify a minimum width and maximum length. I have given a width of 12 mil, about half the usual, with a length of 250 mil or \(\frac{1}{4}\)″, which is plenty to squeeze between a pair of pins. I’ll explain how to use this in section 3.6 on the following page.

Many more constraints can be set: See Creating Design Rules for an introduction. Full details are in Allegro Constraint Manager User Guide and Allegro Constraint Manager Reference, which have unfortunately been omitted from the documentation distributed with version 16.2. When everything has been set up perfectly, use the command File > Export > Technology File to write the constraints to a tech (.tcf) file, which can be used to configure future designs. This can also be done from PCB Editor.

3.5 Disappearing ground and power nets

PCB Editor likes to hide the nets for power and ground signals when it draws the ratsnest. This is obviously beneficial if you use separate ground and power planes but is unhelpful for one or two-sided boards. Unfortunately it has several ways of hiding the nets, which require different techniques for making them visible again. You might hope that Display > Show Rats > All would do what it says, but it does not! Here is the simplest method.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.

2. There is a column headed No Rat and the entry may be On in the rows for the power nets. Change them to (Clear).

3. Quit from the Constraint Manager and the nets should appear in the ratsnest.

If that doesn’t work, or the apparently unconnected pins are shown with a boxed X (like a checkbox), here is the next method.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.

2. Delete any entries in the column headed Voltage. These are constant (DC) voltages and therefore indicate a power supply.

3. Quit from the Constraint Manager and the nets should appear in the ratsnest.

If that doesn’t work either, here’s my final method.

1. Select the missing nets. That sounds tricky but is not. Set the Find control panel for Nets, hover the mouse over one of the unconnected pins and its net is selected (and named on screen). The pins appear in the worldview window too when the net is selected.

3. The list on the right-hand side of the Edit Property box should include Ratsnest_Schedule and its value is probably POWER_AND_GROUND. Click the Delete check box to get rid of this property. If there is a Voltage property, delete that too.

4. Click Apply and the net should appear. Click OK to get rid of the Property Editor.

3.6 Manual routing

PCB Editor offers many features to assist manual routing and I described only the most basic in the walk-throughs. More information is in Routing the Design with details in the references for individual commands, particularly add connect (20 pages!) and slide.

- Two methods can be used to change the width of a track along its length. For a narrower neck, left-click where the width should reduce and choose Neck mode from the contextual menu. The width of the track is reduced to the value specified in the physical constraints (section 3.4 on page 7). Click to mark the end of the neck and select Neck mode again to return to normal width. A DRC error is flagged if the neck is too long.

- More generally, click where the width should change and type a new value into the Line width box of the Options control panel. The drop-down menu offers recently used values. Alternatively, the width can be changed with the contextual menu.

- When you are close enough to the finishing point of a track (the target) that it can be drawn automatically, choose Finish from the contextual menu. PCB Editor completes the track for you.

- When you have drawn part of a track from one end, Target > Route from Target allows you to draw the rest from the other end, which is sometimes easier. Before doing this, check that PCB Editor has the same target as you – it may be aiming for another point on the same net. Use Target > New Target and click on your target if necessary.

- While routing, Options can be set with the control panel or most from Options > . . . on the contextual menu.

- Immediately after selecting the Add Connect command, the Options control panel shows No available via. Don’t worry, it will offer something more helpful as soon as you start a track. Different nets may use different vias, hence the lack of a default.

- Add a via by double-clicking or by left-clicking to mark the spot, then right-clicking and choosing Add Via. Check the the correct via and layers are shown in the Options panel.

- You may wish to adjust the setting of the Bubble option. Its default is Shove preferred, which pushes other tracks out of the way vigorously to create room for the new track being drawn. I prefer Hug only, which draws the new track as close to the old ones as the design rules permit, without moving anything. Hug preferred is intermediate.
3.7 Pours or fills

It is easy to fill the unused areas of an etch layer with conductor to provide screening. This is called a dynamic etch shape in PCB Editor and the procedures are described in Preparing the Layout. A dynamic shape is automatically redrawn in response to changes in other elements, unlike a static shape whose outline is fixed. Thus the filled area of a dynamic shape reflows around tracks and pads if they are moved.

Solid fill

I have used the one-transistor amplifier as an example. Figure 3 on the following page shows the PCB with a solid fill attached to the ground net. I’ll make it cross-hatched later (not necessarily a good idea).

If you have routed the board already, it is best to unroute the ground net before adding the shape or you get both the tracks and the fill. Alternatively, hide the ratsnest for the net before routing. Follow the opposite procedure to one of those described in section 3.5 on page 8; the simplest is to add a voltage to the Net Properties. This hides the net and shows the pins with a boxed X as a reminder that they are connected to a hidden power net.

1. Choose Shape > Global Dynamic Params... from the menu bar to set up the parameters first. There are several tabs.

   • Shape fill – increase the Line width and Spacing from 5 to 25 mils, consistent with the coarse design rules followed in this tutorial. The Border width becomes 25 automatically. I used the default Hori_Vert fill style.

   • Void controls – check the artwork format.

   • Clearances – increased to 25 mils.

2. Select Shape > Rectangular from the menu bar or click the Shape Add Rect button (shape add rect command).

   This is not the same as Add > Rectangle or the Add Rect button (add rect command), which produces an unfilled rectangle. Nor is it the same as Add > Frectangle (add frect command), which produces a static, filled shape.

3. Check the settings in the Options panel. The shape should be in the Bottom Etch layer and the fill should be Dynamic Copper. Select the name of the net to which the shape should be connected by clicking on the ‘...’ button and choosing Gnd or whatever it is called. (Leave the net as Dummy Net if you don’t want it connected to anything.)

4. Draw a large rectangle to include the whole board. It is automatically trimmed to the route keepin and PCB Editor creates spaces (voids) around the pins, tracks and text.

That’s it! A screenshot of the filled board is shown in figure 3 on the following page and I plotted the photomask in the usual way. An empty area called an antipad is left around pins of nets that are not connected to the fill. You might have expected that grounded pins would be surrounded immediately by fill but instead each pin has a thermal relief around it. This is an empty region crossed by a few lines of etch to provide electrical contact.
Thermal reliefs are needed because copper conducts heat as well as electricity. A pin surrounded by a large area of etch therefore cools more quickly after it has been soldered than one that has only a pad and a track. All pins must cool at a similar rate to give consistent joints if the board is soldered automatically so thermal reliefs are used whenever pins are connected to planes of etch rather than tracks. Maxfield [2] and Mitzner [1] explain this clearly. It isn’t such an issue when boards are soldered by hand; in fact the usual problem is overheating of small pads.

Crosshatch fill

Curiously, PCB Editor lets you create a solid shape with either static or dynamic fill but a cross-hatched shape must be created as static. This means that you must first create a dynamic shape with solid fill and change it to crosshatched. Be aware that many manufacturers recommend that fills should be solid rather than cross-hatched.

1. Choose Shape > Select Shape or Void from the menu bar or click the Shape Select button and select the desired shape.

2. Right-click and choose Parameters… from the contextual menu. Select the Shape fill tab and change the Fill style to Xhatch. Other parameters are inherited from the global dynamic parameters that you set up earlier.

Figure 4 on the next page shows a screenshot and photomask for a hori_vert fill. An island has appeared to the right of the transistor, which is a poor feature. It can be removed with Shape > Delete Islands.

Mitzner [1] describes more advanced techniques of handling planes, such as splitting a ground plane into regions for analogue and digital signals.

3.8 Copying the names of pins from Capture to PCB Editor

In my usual instructions, I ask you to label the pins of the connectors on the schematic drawing and later to write the same text to label the pins on the PCB. This is a poor procedure because the
Figure 4. Screenshot and photomask for the one-transistor amplifier with a hatched shape attached to the ground net.

two sets of labels might be inconsistent. It would be far more reliable if the names were copied automatically from Capture to PCB Editor. This can be done but is not as straightforward as it might be. These instructions are based on advice from Joewi, Bill Dempsey, tltoth and oldmouldy in threads 10494 and 10835 on the Cadence PCB Design Forum.

1. In Capture, select the components whose pins are to be named. Open the Property Editor and choose the Pins sheet.

2. Click New Row... (or New Column...) to create a new property and give it an appropriate name, such as SSNAME (for silkscreen name).

3. Enter names for each pin into the row for SSNAME. Make the property visible with Display... so that it shows on the schematic.

4. Two steps are needed in the Setup dialog box for netlisting the design and sending it to PCB Editor. First, the easy one: Activate the checkbox for Allow User Defined Property.

5. Click on the Setup... button across from Create PCB Editor Netlist. The dialog box shows the Configuration File, called allegro.cfg. We need to Edit... this.

   • Add the line SSNAME=YES to the section for [pinprops] at the end of the file, which tells the netlister to include this property in the netlist.
   
   • Save the edited configuration file in a different location, such as the allegro directory for the current project, or give it a different name in the default location. Do not overwrite the supplied file (even if you have permission).

   • Still in the Setup dialog box, use the ‘...’ button to select the edited configuration file.

6. Run the netlister, wait for PCB Editor to open the board and place the components as usual. SSNAME is not yet visible.

7. Choose Display > Property... from the menu bar and select the Graphics tab. Scroll down the list of Available Properties and click on our added property, whose name has
Figure 5. Board for one-transistor amplifier with all pins named.

probably changed to Ssname. SSNAME appears under Selected Properties. Increase the Text block from its default of 1, which is tiny. The drop-down list for Subclass contains only the single entry PROPERTIES, which is part of the Manufacturing class. Click Create and the SSNAME text appears on the drawing. It can be moved and rotated in the usual way.

Whew! A slightly simpler alternative is to use Name, which is a standard property of a pin. Follow exactly the same procedure except that you do not need to define the new property. Curiously, you must still select Allow User Defined Property even though it was not defined by the user. The snag is that the name is now shown for every pin, which can clutter the board – see figure 5.

3.9 Controlling the display of text and other elements in PCB Editor

The footprints supplied with PCB Editor contain a great deal of text (this has been cleaned up in our local footprints). Four items (classes) are displayed:

- **ref des**, such as C1
- **component value**, such as 1u
- **tolerance**, to which I did not assign a value and therefore appears as ***
- **user part number**, which I did not use either

The device type is shown for components that do not have a value, such as the jumpers. Two subclasses are shown for each of these:

- **silkscreen_top**, which is merged with the silkscreen_top subclasses from other classes to produce the complete top silkscreen by running the Auto Silkscreen command.
- **assembly_top**

I suggest that you hide the tolerance and user part number (unless you use them, of course) and keep only the silkscreen_top subclass visible. Here are two ways of doing this.
Options control panel

Pin the Options control panel open.

1. Set the active class to Tolerance/Assembly_Top
2. Click the colour swatch to the left of the drop-down list of subclasses. It turns black to show that this subclass is now hidden and the corresponding text disappears from the drawing.
3. Repeat this for the Silkscreen_Top subclass.
4. Repeat these steps for all the other classes and subclasses to be hidden.

Color Dialog

Open the Color Dialog with Display > Color/Visibility.

1. Select the Components folder in the list on the left.
2. Click the All check box for the Assembly_Top row twice: the first click turns on the visibility for all subclasses and the second clears them all.
3. Do the same for the Tol. and UserPart columns to turn all of them off.
4. Click Apply or OK to update the drawing.

It is a good idea to save the colour settings when you have turned off unwanted elements. Use View > Color View Save from the menu bar (colorview create command) to save the current settings to a file. Its name appears in the list of Views in the Visibility control panel in the same way as the artwork films.

The same methods can be used to hide other unwanted classes, such as the individual silkscreens after the composite silkscreen has been created.

3.10 Creation of package symbols (footprints)

It is straightforward to create a new package symbol (footprint) in PCB Editor and the procedure is clearly described in Defining and Developing Libraries. Two files are associated with each symbol.

- The **drawing** (.dra) file is used to create and edit the symbol with PCB Editor in its symbol mode. This offers a slightly different set of menus and toolbars from the usual layout mode. For example, the menu bar gains **Layout** while losing others, such as **Route**.

- The **package symbol** (.psm) contains additional information, such as a place-bound rectangle, but cannot be edited. It should be stored in a library, where it can be found when the symbol is placed on a new board. PCB Editor compiles the symbol automatically whenever you save the drawing, contrary to statements in some of the manuals.
Other types of symbol include mechanical symbols (.bsm) for features such as mounting holes.

Figure 6 shows the result with a few embellishments. I recommend placing the pins with the Package Symbol Wizard; it is easy to get the origin wrong if you add pins by hand.

1. First identify or create the padstacks needed for each electrical pin. Typically you need two, a square or rectangle for pin 1 and a circle or oblong for the remainder. Use our local padstacks, with the prefix GU-, because they have been edited to include a filmmask that acts as a guide to the drill. See section 3.11 on the following page if you need to create new padstacks.

2. Run the Package Symbol Wizard, most of which is fairly obvious. Choose the symbol origin to be at Pin 1 for a pin-through-hole component to ensure that the pins line up with a 100 mil grid when the component is placed.

   The wizard creates numerous elements in the drawing that may be superfluous. I often delete everything except the pins and the refdes on the top silkscreen.

3. If you prefer to place the pins yourself, choose Layout > Pins from the menu bar. In the Options control panel, choose the padstack for pin 1 by clicking on the “…” button. Place this pin at the origin, either by clicking at the correct point or (more reliably) by clicking on the P (pick) button, typing “0 0” (zero space zero) and clicking Pick.

   Choose the padstack for the remaining pins in the same way. You can either place them manually (a 100 mil grid helps) or use the Quantity settings to place several at once. Right-click and choose Done when all pins are placed.

4. Draw the outline of the body of the component on Package Geometry/Assembly_Top. (The wizard produces a plain rectangle but a DIP should have a notch to mark the end with pin 1.) Reduce the grid spacing to 25 mil.

   Use Add > Line for the drawing; it is really a polygon tool because each click adds a segment to the end of the previous line. Zero width is fine. I have found it better to use the line tool even if the outline is a rectangle. Add any further features desired, such as a + sign for a polarized component.
5. Copy the outline on to Package Geometry/Silkscreen_Top as follows. Make sure that no elements are selected, then choose Edit > Copy. Set the Options for only lines, then drag a rectangle around the objects that you have drawn to select them all. Click on the original to pick them up, then click again to place a copy well clear of the original. Right-click and choose Done. Now drag a rectangle around the copy to select it all, right-click and choose Change to Layer > Silkscreen_Top (alternatively use Edit > Change). Finally, choose Edit > Move, drag a rectangle around the copy to select it, click to pick it up and click again to drop it over the original. Choose Done.

6. Add text to show the value of the component. Use the special command Layout > Labels > Value and choose the Silkscreen_Top subclass. Text block 3 is a suitable size. (Alternatively, the usual Add > Text command seems to do exactly the same.) The text is replaced by the value of the component when it is used on a board so I type the name of the symbol into this field. This is helpful if you place your new symbols into an empty board drawing to make a catalogue of your library.

7. Repeat this for the Refdes if you did not use the Package Symbol Wizard, which adds this automatically. Enter a placeholder such as U* for an IC.

The symbol in figure 6 on the previous page contains a few extra features. It is intended for a dual-in-line IC mounted in a socket on a board without plated-through holes.

- The outline (cyan) shows the socket as well as the DIP8 IC itself.

- A rectangular route keepout (magenta) surrounds each row of pins. This prevents tracks running to the top pads of the pins, where they cannot be soldered because the socket is in the way. Use Add > Frectangle and set the active class to Route Keepout/Top. In fact you can use Add > Rectangle or the Add Rect button, which are officially for unfilled rectangles, but PCB Editor creates filled rectangles automatically where appropriate. For a more complicated shape use Shape > Polygon. The Options default to the type Static solid, which is appropriate.

- Another rectangle for Via Keepout/All surrounds the whole symbol. This excludes hand-soldered vias where they would obstruct the socket.

- The padstacks have smaller pads on the top than the bottom because no tracks should run to the top; the top pads are markers only.

The completed symbol should be stored in the design’s allegro folder so that PCB Editor can find it automatically.

### 3.11 Creation of local padstacks with filmmask

The padstacks in our local library include a filmmask to provide a guide to the drill for pin-through-hole components and give generous clearance around the pads on a ground plane. This is the procedure to create a new padstack if necessary. It may be easiest to copy an existing padstack and modify it, rather than create a new one from scratch. Each padstack has a separate file with extension .pad. See Library Padstacks in Defining and Developing Libraries,
Figure 7. Parameters tab of the Padstack Designer.

Layout Padstacks, Vias, and Etch Shapes in Preparing the Layout, and Padstack Designer in P Commands for full details of the Padstack Designer. The name of its window varies slightly, depending on whether it was started in standalone mode or from PCB Editor.

Run the Pad Designer from the Start menu (it is in a subfolder OrCAD PCB Editor Utilities) and open a padstack with the File menu. You should see a window similar to figure 7; click the Parameters tab if it is behind the Layers tab. Change the Drill diameter to the desired value.

Now make the Layers tab active as in figure 8 on the next page. The rows for the filmmasks are probably blank unless you have modified a gui-padstack. Click on FILMMASK_TOP to edit it. In the group below for Regular Pad, choose the Geometry to be Circle and the Width to be 20. Repeat this for FILMMASK_BOTTOM. These layers now have small circles that become the guide holes in the final plot. The other layers can be left unchanged. Save the pad.

3.12 Miscellaneous PCB Editor tips

- PCB Editor seems to have no Unroute Board command, which would be helpful if you made a complete mess of routing. One method is to reload the design, assuming that you saved it first. Alternatively, do this.

1. Select Nets only in the Find control panel.
2. Drag across the design to select all the nets.
3. All the nets are now highlighted in the design window. Right-click and Ripup etch.
The conversion of libraries from Layout is described under the orcad in command in *O Commands*. Names of symbols are highly restricted in PCB Editor so you may find that you have to rename all your footprints (sigh...). I found the conversion generally reliable but the text for values vanished and a few symbols acquired DRC errors.

It would be convenient if the schematic circuit could be drawn once with both ‘virtual components’ such as sources for simulation and sockets for the real PCB. Unfortunately this cannot be done without editing the components in the pspice library because some have pins numbered 0, which allegro rejects. Many of the libraries are full of bugs. Some components have pins ‘numbered’ with letters (such as the electrolytic capacitor) and some aren’t numbered at all. Avoid the libraries in *oldlibs*.

I find it helpful to adjust the grids provided by the new board wizard, which are the same for everything. Choose Setup > Grids... from the menu bar. I suggest spacings of 100 for Non-Etch (essentially the components) and 25 for etch. If you enter a value for All Etch it is copied to all etch layers, which saves some typing.

Lines in the ratsnest are ‘jogged’ by default. If you prefer to join the components with straight lines instead, choose Setup > Design Parameters... from the menu to bring up the Design Parameter Editor. Select the Display tab and adjust the Ratsnest geometry to Straight.

Two types of ‘design’ file both use the extension *.dsn*, but have entirely different contents.
Capture has a design file to hold its database (Windows calls it a Data Source Name)
PCB Editor uses a design file to export the board to the autorouter.

Don’t mix them up! This is one reason for setting up a separate allegro directory.

- There is a high chance of error if you copy names of footprints from a document and type them manually: It is better practice to select them from a library. Unfortunately this is clumsy in PCB Editor.

1. Choose Place > Manually... from the menu bar.
2. Click the Advanced Settings tab and choose to Display definitions from Library.
3. Return to the Placement List and select Package symbols from the drop-down list. You now see a list of all packages in the libraries.
4. Scroll down to find the outline that you want, res400 for example. Click in the check box next to the component and a graphic appears in the Quickview window. This helps you to confirm that it is the correct outline, although there is no scale.
5. Select the Text radio button and the name of the component appears. You can copy this and paste it into the Properties Editor in Capture.
6. Dismiss the Placement box with Cancel when you have finished and quit from PCB Editor without saving any changes.

A listing of the directory might be easier! Layout was much better.

4 SPECCTRA techniques

Tracks can be edited in SPECCTRA instead of PCB Editor. This is handy for moving badly-placed vias; I found it easier than PCB Editor. Right-click in the window, which brings up the INTERACTIVE ROUTING MENU. Move mode is probably the most useful. You can then select tracks or vias and move them. Do this before the finishing touches of spreading and mitring. In fact you can do most of the placement in SPECCTRA as well as the routing but I didn’t want to describe yet another interface.

If you export a fully or partly routed board from PCB Editor to SPECCTRA, the imported tracks are protected against changes in SPECCTRA. Choose Edit > [Un]protect > Wires by Net... (or Wires by Layer List...) to remove the protection. You can then unrout these tracks and reroute the board.

References

[1] Kraig Mitzner, *Complete PCB Design using OrCAD Capture and PCB Editor*, Newnes (Elsevier), 2009, ISBN 9780750689717, about £40. This covers PCB Designer in far more detail than this tutorial including many advanced techniques that I haven’t mentioned including split planes and gate swapping. It also includes general aspects of PCB design, not just OrCAD. Highly recommended.

[3] David L Jones, *PCB Design Tutorial*, [www.alternatezone.com](http://www.alternatezone.com). This is a good, practical guide to the design and manufacture of PCBs but not specific to OrCAD. The comments on CAD software are a little out of date but it is full of real-world advice.