Solutions to examples on data conversion

2.1 \( \text{LSB} = (3.3 \text{ V})/2^{12} = 0.8 \text{ mV}. \)

2.2 The output of an \( n \)-bit converter is given by \( (V_{\text{ADC}}/V_{\text{FS}}) \times 2^n \) rounded to the nearest integer, except that the maximum value of \( 2^n \) is impossible. Here \( n = 12 \) and \( 2^n = 4096 \) so we get (i) \( 0.1 \times 4096/5.0 = 81.92 \), which rounds to 82; (ii) \( 1.0 \times 4096/5.0 = 819.2 \), which rounds to 819; (iii) \( 4.0 \times 4096/5.0 = 3276.8 \), which rounds to 3277; (iii) 5.0 is the full-scale input so the output is also the maximum, 4095 – it cannot be 4096! These are decimal; in hexadecimal they are 0x052, 0x333, 0xCCD, 0xFFF.

2.3 This is of course the inverse of the previous question but with the difference that the input voltage can lie in a range; it is not a single number because of the quantization. In most cases the input can lie in a range of \( \text{LSB} = (2048 \text{ mV})/2^8 = 8 \text{ mV}. \) The exceptions are the ranges at the ends. The analogue input voltage in the middle of the normal intervals is related to the digital output \( d \) by \( V_{\text{ADC}} = V_{\text{FS}} \times (d/2^n) = 8d \text{ mV}. \)

(i) Zero output corresponds to inputs of zero to \( \frac{1}{2} \text{LSB}, \) which is 0–4 mV. This has only half the width of the normal intervals.

(ii) The midpoint is 72 mV and this has the normal spread of \( \pm \frac{1}{2} \text{LSB} \) so the range of possible inputs is 68–76 mV.

(iii) 0xAB is 171 in decimal so the midpoint is 1368 mV and the range is 1364–1372 mV.

(iv) This is the top of the scale, which is the other abnormal interval. 0xFF is 255 in decimal so the usual midpoint would be 2040 mV. In this case the range goes down \( \frac{1}{2} \text{LSB} \) but up by a whole LSb, giving 2036–2048 mV.

2.4 The number of possible output values is \( 1.8 \text{ V}/1 \text{ mV} = 1800. \) This must be rounded up to the next power of two, \( 2048 = 2^{11}. \) Thus an 11-bit converter is needed. (These are unusual and you would probably have to go for 12 bits.)

2.5 It arises from the unavoidable difference between the staircase and straight line. Of course it reduces as the number of bits increases because LSB gets smaller.
3.1 A flash converter compares the input with voltages of \( \frac{1}{2} \) LSB, \( \frac{3}{2} \) LSB and so on. For a 4-bit converter \( \text{LSB} = V_{\text{FS}}/16 \) so the 15 voltages for comparison are \( \frac{1}{32} V_{\text{FS}}, \frac{3}{32} V_{\text{FS}} \) and so on up to \( \frac{29}{32} V_{\text{FS}} \). The wider top interval means that \( \frac{31}{32} V_{\text{FS}} \) is not required.

For a 5 V range the voltages are \( \frac{5}{32} V, \frac{15}{32} V \) and so on up to \( \frac{145}{32} V \) or \( 0.15625 V, 0.46875 V \ldots, 4.53125 V \).

3.2 The input voltage in terms of LSB is \( 3.5 = \frac{10}{3} \). The comparators have voltages of \( \frac{1}{2} \) LSB, \( \frac{3}{2} \) LSB and so on. The output will be 1 from the comparators up to \( \frac{9}{12} \) LSB = \( \frac{19}{2} \) LSB, which is 10 comparators. The remaining 5 will give zero. Thus the thermometer code has 10 low bits of 1 and 5 high bits of 0: 0b000001111111111. Decoding this gives a decimal value of 10 or normal binary of 0b1010. This is the nearest integer to 9.6, which is what we expect.

3.3 It’s easier to write this out for \( V_{\text{ADC}}/V_{\text{FS}} = 3/5 = 0.6 \). Here is the sequence of four comparisons for a 4-bit ADC.

1. Compare with half full range: \( 0.6 > \frac{1}{2} \) so bit = 1.
2. Split upper range from \( \frac{1}{2} \) to 1 in two to get \( \frac{3}{4} \) and compare: \( 0.6 < \frac{3}{4} \) so bit = 0.
3. Split lower range from \( \frac{1}{2} \) to \( \frac{3}{4} \) in two to get \( \frac{5}{8} \) and compare: \( 0.6 < \frac{5}{8} \) so bit = 0.
4. Split lower range from \( \frac{1}{2} \) to \( \frac{5}{8} \) in two to get \( \frac{9}{16} \) and compare: \( 0.6 > \frac{9}{16} \) so bit = 1.

Thus the output is 0b1001 = 9 but we expect it to be 10! Oh dear . . . 

The problem is that this method always gives the integer below the exact value, not the nearest integer. None of the application notes or books makes this clear! One way of solving this problem might be to add an offset to the capacitor network. Another is to perform one extra comparison:

5. Split upper range from \( \frac{9}{16} \) to \( \frac{5}{8} \) in two to get \( \frac{19}{32} \) and compare: \( 0.6 > \frac{19}{32} \) so extra bit = 1.

This shows that the result should be rounded up from 9 to 10.

3.4 The first comparison is with \( \frac{1}{2} V_{\text{FS}} \), which gives the msb.

3.5 The fractional deviation from perfect charging must be less than \( \frac{1}{2} \times 2^{-12} \approx e^{-9} \). Thus 9 time-constants \( \tau \) must be allowed. For the given values, \( \tau = RC = 0.8 \mu s \) and \( 9 \tau = 7 \mu s \).

The output resistance is in series with the internal resistance so the total rises from 2 k\( \Omega \) to 12 k\( \Omega \), a factor of 6. This affects \( \tau \) with the same factor so the sampling time should be increased to about 43\( \mu s \).

3.6 The ratio of the input voltage to the reference is given by the ratio of the count to the range of the counter, so \( V_{\text{ADC}} = 10 \times 838859/2^{20} = 10 \times 838859/1048576 = 7.999998 \) V. The result must be quoted to this precision.

The resolution is 1 in \( 2^{20} = 1 \) in 1048576 \( \approx 1 \) in \( 10^6 \). The corresponding voltage is \( \text{LSB} = 10 \mu V \).

The reference voltage must not change by more than 1 part in \( 2^{20} \) over a range of 25\°C, so the coefficient must not exceed \( 1/(2^{20} \times 25) = 4 \times 10^{-8}/\text{°C} = 0.04 \text{ppm/°C} \). It will not be easy to meet this specification!
4.1 The frequency of sampling must be at least the Nyquist frequency $f_N$ for the sampled sequence to be a faithful representation of the continuous input. In other words, it is possible to reconstruct the input from the sequence. Higher frequencies are aliased, which means that they give the same sequence of samples as a lower frequency. The formula is $f_N = 2f_{\text{max}}$, where $f_{\text{max}}$ is the maximum frequency in the input.

4.2 The signal must be sampled at double its maximum frequency or more, so the minimum rate of sampling is 100 kilosamples per second. Aliasing would occur if a lower rate were used: high-frequency signals would appear to have a lower frequency after sampling.

6.1 First imagine connecting the noninverting terminal of the opamp to ground instead of $V_{\text{bias}}$. This leaves a standard inverting amplifier, which gives the second term on the right-hand side of equation (6.3).

Next, restore $V_{\text{bias}}$ but connect the input of the circuit to ground instead of $V_{\text{in}}$. This leaves a standard noninverting amplifier with $V_{\text{bias}}$ as input, which gives the first term on the right-hand side of equation (6.3).

6.2 Well, something to provide a signal, of course... More seriously, the intended answer is a low-pass filter to remove noise and prevent aliasing. An amplifier may also be needed.

6.3 An integrating or sigma–delta ADC should average over a whole number of cycles to reduce interference. This means sampling at 400 Hz or submultiples, 200, 133, 100 Hz and so on. None of this would help with a SAR ADC, which samples its input over a short interval. On the other hand, it would be possible to average the outputs from a SAR over a period of the power supply in software. This achieves the same effect.

6.4 Differential inputs, high input impedance on both inputs, ‘high’ gain for differential inputs, programmed by a single resistor, and low gain for common-mode inputs. It may also shift the output voltage by an offset.

6.5 I hope that you remember how to do analyse this sort of circuit! Here are the usual three steps.

1. Work out the voltage on the non-inverting input, $v_+$. This is set by the potential divider so $v_+ = V_{CC} \times R_3/(R_3 + R_4) = (5/11)V_{CC}$. We are assuming that no current flows into the non-inverting input because an ideal op-amp has infinite input resistance.

2. An ideal op-amp has infinite gain and does whatever is necessary with negative feedback to bring its inputs to the same potential, so $v_- = v_+$.

3. We now know $v_-$ and can apply nodal analysis at the inverting input, again assuming that no current flows into the op-amp. We also assume that the op-amp has zero output resistance, which means that the load has no effect on the output voltage $V_{out}$. Here the load is just the feedback circuit.

The last step is, as usual, the only one to require any work. Nodal analysis gives

$$\frac{V_{\text{in}} - v_-}{R_1} + \frac{V_{\text{out}} - v_-}{R_2} + 0 = 0. \quad (15.6)$$
I’ve added a 0 as a reminder that no current flows into the op-amp. Rearranging this gives

\[ V_{\text{out}} = -\frac{R_2}{R_1} \left( V_{\text{in}} - \frac{R_1 + R_2}{R_2} v_- \right) \]

\[ = -10(V_{\text{in}} - \frac{11}{10}v_-) \]

\[ = -10(V_{\text{in}} - \frac{1}{2}V_{\text{CC}}). \quad (15.7) \]

The output must line between ground and \( V_{\text{CC}} \), assuming true rail-to-rail output. This determines the range of inputs. Clearly \( V_{\text{in}} = \frac{1}{2}V_{\text{CC}} = 1.5 \text{ V} \) gives \( V_{\text{out}} = 0 \). The other limit is \( V_{\text{out}} = V_{\text{CC}} \), which needs \( V_{\text{in}} = 0.4V_{\text{CC}} = 1.2 \text{ V} \). Thus the input must lie between 1.2 and 1.5 V for correct operation. There would be no point in specifying rail-to-rail inputs.

A simple inverting amplifier could not be used because a positive input would lead to a negative output, which cannot be provided with a single supply. An inverting amplifier must have a shift to work in a single-supply system.

6.6 I’ll choose an inverting amplifier to match the text. The circuit will be the same as figure 6.7 on page 45 except for the values of the resistors.

1. The range of input voltage is 0.1 V and the range of output voltage is 3.0 V so the gain is −30. This is given by \(-R_2/R_1\) in the usual way so we need \( R_2 = 30R_1 \). A suitable choice using standard values is \( R_1 = 3.3 \text{ kΩ} \) and \( R_2 = 100 \text{ kΩ} \).

2. Substitute a pair of values for \( V_{\text{in}} \) and \( V_{\text{out}} \) into equation (6.3) or (6.4) to find \( V_{\text{bias}} \). Choose \( V_{\text{in}} = 0.3 \text{ V} \) and \( V_{\text{out}} = 0 \text{ V} \) in equation (6.3), which gives

\[ 0 = 31V_{\text{bias}} - 30 \times 0.3 \text{ V}. \]

Thus \( V_{\text{bias}} = (9/31) \text{ V} \).

3. The potential divider formula for \( R_3 \) and \( R_4 \) gives

\[ V_{\text{bias}} = \frac{R_4}{R_3 + R_4} V_{\text{CC}} = \frac{9}{31} \text{ V}. \]

This can be rearranged to

\[ \frac{R_3}{R_4} = \frac{28}{3}. \quad (15.10) \]

It is not possible to find suitable numbers within the most common set of values (E12, described in section 15.4). The problem is that the ratio of successive values in E12 is about 1.2 but 3.0/2.8 = 1.07, which inevitably lies between values. You could make a suitable value for \( R_3 \) by putting two values in series. Alternatively, try the E24 series, which offers twice as many values. I found that \( R_4 = 16 \text{ kΩ} \) and \( R_3 = 150 \text{ kΩ} \) gave the ratio very closely.

7.1 The fractional change in voltage must be smaller than \( 1/2^n \) for an \( n \)-bit converter to avoid errors of a single bit or more. For an 8-bit converter this needs a change of less than \( 1/256 \) so the range of temperature \( \Delta T \) must obey \( 5 \times 10^{-5} \Delta T < 1/256 \) so \( \Delta T < 78^\circ \text{C} \). The range is reduced by \( 2^4 = 16 \) to \( 2^\circ \text{C} \) for a 12-bit converter.
7.2 This is the reverse of the previous question. The temperature coefficient \( C \) must obey \( C \Delta T < 1/2^n \) or \( C < 1/(2^n \Delta T) \). For 8 bits this needs \( C < 1/(256 \times 70) = 5 \times 10^{-5}/\degree C = 5 \times 10^{-3}\%/\degree C = 50 \text{ ppm/\degree C} \). I have rounded the coefficient down to one significant figure. The other numbers follow in the same way.

7.3 Call the minimum and maximum resistance of the thermistor \( R_{\text{min}} \) and \( R_{\text{max}} \). Then the range of voltage from the potential divider is

\[
\Delta V = V_{\text{CC}} \left( \frac{R_{\text{max}}}{R_{\text{ref}} + R_{\text{max}}} - \frac{R_{\text{min}}}{R_{\text{ref}} + R_{\text{min}}} \right) \quad (15.11)
\]

\[
= V_{\text{CC}} \frac{R_{\text{ref}}(R_{\text{max}} - R_{\text{min}})}{(R_{\text{ref}} + R_{\text{max}})(R_{\text{ref}} + R_{\text{min}})} \quad (15.12)
\]

(a couple of terms cancelled from the numerator). Now we have to find the maximum as a function of \( R_{\text{ref}} \), which requires differentiation and setting the result to zero. Clearly the result is going to be a mess! Fortunately we need only to know when the derivative is zero so we can forget about its denominator. In other words, we want the derivative of \( f/g \) and the usual rule gives \((f'g - fg')/g^2\), but we just need to find the value of \( R_{\text{ref}} \) that gives \( f'g - fg' = 0 \). Here goes.

\[
(R_{\text{max}} - R_{\text{min}})(R_{\text{ref}} + R_{\text{max}})(R_{\text{ref}} + R_{\text{min}}) - R_{\text{ref}}(R_{\text{max}} - R_{\text{min}})(2R_{\text{ref}} + R_{\text{max}} + R_{\text{min}}) = 0. \quad (15.13)
\]

I multiplied out the denominator to find its derivative. We can cancel the factor of \((R_{\text{max}} - R_{\text{min}})\) and multiply out the remaining brackets. Most terms cancel to leave

\[
R_{\text{ref}}^2 - R_{\text{max}}R_{\text{min}} = 0 \quad (15.14)
\]

so

\[
R_{\text{ref}} = \sqrt{R_{\text{max}}R_{\text{min}}}. \quad (15.15)
\]

The numbers here give \( R_{\text{ref}} = 14 \text{ k}\Omega \) to the nearest kilohm; 15 k\( \Omega \) is the closest standard value.

With 15 k\( \Omega \) and a 3 V supply the voltages from the potential divider go from 1.20 V to 1.71 V. The range is now 0.51 V compared with 0.36 V before. It’s a significant improvement but an amplifier would do far better.

7.4 In 8-bit mode LSB \( = (3.3 \text{ V})/256 \approx 13 \text{ mV} \) at the input to the ADC. This is 1.3 mV at the input to the amplifier, which is the output of the sensor, and therefore 0.13\(^\circ\)C.

7.5 The answer to a question like this is inevitably No but it needs justification! Suppose that we designed the amplifier so that LSB corresponds to 0.1\(^\circ\)C. The output from the LM35 is 1 mV and LSB \( = (3.3 \text{ V})/1024 = (3300 \text{ mV})/1024 \) so the gain should be 3300/1024 = 3.22.

7.6 The trivial answer would be ‘No problem, the amplifier now gives 0.0–3.0 V for this range of temperatures’. The difficulty is that even an amplifier with so-called rail-to-rail output cannot give an output of 0 V, so the system would fail at the lowest temperatures.

This is an ideal application for the LM7705 or a similar negative bias generator, which would enable the output of the noninverting amplifier to go down to zero.
Alternatively, add an offset voltage to the amplifier, which would have to be changed to an inverting configuration as in figure 6.5 on page 43. Choose a gain of $-10$ instead of $+10$ for convenience. The inverting amplifier could then map $0 \, \text{V} \rightarrow 3.2 \, \text{V}$ and $0.3 \, \text{V} \rightarrow 0.2 \, \text{V}$. Equation (6.3) shows that this needs $V_{\text{bias}} = (3.2/11) \approx 0.29 \, \text{V}$. 

7.7 With a direct connection we need 1 mV resolution in 2.5 V, which needs 2500 values. This is a bit too high for $2^{11} = 2048$ so 12 bits are needed. The resolution is $\text{LSB} = (2.5 \, \text{V})/2^{12} = 0.6 \, \text{mV}$. 

Only 500 values are needed if the amplifier boosts the signal to the full range of the ADC. This number is just the range of inputs (0.5–1.0 V) divided by the resolution. This is conveniently just below 512 = $2^9$ so a 9-bit converter would be sufficient (if such a device exists). The actual resolution would be $(500 \, \text{mV})/2^9 = 0.98 \, \text{mV}$. 

The amplifier needs to provide both gain and offset. To provide perfect matching it would need a gain of $2.5/0.5 = 5$ and an offset to bring the output to 0.0–2.5 V. If an inverting amplifier is used, equation (6.3) on page 44 shows that $V_{\text{bias}} = 2.5/6 \approx 0.42 \, \text{V}$ is needed. However, problems may arise if the system works from a single supply because the output of the op-amp would be unable to go all the way down to 0 V. See section 7.5 on page 58 for how to solve this problem.

7.8 The potential divider gives

- Light: 0.73 V and 1.2 kΩ
- Dark: 3.12 V and 5.3 kΩ (not far from $V_{\text{CC}}$ and 5.6 kΩ)

The worst case is in the dark, where the total resistance is $5.3 \, \text{kΩ} + 7.5 \, \text{kΩ} \approx 13 \, \text{kΩ}$ and $\tau = 13 \, \text{kΩ} \times 15 \, \text{pF} \approx 0.2 \, \mu\text{s}$. The usual calculation shows that the number of time constants should be greater than $13 \ln 2 \approx 9$, giving $1.8 \, \mu\text{s}$. This is 234 cycles of a 13 MHz clock.

A comparator would be sufficient if the system had only to distinguish between light and dark.

7.9 Taking the hint in the question allows the circuit to be simplified as in figure 15.17. Nodal analysis at the central junction gives

$$\frac{V_{\text{in}} - V_{\text{CC}}}{R_{\text{ref}}} + \frac{V_{\text{in}} - 0}{R_{\text{th}}} + \frac{V_{\text{in}} - V_{\text{bias}}}{R_{1}} = 0. \tag{15.16}$$

Multiply out the fractions and collect terms. It’s a bit of a mess but straightforward. The result is

$$V_{\text{in}} = \frac{R_{1} R_{\text{th}} V_{\text{CC}} + R_{\text{ref}} R_{\text{th}} V_{\text{bias}}}{R_{1} R_{\text{th}} + R_{\text{th}} R_{\text{ref}} + R_{\text{ref}} R_{1}}. \tag{15.17}$$

In fact this is not the best route. It is clearer to replace the potential divider formed by $R_{\text{th}}$ and $R_{\text{ref}}$ with its Thévenin equivalent. This gives the alternative expression

$$V_{\text{in}} = \frac{R_{\text{th}} V_{\text{CC}}}{R_{\text{ref}} + R_{\text{th}}} \frac{1}{R_{1} + R_{s}} + \frac{R_{s} V_{\text{bias}}}{R_{1} + R_{s}}. \tag{15.18}$$
Figure 15.17 Analysis of thermistor and input resistance of inverting amplifier.

where $R_s = R_{ref}$ is the Thévenin resistance of the divider. The first fraction in the first term is the potential from the unloaded divider and the second fraction shows how this is reduced by the input resistance of the amplifier, $R_1$. The second term arises from the bias.

It’s probably best to substitute numbers now. For $R_{th} = 20\,k\Omega$ we found $V_{in} = 0.86\,V$ before, which falls to 0.82\,V including $R_1$. That’s about a 5% error. At the other end of the range, where $R_{th} = 10\,k\Omega$, $V_{in}$ rises from 0.50\,V to 0.62\,V. This is an error of nearly 25%. Several solutions are possible. We could use a non-inverting amplifier with offset to raise the input resistance. Alternatively, we could stick with the circuit in figure 7.5, calculate the error and compensate for it in software.

8.1 The general formula is $V_{out} = V_{ref} \times d/256$ where $d$ is the digital input. The maximum output is given by $d = 255$, not 256! It is 4.98\,V.

8.2 Same as before.

8.3 The main point is that 5\,V is 500 intervals of 10\,mV so the period of the PWM signal should be 500. It can then be varied to give the desired resolution. This would be no problem with a a 16-bit timer because $500 < 2^9$.

8.4 A 12-bit simple string needs $2^{12} = 4096$ resistors. They all have the same value, unlike the resistors in a flash ADC. If it were segmented, each string would need $2^6 = 64$ resistors giving a total of 128. Of course this would also need buffers, switches and logic to drive the interpolator.

8.5 The current through each resistor is $2.5\,V/100\,k\Omega = 25\,\mu A$ and there are $2^8 - 1 = 255$ of them so the reference must provide about 6.4\,mA, which is rather high by modern standards – this is not a low-power device!

The current is ‘multiplied’ by the 1\,k\Omega feedback resistor to give 25\,mV for each 25\,\mu A. Thus the outputs are negative 0, 25\,mV, 50\,mV, . . . up to a maximum of 6.375\,V from all 255 sources. Remember that, like all DACs, it cannot produce 256 currents and 6.4\,V!

8.6 The most significant 4 bits need 15 current sources and therefore 15 resistors. The $R$–$2R$ ladder has an extra section compared with that shown in the lecture notes and therefore requires
15 ‘thermometer’ resistors for 4 more significant bits

$V_{\text{ref}}$ $R$ $R$ $R$ $R$ $R$ $R$ $R$ $2R$ $2R$ $2R$ $2R$ $2R$ $R$

$I$ $I$ $I$ $I$ $I/2$ $I/4$ $I/8$ $I/16$ $I/16$

$R$–$2R$ chain for 4 less significant bits

bit: 3 2 1 0 $I_+$

Figure 15.18 An 8-bit segmented DAC, where the 4 more significant bits use thermometer currents and the 4 less significant currents are generated by an $R$–$2R$ chain.

four resistors of $2R$ and five of $R$, giving 13 of $R$ in total (each $2R = R + R$). Thus the overall total is 28 resistors. The part of the DAC that generates the current is shown in figure 15.18.