Digital logic Families and converting between standards.

Introduction

A logic family is a collection of chips all using the same interior technology. The chips contain a collection of useful logical functions e.g. NAND gates, D latches, etc. Since all the chips in the same family share the same specifications, they can be interconnected without further thought and all work together. This concept of the family allows digital designers to concentrate on the logical design, knowing that the actual circuitry will be a simple interconnection job (hopefully!).

The oldest universal family is called the 7400 series. It was based on transistor, transistor logic - TTL. These first ‘74xx’ chips encapsulated a useful set of general purpose functions. So much so, that the old serial numbers (e.g. 74163) have rather taken on a life of their own and 74xx type numbers turn up in all logic families regardless of technology! We now often refer to chips using these building block functions as MSI (medium scale integration) chips.

A family is defined by its interfaces. The following are the most important.

- Power supply voltage.
- The voltage levels which signal logical values. These differ between inputs and outputs. The input range is wider so that it is certain that any output at the margin can be reliably detected.
- What input conditions are required.
- What are the characteristics of the outputs.

Other family characteristics are often of concern. Here are some:

- How many inputs of the same family can an output drive in parallel, called ‘fan out’.
- How many inputs of the family can be connected in parallel, called ‘fan in’.
- Output impedance.
- Input impedance.
- General current consumption and its characteristics.
- Operating speed.
- Maximum output current and is it symmetrical for logic high and for logic low.
- Dealing with unconnected inputs.
- The use of pull up or pull down resistors.

TTL.

This is the oldest of the universal logic technology. Introduced as the 7400 series, it has gone through many upgrades. TTL gets its name from the logic gate being fully transistorised. This was an innovation when it was introduced in the 1960s. It is often called bipolar logic to distinguish it from CMOS based devices. An outline gate shape (a NAND gate) is shown the figure. The characteristics of this logic family arise from the inputs which are...
emitters and the output which is taken from the collector of the transistor.

Characteristics of TTL

Power supply voltage: The basic (now called high voltage TTL) is 5Volts ±0.5 This is why the logic world standardised on 5V as the power supply value!

Voltage for Logic high:
- On output 2.7 – 5.0 V. On Input 2.0 – 5.0 V.

Voltage for logic low
- On output 0.5 – 0 V. On input 0.8 – 0 V.

Input conditions.
- Inputs require about 40 μA.
- Note that logic low on the input DRAWS current from the input (because it is an emitter connection).

Output characteristics.
- Maximum source current on logic high: ~ 0.4 mA
- Maximum sink current on logic low : ~ 4 – 20 mA.

Notice that the characteristics of the TTL output are that they can sink lots of current compared to sourcing almost none. Thus they can not drive anything substantial on logic high but they can on logic low (e.g. an LED). The general current consumption of TTL is not good, they are heavy users of current hence power supplies are large. Switching transients are also large, so that big decoupling capacitors are mandatory. Their inputs can be left unconnected, but as this is never a good thing, unused inputs should use pull up or pull down resistors to keep them safe. Because of the internal connections in a TTL output, the internal pull up is weak. Thus it can happen that external pull up resistors may be needed if the output is connected to a device with high impedance inputs (e.g. a CMOS device).

Low voltage ttl families

The old standard of 5 volts for logic being used less and less. As logic chips become more complex their power consumption increases. By lowering the supply voltage, this can be reduced. Hence the latest logic families have supply voltages of, 3.3, 2.5 and down to 1.8 Volts. The thresholds for logic high and low are thus also changed.

CMOS technology.

CMOS is a later development than TTL. This is the technology that now dominates the big VLSI chips because of its inherently low quiescent current consumption. CMOS gates only consume current when they switch and take only micro Amps when in steady state. The first logic family which used CMOS was the 4000 series. In a similar way to the 7400 series some of the part numbers have taken on a life of their own (e.g. the 4511 BCD to 7 segment decoder). The 4000 series in its original form was rather slow (~2 MHz) but modern variants are faster so it now competes and CMOS versions of 7400 devices, e.g. 74HCxxx series are available. CMOS is more flexible in its power supply requirements than TTL and its logic voltage levels are defined differently. The gate design (an inverter) is shown in the figure. It can immediately be seen that the CMOS gate is like two switches, one to power rail and the other to the ground rail.
Characteristics of CMOS logic.

Power supply voltage.

In 4000 series, this can be from 3 to 18V. In 74HC types this is less, ~4 to 6V. Newer series are lower with supplies down to 1.8V

Voltage for logic high:

70% of supply voltage. However, in 74HC series, this is modified to be more TTL like and for 74HCT devices it is the same as ttl.

Voltage for logic low.

30% of supply voltage. Again for HC and specifically for HCT types the levels are closely those of TTL.

Input conditions

Inputs are very high impedance and can be sensitive to electrostatic discharge. The input can be approximated as drawing virtually no current, micro or even nano Amps.

Output characteristics.

CMOS outputs are symmetrical, that is, they can sink as much current as they can source. Their output is often not very potent, the 4000 series was only ~ 2 mA.

With their symmetrical output drive they are unlike TTL outputs, but with their low current sourcing, they generally need buffer drivers if they are to drive bigger items. They do not need pull up resistors on their outputs as the output is driven positively either high or low. Their output impedance is that of the drive gate channel, it can be appreciable, so this must be taken into account if maximum current is to be drawn. Input impedance is very high. This has consequences for unconnected inputs, which float unpredictably and should always be connected to ground or high for safety. CMOS has very good current consumption, that is, very low, as they only consume current when they are switching. Hence their current requirements go up as the switching rate (clock speed) goes up. The 4000 series was rather slow, later families were better. As MSI devices they are not the fastest, however as VLSI, this is the technology in use for the biggest devices.

Interfacing between different families

Since there are now many families of logic in regular use there is a need to be able to translate between them e.g. 3V -> 5V or 5V -> 3V. It is often found that mixed systems are necessary particularly microprocessors at 3v3 need to talk to peripheral chips at 5V. Hence there is a need for logic translation in both directions and even cases where bidirectional busses need to be translated.

Compliant devices

The simplest case is where the target device is compliant or tolerant. That is the device (and it is usually 3v3 devices) has inputs which can take 5V without damage. The MAX7000 PLD devices are in that category. Some microprocessors can also do this. Their output, however, is still only at the 3V levels. This may not be a problem, since the 5V logic level for logic 1 is 2.7V and CMOS outputs can be at that level. Some devices have an extra power pin so that the outputs can actually drive to the required different logic level (some of the Altera PLD devices can do this).

Specialised chips

There are a variety of specialised buffering chips from all the major logic manufacturers. Some can also deal with bidirectional busses.
Trick, using 74HCT buffers
The normal 3V logic levels overlap the 5V ttl levels. Hence a 3V device can legally drive a 5V ttl device, so an HCT device (CMOS, so low input current, but logic levels defined as ttl) will properly read the outputs from a 3v3 device but, since it is a 5V part, the outputs will be 5V logic compliant. Here is an example showing buffering of the SPI connection between a Freescale Kinetis 3 volt microprocessor and a 5V Maxim LED display driver. Since the device (the 74HCT04) is an array of inverters, two are needed in series.

Going from 5V to 3V
The simplest is to use a voltage divider as per the diagram. It would be expected that the input of the 3v3 device is of CMOS type and hence need little current, but check!

A general alternative is to use a transistor inverter. This can do conversions to higher or lower voltages.

The resistor values are chosen to limit the current when the transistor is ‘on’. The ‘on’ voltage across the transistor needs to be checked to ensure that it is less than the logic ‘0’ threshold. This circuit will also work from 5 to 3 volts and for much larger voltages. When the input voltage side is higher than the output side, care needs to be taken to ensure that the transistor or FET can take such a condition on its base, or gate.